P R L

T E C H N I C A L N O T E

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PC CLONE DESIGN WITH PASSIVE BACKPLANE

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DOCUMENT CONTROL AND DATA SHEET

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12.	Abstract	:	A simplified design of IBM compatible PC has been described. The motherboard logic has been realized in two plug-in printed circuit boards. Passive PC Bus backplane is used for interconnection as well as other plug-in cards.
13.	Key words	:	Personal Computer (PC), 8088 Laboratory automation, PC motherboard, Passive Backplane.
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CONTENTS

APPENDICES

LIST OF ILLUSTRATIONS

PC CLONE DESIGN WITH PASSIVE BACKPLANE

The PC has become the backbone of office as well as laboratory automation.The environment of laboratory automation is somewhat different in that it is often the laboratory staff who has to take up the responsibility of maintenance of the PC alongwith the specialised plug in cards .The pressure of ever increasing complexities of the PC, as a consequence of development in technology ,has brought the difficulty of chip level maintenance .A large number of applications do not demand performance beyond that of a Vanilla PC from the hardware, and arithmatic operations are either nonexistent or just minimal.A simplified design of PC with passive backplane approach and dual board implementation of logic has been attempted by the author.This simplified dual board unit can be utilised for general laboratory applications.

KEYWORDS:Personal Computer (PC),8Ø88,Laboratory automation, PC motherboard,Passive Backplane.

1.Ø INTRODUCTION

The importance of PC in our day to day work is beyond dispute.The original 8Ø88 in the PC has been , by and large ,replaced by the newer and faster microprocessors like 8Ø286,8Ø386 and 8Ø486.As far as the manufacturer is concerned ,the microcomputer motherboard,for the various types of PC's and upgrades , in general , is not very different as a unit item ,be it 8Ø88 based or 8Ø286 based for that matter.The glue logic has been integrated alongwith the peripherals to such an extent that just one or two surface mount devices are sufficient to interface the microprocessor to the memory and other remaining peripherals. The circuit details, placement of parts and configuration details ,of the commercial PC motherboards , are most often not available , which creates difficulty in undertaking the repairs.Most of the time ,sheer difficulty of handling surface mount devices, forces one to abandon attempts to repair.

The basic PC based on 8Ø88 is very well documented, thanks to its originator IBM, and lends itself to easy repair.The general laboratory and other requirements can often be met by the simple PC itself and it is worthwhile to assemble one's own unit as an embedded unit.Availability of the V2Ø microprocessor from NEC ,which is pin compatible to 8Ø88 and executes binary arithmatic instructions faster as well,has helped vanilla PC to retain its place.A simplified design of PC has been attempted by the author to reduce chip count and save printed circuit board space.The use of passive backplane bus has also been resorted at to reduce the printed circuit board area.The rest of the

circuitry has been partitioned to accomodate it in two printed circuit boards of moderate size which are both electrically as well as mechanically compatible to I/O channel , sometimes referred to as PCBUS. These have been interconnected by means of passive backplane PCBUS . The peripheral cards can also be plugged in the same bus to complete the system .

2.Ø DESIGN

The block diagram of the motherboard logic has been shown in fig. 1 .The overall design of the system has been simplified to save the chip count and consequently reduce the printed circuit board area .Design of a PC compatible appeared in the BYTE magazine during 1982 (2) .However the PC described therein deviated from the IBM design substantially and compatibility was maintained only at BUS level and not at the BIOS level.

Another series of articles appeared in the Electronics For You magazine during 1989 by Padmanabhan et. al.(4).This design went very close to the IBM design except that it was based on the special keyboard .The hardware was,however, compatible to PC at the BIOS level.Several useful boards have been described in the series and the article series forms excellent material for understanding the working of the PC hardware. Some alterations were attempted for the Color Graphics Adapter (CGA) card.The CGA and floppy disk controller cards described therein are totally compatible to those available in the market.Use of standard XT/AT keyboard available in the market is , however, preferable as the ones offered are fairly cost effective and ergonomically designed for operator comfort,but the difficulty lies with the motherboards which are usually without proper documentation .

The role of numeric coprocessor 8087, in a PC ,is limited to programs requiring numerical computations ,and would remain underused in a PC meant for for control applications. The coprocessor requires the use of maximum mode of operation of the 8088 for proper interfacing, thus necessitating elaborate hardware for direct memory access (DMA) and related circuits. If on the other hand, the CPU is operated in the minimum mode, the hardware gets simplified to a large extent and this fact had been utilised by Padmanabhan in his design to save hardware.The motherboard was designed on the lines of the industry standard motherboard concept , except that it has been constructed out of double sided printed circuit board as compared to multilayer (5 layer in some cases) motherboards of the standard PC's.However it required a set of eight conductor ribbon cable jumpers which are likely to create reliability problems in the long run.

The author tried to eliminate some of these problems by partitioning the motherboard circuit in such a way that the mother board circuitry could be accomodated in two printed circuit boards of the double sided type.These two should be such that they interface only at the PCBUS level so that a passive back plane of 62 pin connectors could be used to interconnect the two PCB's just like any other peripheral card on the expansion bus.A close scrutiny of the PC hardware reveals that the only section which could be separated in this manner is the memory.Therefore the CPU and all associated hardware has been accomodated on one of the two printed cicuit boards while all the memory ,DRAM as well as ROM , on the other.As the memory

requires separate buffers for data as well as address on the motherboard , this partitioning seemed to be most appropriate.

2.1 THE CPU AND CLOCK

The 8088 has been configured for the minimum mode operation with max/min pin pulled up to Vcc.The RD*,WR* and IO/M* signals have been decoded in a tristate quad 2 to 1 multiplexer type 74LS257 , to generate IOW*,IOR*,MW*and MR* signals.These have been used on the CPU board as control signals for different sections.During the DMA cycle, these are tristated by the AEN signal and the one's generated by the DMA controller , which have also been connected to the same lines, take control. The clock , wait state ,bus arbitration and decoding logic has been shown in fig,2.

The clock and reset signal generator type 8284 has been used for the generation of these signals.The oscillator frequency of 14.318 MHz has been chosen for the sake of compatibility to the CGA and the standard BIOS.The clock output is high for 33% of its period and low for 67% ,which meets the requirements of the processor.The DMA controller type 8237A -5 requires a clock high period of 80 nsec and low of 68 nsec.The 8088 operating at 5 MHz requires clock Hi period of 69 nsec and clock low of 118 nsec.Therefore the clock for the 8237A can easily be derived by inverting the CPU clock (8).The designs described in BYTE as well as the IBM technical reference manual instead required use of pulse streching circuitry which may be avoided to save one IC.

The synchronization of the HOLD signal to the CPU is done with the help of one section of a quad D flip flop type 74LS175.The two other stages of this IC are used for providing

delay to the HLDA (Hold Acknowledge) signal from the CPU.The output of the first stage is the AEN signal and that of the next stage is used to give enable signal to the clock and reset logic in 8284.The AEN signal is sufficient for control of DMA logic(9). The 8237A is connected to the microprocessor bus in such a way that its data lines are driven from the buffered data bus driving all the I/O devices on board.The address lines AØ -A7 are output by the 8237A during the DMA cycle while the lines AØ - A3 receive information from the microprocessor during the CPU cycle and A4-A7 remain tristated during the same period.The change of data direction for these lines has been controlled by the AEN signal with the help of a bidirectional 8 bit buffer type 74 LS 245. The circuit details of CPU and DMA logic has been shown in fig.3.

The control signals IOR*,IOW*,MR*,MW* have been generated with the help of 74LS257 as said earlier and have been used to drive the corresponding lines of the I/O devices on board including the DMA controller 8237A.The latter generates these signals during the DMA cycle and becomes the master, while the 74LS257 is tristated during this period with the help of the AEN signal.The Hi address lines A8-A15 are generated by the 8237A during DMA cycle and presented on the its data lines which are latched in the 8 bit latch type 74LS373 with the help of the ADSTB pulse available at pin 8 of the 8237A.These address lines are enabled by the AEN* signal so as to become active only during the DMA cycle.The address lines A16-A19, during the DMA cycle , are provided by the 4X4 bit register file type

74LS67Ø.This information has to be latched in the latter before starting the DMA operation.These are located at addresses Ø8ØH,Ø81H,Ø82H and Ø83H in the I/O space of the microprocessor.

The control signals are directly available on the pins of the CPU in the minimum mode of operation .The multiplexed address and data bus ADØ-AD7, of the microprocessor drives an 8 bit latch type 74LS373 as well as an 8 bit bidirectional buffer type 74LS245.While the latch is used to separate the address lines AØ-A7 with help of ALE pulse available on the CPU ,the buffer provides drive to the data bus and its output is connected to the data lines of the 62 pin edge connector.The same have also been connected to another buffer of the same type to provide extra drive signal and isolate the onboard I/O devices.Eventhough the address lines A8-A15 are continuous from the CPU, these have been latched in a way akin to the address lines AØ-A7.The most significant address lines A16-A19 have been latched by ALE pulse in the same manner .All these address lines are brought on the edge connector and enabled by the AEN signal described before.The address lines generated by the DMA logic have also been joined to the same corresponding pins.

The control signals AEN,IOR*,IOW*,MR* and MW* , system clock of 4.77 MHz,oscillator output of 14.318 MHz along with the RESET signal are buffered in an 8 bit buffer 74LS245 ,which is enabled permanently,to provide adequate drive ,before bringing to the 62 pin edge connector.The I/O channel (backplane BUS) edge connector pinouts have been given in the Appendix A.

2.2 WAIT STATE LOGIC

The wait state logic has been implemented by dual D flip flop and triple 3 input NAND gate 741Ø.The clock of the first flip flop (FF) is generated if either I/O read or write operation is in progrss i.e. either IOR* or IOW* is low ,while AEN is low.Clock will also be generated whenever MR* goes low During the DMA cycle, indicated by AEN high ,provided DACKØ is also high . This indicates DMA channel request being serviced except for channel zero . Thus the first FF will get a clock pulse during I/O operation as well as memory read operation during DMA .This pulse sets the first flip flop, the Q output of which sets CPURDY* signal high thereby giving a nonready condition to the CPU.The next CPU clock sets the second FF which in turn resets the first one to give ready signal to 8284.Thus a single wait state is inserted for all I/O operations during non DMA cycle as well as memory read operations during DMA cycle .During DMA the IOW* signal originates in the DMA controller.The external memory or I/O devices located on the different boards on the I/O bus can insert wait states by pulling down the IOCHRDY line for as long a time as they please, except violating the refresh requirements. Pulling IOCHRDY low forces FF 1 to go high and give non ready condition to the CPU. Ready to DMA is generated by Q* output of the FF 1 and is restored by next clock pulse , in case Q* is reset to high , or else can extend to longer periods.Delayed AEN is used as AEN84 and CPURDY is driven by Q output of FF 1.As long as the Q output of FF1 is high ,the RDY to DMA will be held low to create non ready condition to the DMA

logic.The ready will be given only after the IOCHRDY is released and then RDY to DMA is restored from the next CPU clock . The circuit details of the wait state logic have been given in fig.2.

2.3 ONBOARD I/O CIRCUITS

The details of the onboard I/O circuits have been given in fig.4. The devices located on the data bus are programmable input output device 8255, programmable timer type 8253, DMA controller type 8237A,interrupt controller 8259A and the 4X4 register file 74LS67Ø. The data bus has to drive several input outpput devices onboard and therefore a separate data bus buffer type 74LS245 has been used for this purpose , as explained earlier.This buffer is enabled during the I/O operation in the address space ØØØ-ØFFH of the microprocessor as well as interrupt acknowledge .The details of enable logic has been given in fig.3 . The address lines A8 and A9 have been OR'ed along with the IOR* signal and the output thereof NAND'ed with the INTA* signal to realise the DIR signal for the data buffer.The latter has been enabled by the AEN.Thus the buffer opens up only during the time when microprocessor is master,and data is read from the I/O devices only if the same are situated in the I/O address space below 1ØØH during which A8 as well as A9 are both zero.During interrupt acknowledge , the interrupt controller situated on the I/O bus sends the address vector on the data bus and pulls INTA* line low.Now the vector address will be read by the CPU, as the data buffer is also in read mode when INTA* is low.The buffer is in write mode in all other times and does not interfere with main data bus opertions as it it only a passive listener.

The programmable port type 8255 has been used for keyboard interface, reading the configuration switch and control of the speaker.The 8 configuration switches have been grouped in two sets of four and are sensed through a quad 2 input multiplexer type 74157,selection of the group being done by the port line PB3 .The switches themselves are read by the port lines PCØ-PC3.

The keyboard clock can be enabled or pulled low by software through the port line PB6.It is passed through 2 stages of D flip flops clocked by the PCLK signal to synchronize it before being used for data shift operation.Onboard reset signal is inverted to provide reset to the keyboard clock shift register and provide reset signal to the keyboard.The shift register is realised by 2 sections of the quad D flip flop type 74175,one of the other sections of which is used to divide the PCLK by 2 to provide clock to the timer at 1.19 MHz.

The keyboard data is fed to a serial to parallel converter type 74LS322, the 8th output QH' of which is stored in a D flip flop 7474.The Q output of the 7474 forms the keyboard interrupt IRQ1.The parallel output of the shift register 74LS322 is disabled when IRQ1 goes high and the keyboard data line is held low.The buffered and synchronised keyboard clock signal is now used for shifting the data in the 74LS322. The output of the shift register is read by bringing the line PB7 low, which is again made logical ONE to disable the outputs of the shift register and clear its contents.The D flip flop 7474 remains cleared when PB7 is high.The Port A of he 8255 is used for reading the keyboard data as well as to output the checkpoint

information during initialization.The PB7 is kept logical ONE to disable the shift register outputs during this period .

The 1.19 MHz square wave obtained by dividing the PCLK by 2 serves as clock to all the 3 sections of the programmable timer type 8253 .The output of timer Ø is used for time of the day application and it divides the clock by FFFFH to provide square wave at 18.2 Hz.This square wave gives interrupt at IRQØ line of the interrupt controller 8259A.The timer 1 is programmed to provide a pulse train with a period 15 microseconds to provide DMA request at pin DRQØ to the DMA controller.The latter in turn generates address lines in successive steps to provide refresh to the dynamic random access memeory (DRAM).Gate lines of timer Ø as well as 1 are pulled high.

The OUT2 of the timer is used for giving tone to the speaker under control from the PB1 line while the gate 2 is controlled by PBØ. The presence of speaker is detected by a high signal at PC4. Pins PB2 and PB4 are not used in the system and PB5 is used for I/O check enable operation.It resets a R-S flip flop, the out put of which is sensed at PC6.The PC5 line has been used to test the output of the speaker and PC7 has not been used as the parity check of DRAM has been dispensed with.The NMI input of the microprocessor has also been grounded for this reason.

The interrupt controller type 8259A has been interfaced to the microprocessor through INTR and INTA* lines and interrupt requests IRQ2 to IRQ7 have been brought to the 62 pin connector of I/O bus.IRQØ and IRQ1 have been used onboard for time of the day and keyboard interrupts respectively.

The address lines AØ and A1 which go to the I/O devices on board have not been buffered to reduce chip count and it is expected that the address buffer would have adequate drive to take this extra load from NMOS devices.The chip select signals for the I/O devices have been generated with the help of a 3 to 8 decoder type 74LS138 using address lines A5,A6 and A7 as inputs. The A8 OR A9 signal, obtained from quad 2 input OR gate 7432 , drives the enable input G1* of 74LS138 .The other enable input,G2*, is driven by the AEN signal , thus fulfilling the decoding requirements.The A8 OR A9 signal is again combined with IOR* in other section of 7432 and the output thus obtained is combined with INTA* signal in NAND gate to provide DIR signal for data bus buffer as explained earlier.The data buffer is enabled by AEN signal and the data is read from I/O devices if AEN is low and the I/O ports on board are selected.The pinouts of 8Ø88 have been given in fig.5 and the printed circuit board layout of the component and solder sides of the CPU board in figs. 7 and 8.

2.4 THE MEMORY CARD

Passive backplane PC has its own advantages. However all the circuits of the PC can not be accomodated on a three quarter size plug in card for the PCBUS without resort to use of LSI glue logic.The partitioning of the circuitry ,therefore,has to be done in such a way that , the two sections remain functionally somewhat independent and their interface does not go beyond the backplane bus.The memory occupies substantial area on the printed circuit board and mainly requires only address and data lines for operation.Therefore it is possible to split the motherboard

circuitry into two parts ,one containing all the memory including RAM and ROM and the other part containing the rest of the circuits.The availability of 256 K X 1 bit DRAM has made realisation of 512K byte RAM fairly simple with 16 such devices.These are pin compatible to the 64K units and thus down sizing the memory would also be possible in some applications.The newer devices are reported to be relatively free from soft errors and the parity check may be omitted altogether to gain some saving in hardware. As the parity check logic interfaces to the NMI pin of the microprocessor,the latter can be grounded and thus the memory block is further isolated from CPU and DMA logic , as far as circuit partitioning is concerned.

The dynamic RAM's are refreshed by use of one of the four DMA chamnnels ,channel zero, and the DACKØ line available on the I/O channel bus can be used for this purpose for the memory located on any card.A simple circuit consisting of address multiplexer ,and RAS*,CAS* generation logic using standard LSTTL gates has been designed to provide all the control signals.The 64K devices may be substituted in place fo 256K devices by a set of jumpers to get a RAM of 128 K bytes if needed. Two 28 pin sockets to accomodate one each of 8 K X 8 and 32 K X 8 EPROM's have also been provided on the memory PCB .These are located at FEØØØH and F6ØØØH in memory address space to serve for BIOS and BASIC ROM's respectively.The circuit diagram of the memory card and memory device pinouts have been given in the fig .6.

2.5 REFRESH LOGIC

The memory read and write signals available on the backplane have been used to generate refresh and multiplexer control signals for the DRAM.The MR* and MW* signals are combined in a NAND gate to generate basic memory request signal which is delayed in an R-C circuit to generate RAS* and then MUX signals.The RAS* signal is generated in the one half of the decoder type 74 LS 155 which is enabled by the RAM select logic.Separate RAS* signal is generated for each of the two banks of DRAM's. The MUX signal is used to enable the second part of the decoder to get the two CAS* signals, one for each of the memory banks.Inherent delay of the decoder serves to provide the necessary time delay to the CAS*signals from the MUX signal.These signals serve only for the actual read/write opreration of the memory.The refresh operation is enabled by OR'ing the RAS* signal generated at the output of the decoder with the RAS control signal which is active for every memory access cycle .The refresh RAS is enabled by the DACKØ signal to restrict the refresh action only under the control of the DMA controller.

Two types of access for the memory are needed during the normal read/ write operation.The DACKØ is logical 1 during such cycle and the RAS* as well as CAS* signals are generated for the selected memory bank.The refresh operation is continuously performed at intervals of 15 microseconds and in this period the RAS* signal generated by MR* and MW* is directly fed to the RAS* lines to provide refresh.The DMA controller provides refresh addresses on AØ-A9 lines during this period .The address

multiplexing is performed by a set of three units of quad 2 input multiplexers type 74LS157 .

The data bus of the memory card is buffered by bidirectional buffer type 74 LS 245 ,which is enabled during the time CPU makes an access to the RAM located from ØØØØØH to 8ØØØØH and ROM located at FØØØØH to FFFFFH.It is inhibited during the DMA operation on channel Ø by DACKØ.The memory decoder is enabled by DACKØ and memory bank address,while the addresses A16 and A17 are decoded to generate RAS* and CAS* signals for the two banks.These addresses are for the 64 K X 1 devices.For the case of 256 K X 1 devices the same would become A18 and A19.Memory bank address is generated by A17, A18,A19 for 64 K X 1 devices and just A19 for 256 K X 1 devices.

The EPROM select logic has been realised by decoder type 74LS156 of open collector type,which is enabled by the output of 4 input NAND gate 742Ø ,which generates logical Ø if address lines A16,A17,A18 and A19 are all logical 1 .As said earlier the chip select for FEØØØH -FFFFFH is for the BIOS and the one for F6ØØØH-FDFFFH for the BASIC ROM. The printed circuit board layout of the memory card has been given in fig.9.

3.Ø BACKPLANE AND POWER SUPPLY REQUIREMENTS

A passive 6 slot single sided back plane is sufficient to run the minimum system.The ground track is all around the PCB and the +5 v track is laid by thick lines wherever possible .An extra thick line has been provided for +5v line along the ground to reduce voltage drop .Additional jumpers have been used to reduce the same still further. The CPU, memory, Floppy Disk Drive

and the CGA cards together draw about 2.8 amperes of current from +5 v line.If the Floppy disk drive is provided +12 volts as well as +5 v from separate source,3 amp regulator of linear type can serve the system adequately.

4.Ø CONCLUSION

A passive backplane BUS based PC compatible motherboard has been designed .The CPU, DMA and I/O related logic have been located on one of the printed circuit boards and the memory on the other.A six slot passive backplane similar to the I/O channel bus of the PC has been used to interconnect the two to realise full motherboard logic.The peripheral adapters may be plugged in the remaining 4 slots to complete the system.

5.Ø ACKNOWLEDGEMENTS

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APPENDIX A

PC BUS (I/O CHANNEL BUS) SIGNALS

Connector type PCB Edge ,62 pin dual readout,Ø.1 inch

Pin No.	Component Side	Pin No.	Solder Side
A1	I/O CH CK*	B1	GND
A2	D7	B2	RESET DRV
A3	D6	B3	+5V
A4	D5	B4	IRQ2
A5	D4	B5	-5V
A6	D3	B6	DRQ2
A7	D2	B7	-12V
A8	D1	B8	CARD SELCTD*
A9	DØ	B9	+12V
A1Ø	I/O CH RDY	B1Ø	GND
A11	AEN	B11	MEMW*
A12	A19	B12	MEMR*
A13	A18	B13	IOW*
A14	A17	B14	IOR*
A15	A16	B15	DACK3*
A16	A15	B16	DRQ3
A17	A14	B17	DACK1*
A18	A13	B18	DRQ1
A19	A12	B19	DACKØ*
A2Ø	A11	B2Ø	CLOCK
A21	A1Ø	B21	IRQ7
A22	A9	B22	IRQ6
A23	A8	B23	IRQ5
A24	A7	B24	IRQ4
A25	A6	B25	IRQ3
A26	A5	B26	DACK2*
A27	A4	B27	T/C
A28	A3	B28	ALE
A29	A2	B29	+5V
A3Ø	A1	B3Ø	OSC
A31	AØ	B31	GND

APPENDIX B

LIST OF COMPONENTS

CPU board:

Integrated circuits:

1.	74LS125	16.	8088
2.	74LS175	17.	74LS00
3.	8253	18.	74LS257
4.	8237A	19.	8284A
5.	74LS373	20.	74LS00
6.	74LS373	21.	8255
7.	74LS373	22.	74LS74
8.	74LS175	23.	74LS10
9.	74LS00	24.	74LS32
10.	74LS322	25.	74LS138
11.	74LS00	26.	74LS245
12.	74LS74	27.	74LS245
13.	74LS670	28.	74LS245
14.	74LS245	29.	DIPSWITCH
15.	74LS373	30.	74LS157
		31.	8259A

CAPACITORS		RESISTORS	
10 pf	1	33 E ,100E &510 E	ea. 1
47 pf	3	1K2	1
300 pf	4	1K5	2
0.1 uf	5	2K	2
10 uf 10 v	3	4K7	2
		100 K	1
DIODE	1N4148	TRANSISTOR	2N2222 ea. 1

Memory board:

Integrated Circuits

IC 1-16		256K X1 bit Dynamic RAM
17.	74LS157	
18.	74LS157	
19.	74LS157	
2Ø.	74LS157	
21.	74LS257	
22.	27256	32KX8 bit EPROM
23.	74LS32	
24.	74LSØØ	
25	74LS156	
26.	74LSØ4	
27.	2764	8KX8 bit EPROM
28.	74LS2Ø	
29.	74LS245	

Capacitors		Resistors.	
33Ø pf	1	33 E	14
Ø.1 uf	15	47Ø E	1
1Øuf 1Ø v	1	1 K 5	3

APPENDIX C

Salient Features:

1. Minimum mode operation of 8088.
2. Standard Keyboard and Peripherals.
3. Passive , single sided backplane.
4. Separate CPU and Memory cards to use standard PC BUS, and small size double sided PCB's to realise 512 K DRAM along with 8K X 8 BIT and 32K X 8 bit EPROM,RAM configurable for 64 K, 128 K, 256 K and 512 K bytes.
5. Conservative artwork to improve reliability.
6. Use of standard MSI/SSI devices as glue logic for easy availability of spares for repairs.
7. Simple data direction logic for DMA.
8. Compatibility to standard BIOS .

APPENDIX D

LOAD ON 8088 PINS

AD0-AD7	2 LSTTL
AD8-AD15	1 LSTTL
INTA*	2 LSTTL
HLDA	2 LSTTL
IO/M*	2 LSTTL
RD* & WR*	1 LSTTL
ALE	4 LSTTL , buffered out on bus
AEN ('175)	10 LSTTL ,buffered out on bus

8284 SIGNALS:

SAYSCLK	6 LSTTL , buffered out on bus
PCLK	1 LSTTL
RESET	7 LSTTL , buffered out on bus
OSC	DIRECT on bus

BUS LOAD BY ON BOARD DEVICES :CPU BOARD:

A0	3 LSTTL +8253,8255,8259A
A1	4 LSTTL
A2-A4	NONE
A5-A8	1 LSTTL
A9	2 LSTTL
A10-A19	NONE
D0-D7	1 LSTTL

BUS BUFFER USED : 74LS245

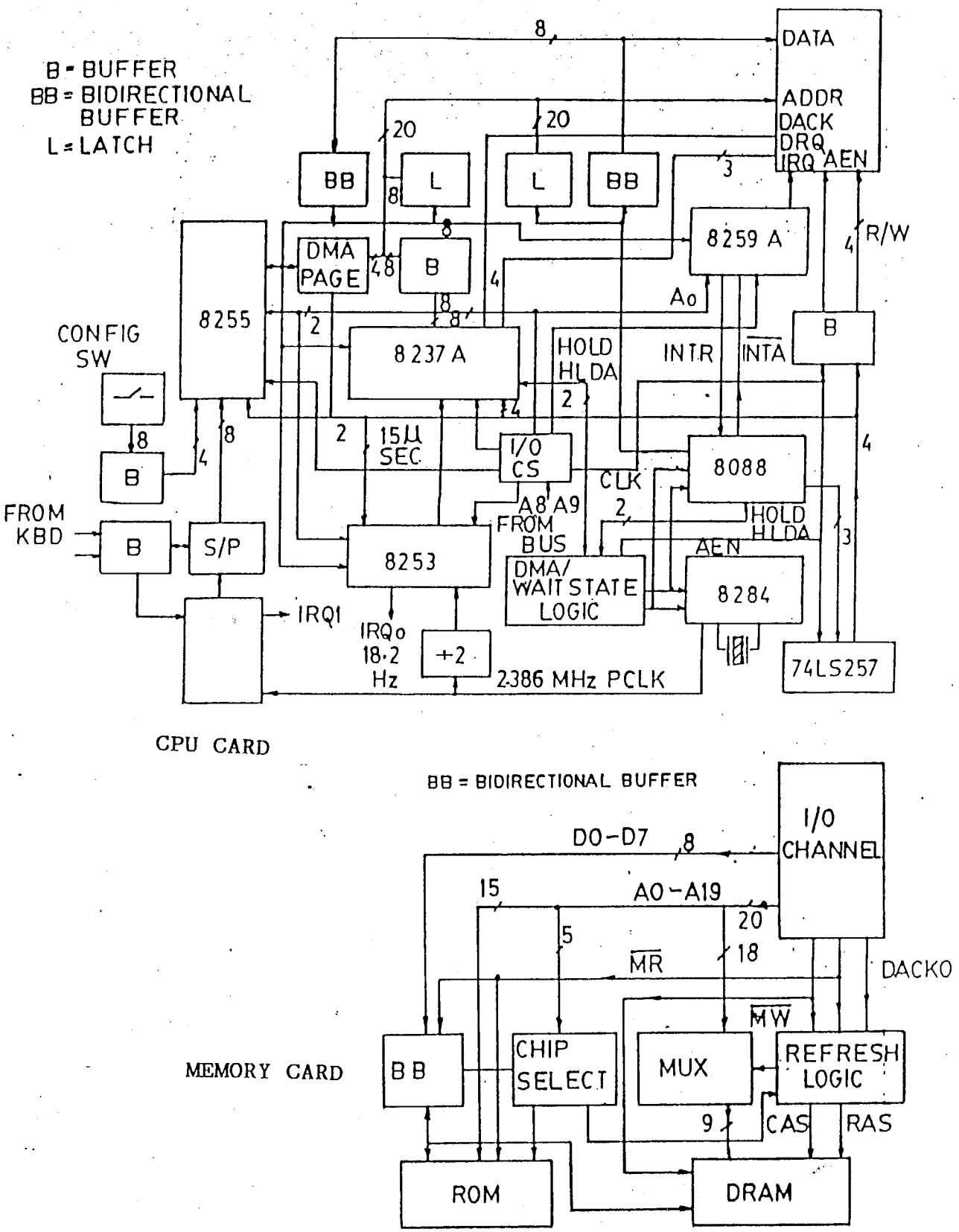


Fig. 1 BLOCK DIAGRAM OF MODIFIED PC HARDWARE

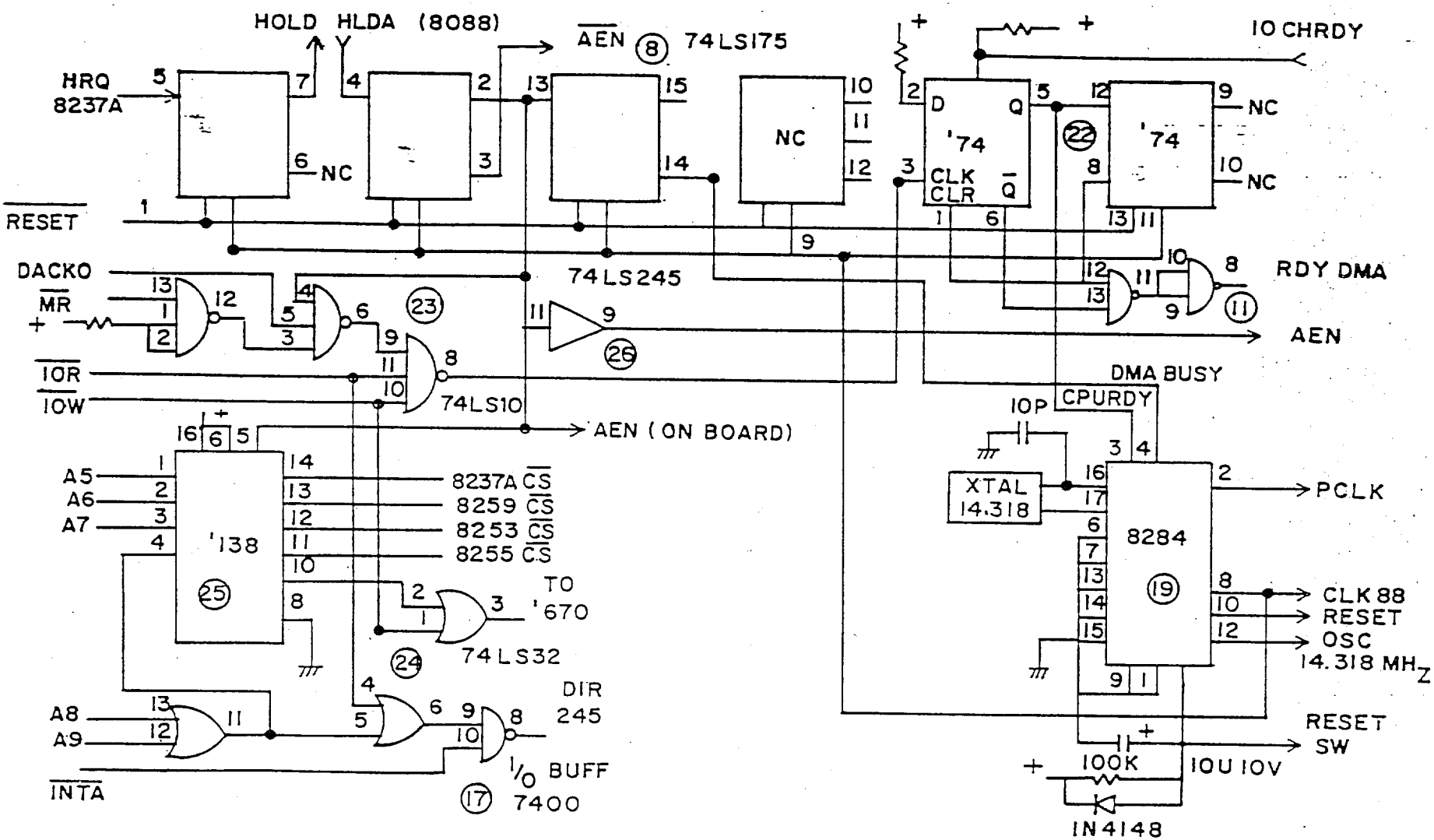


FIG.2CLOCK WAIT STATE, BUS ARBITRATION AND I/O SELECT

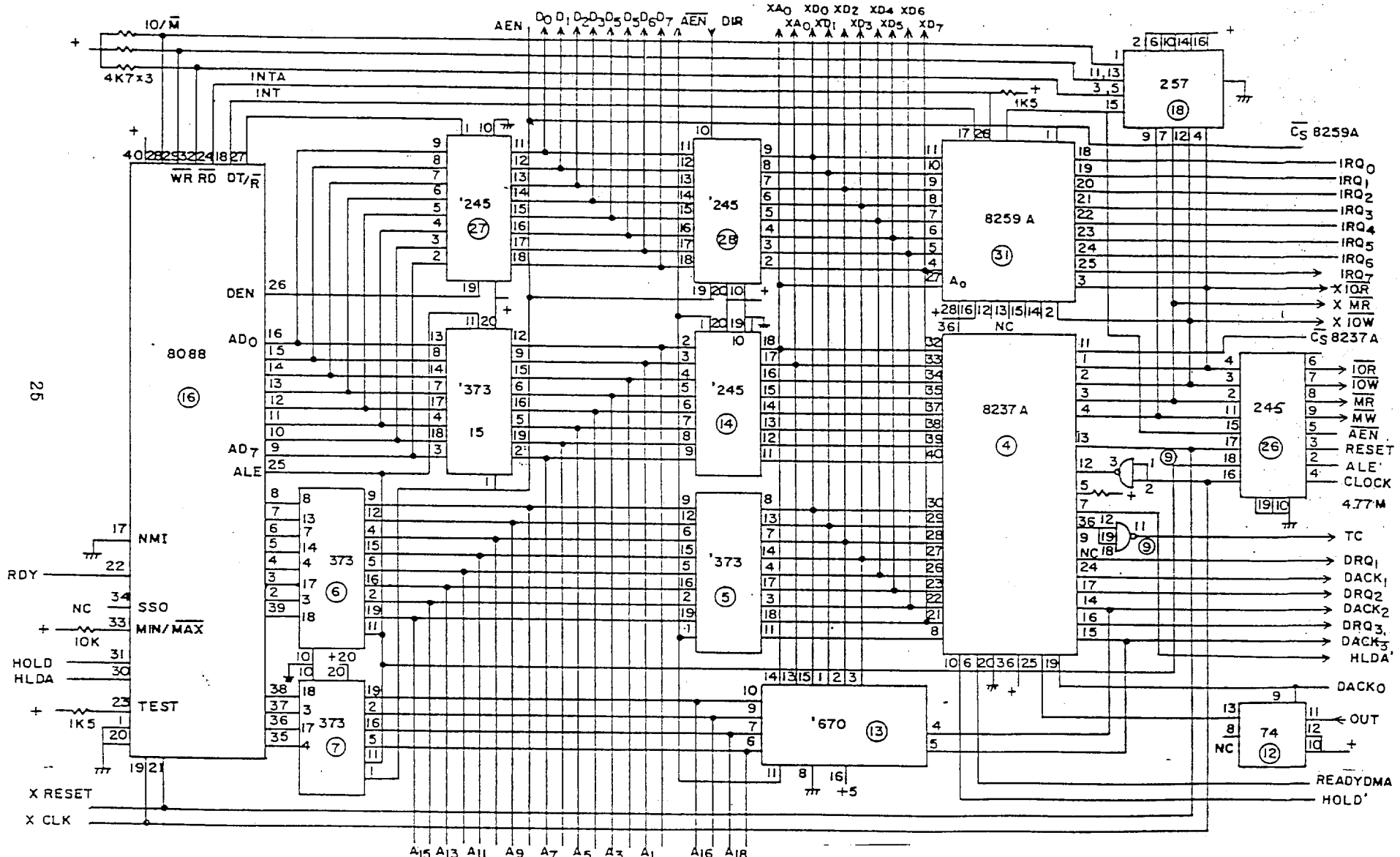


FIG. 3 CPU, DMA AND INTERRUPT

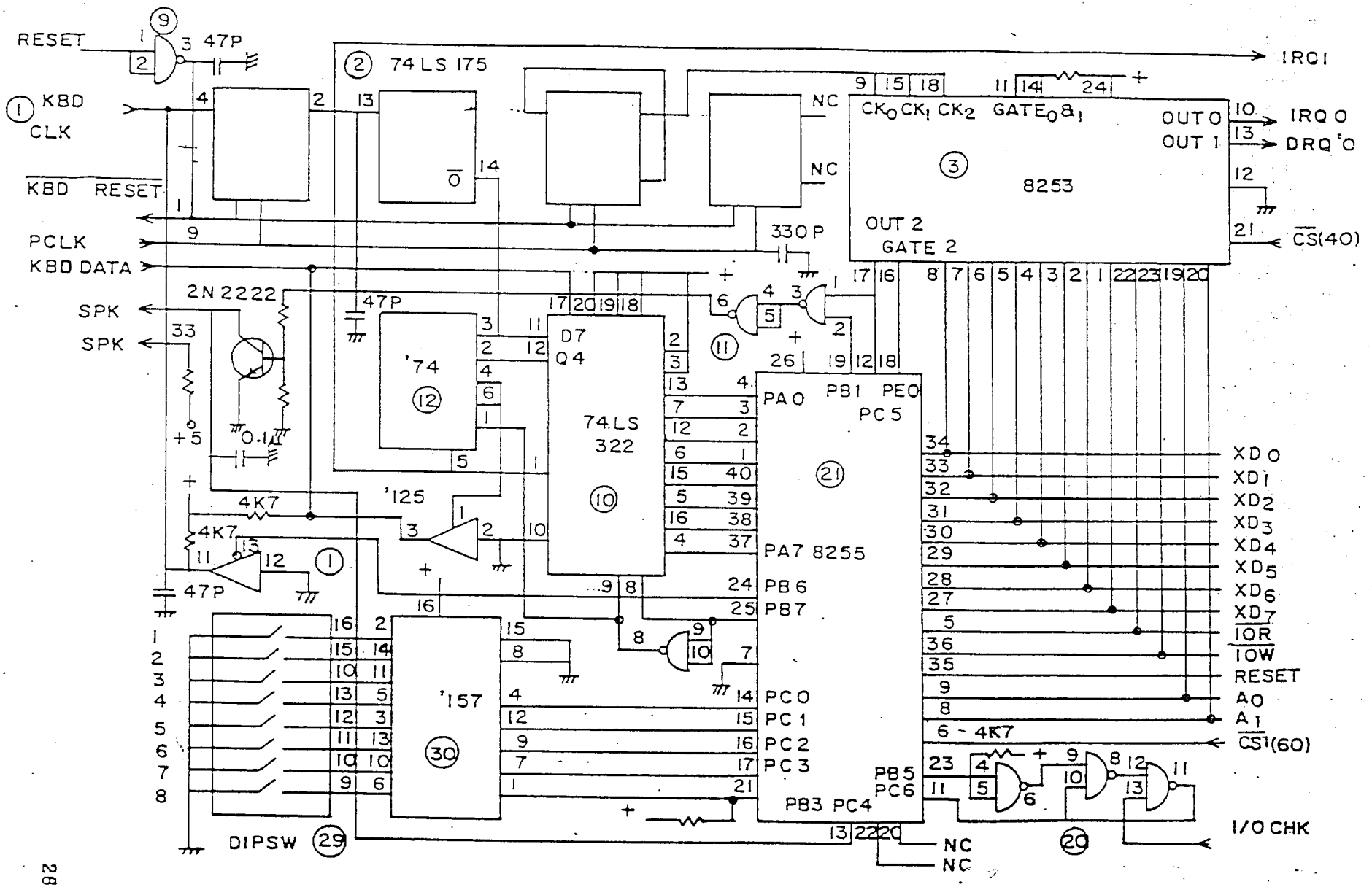


FIG 4. CONFIGURATION, TIMER, KEY BOARD LOGIC

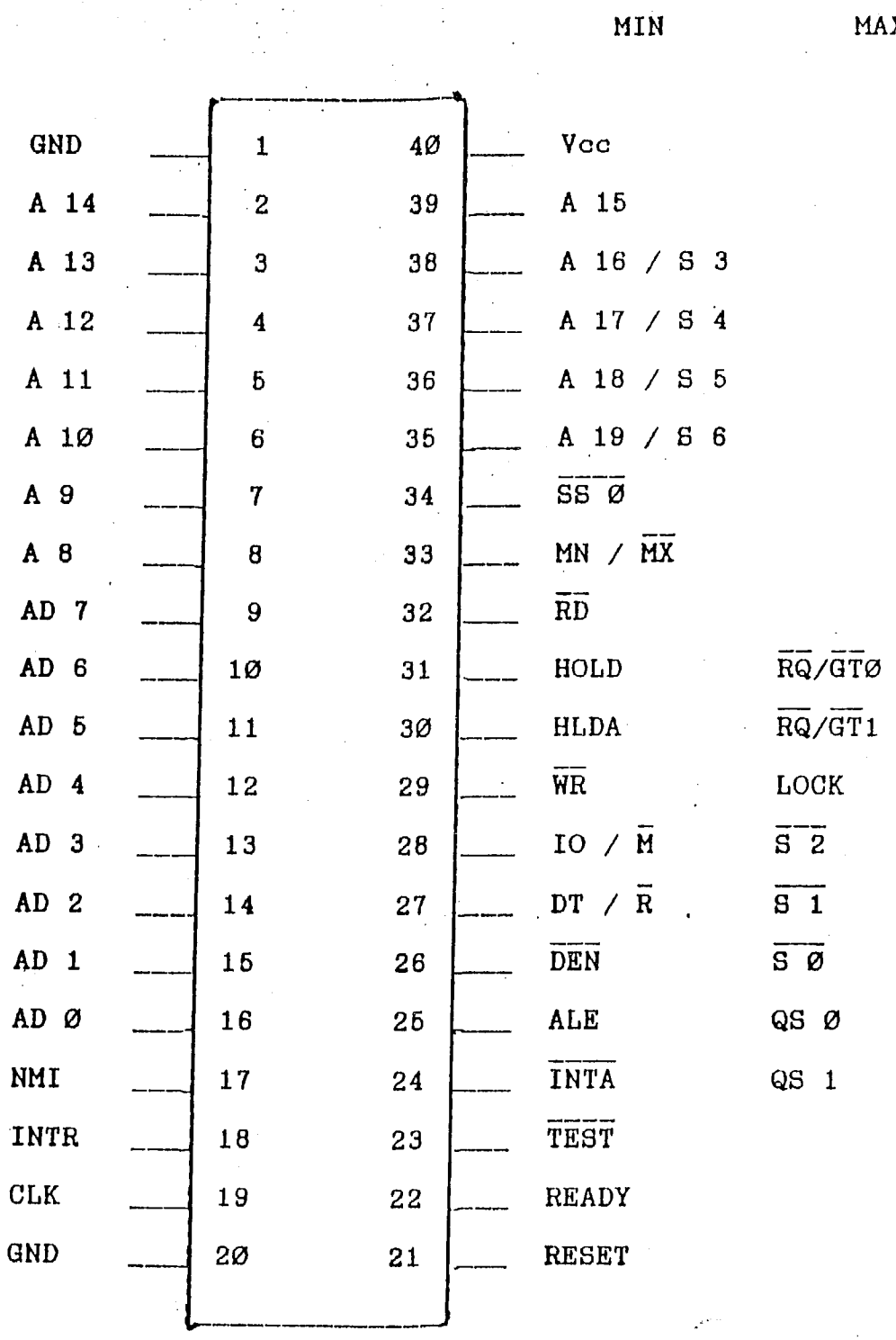


FIG. 5 - PINOUTS OF 8088

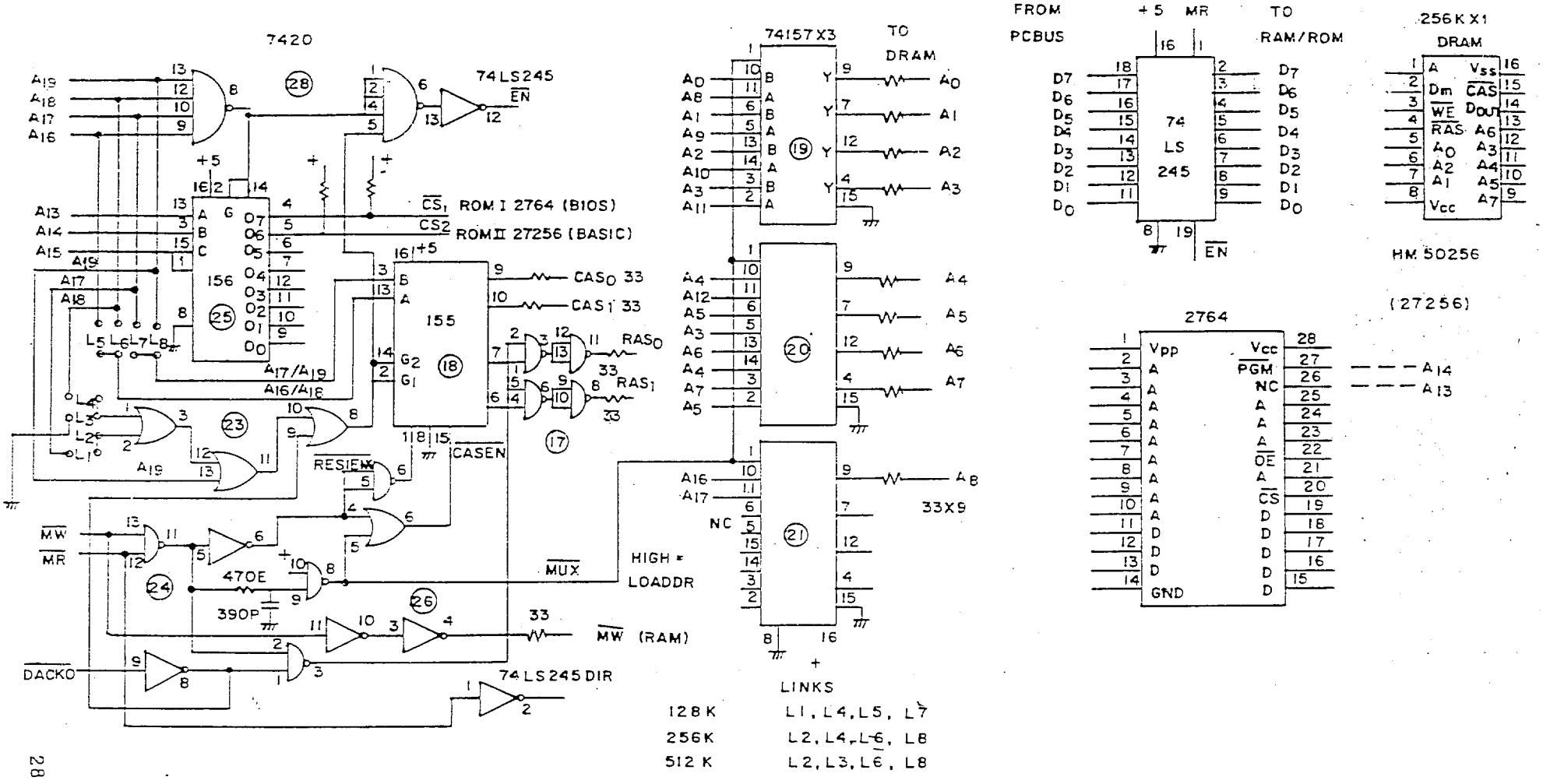


FIG. 6 MEMORY CARD

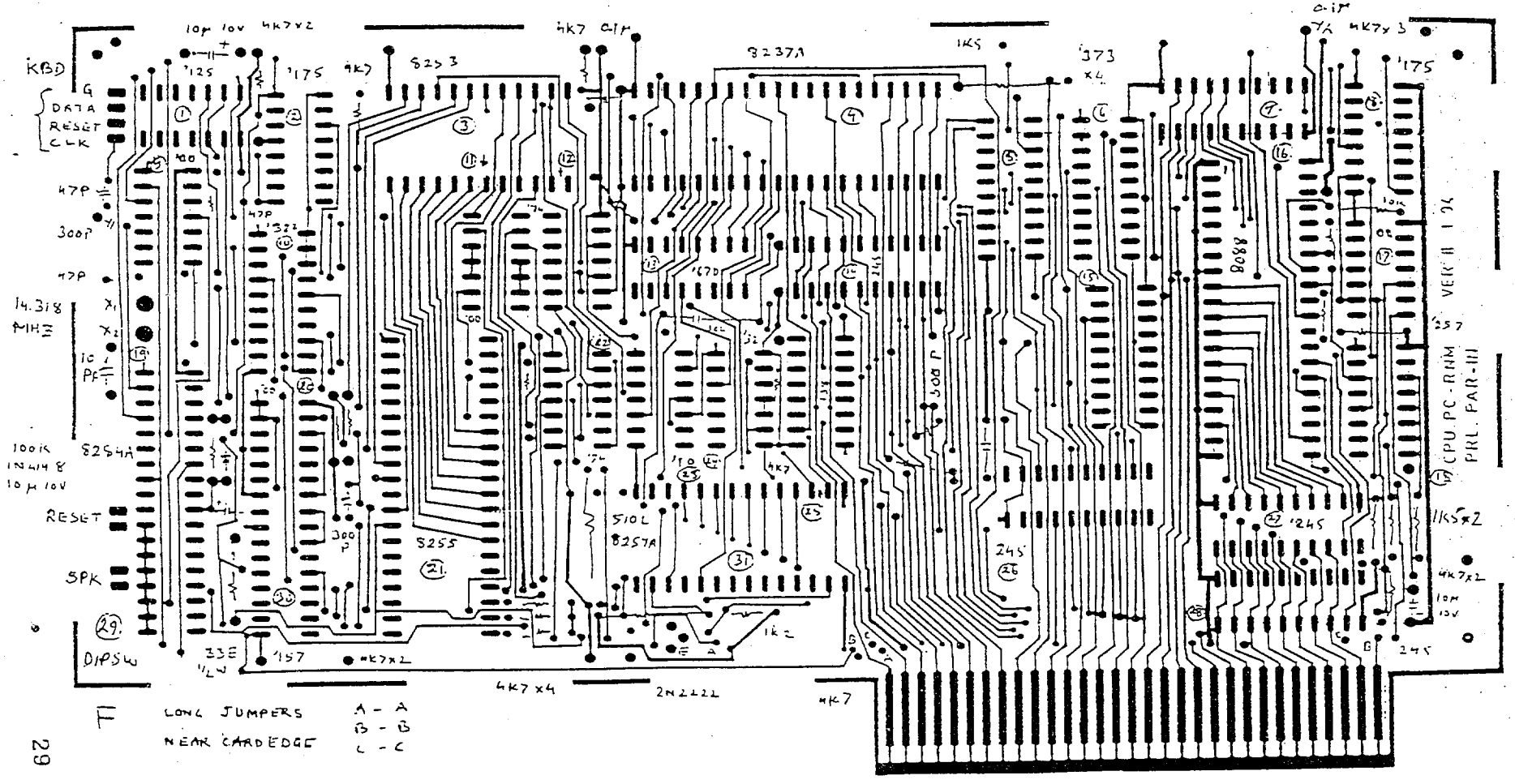


Fig. 7. Printed circuit Board layout of the CPU card

: Component side

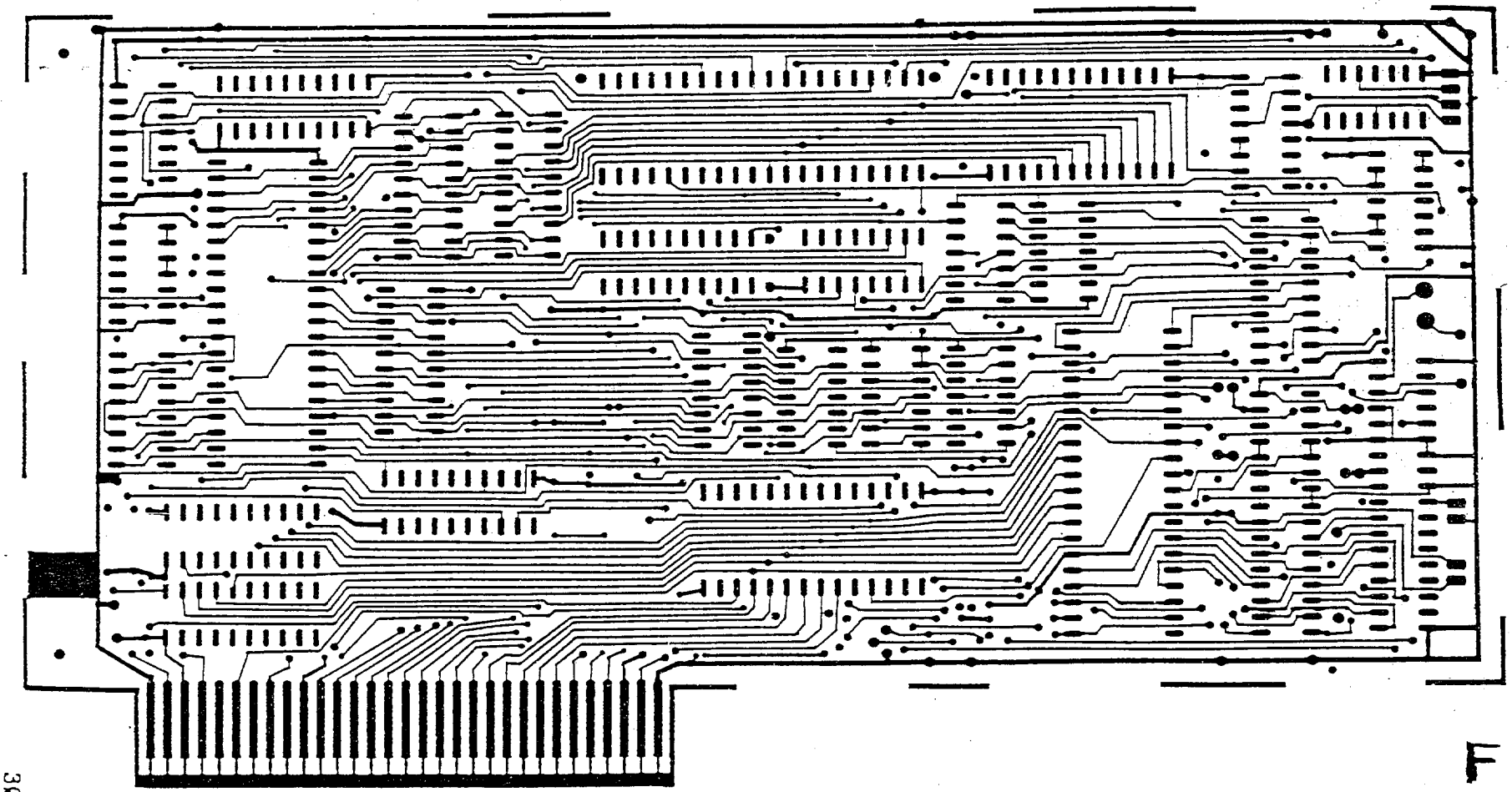
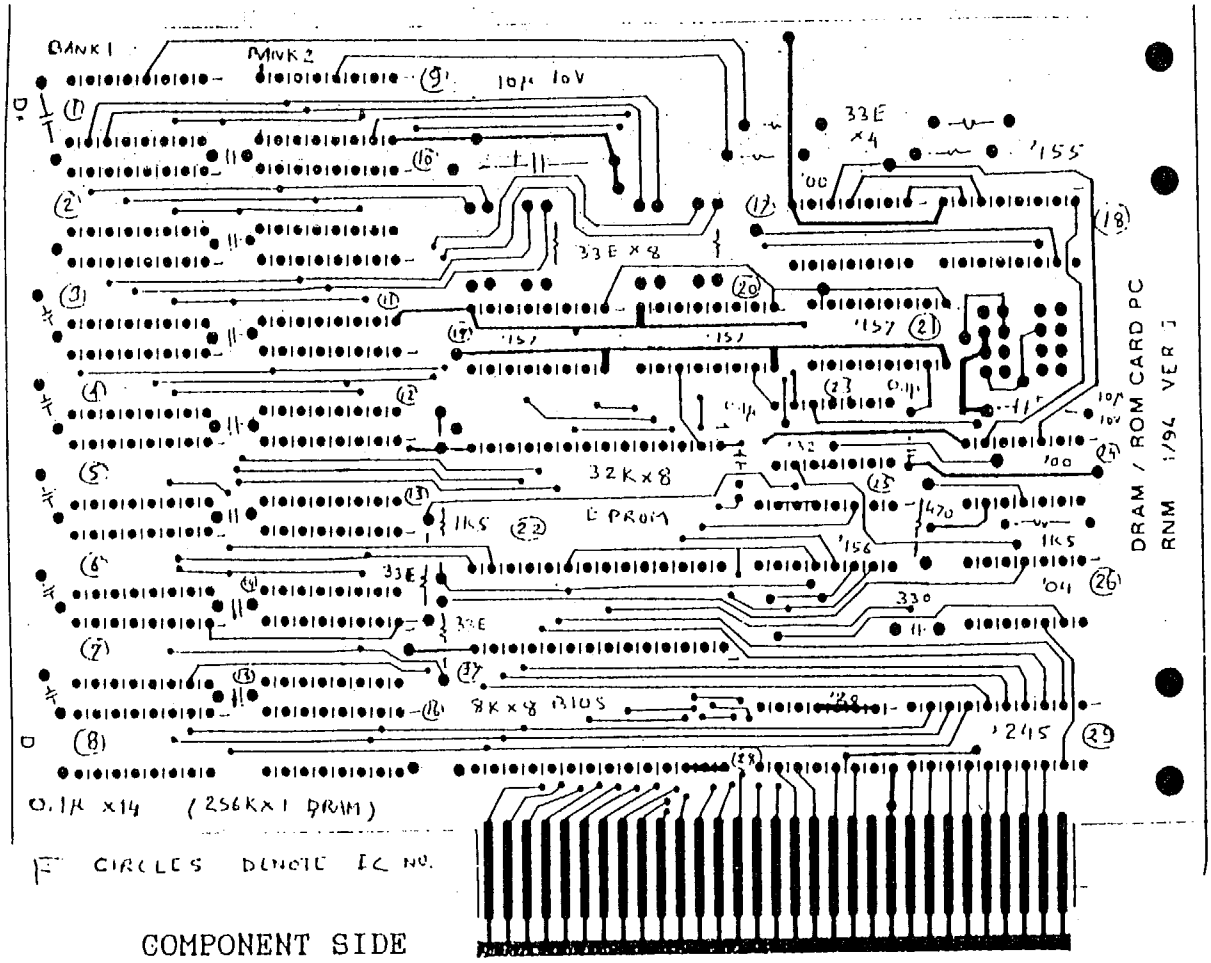


Fig. 8. Printed circuit Board layout of the CPU card

: Solder side



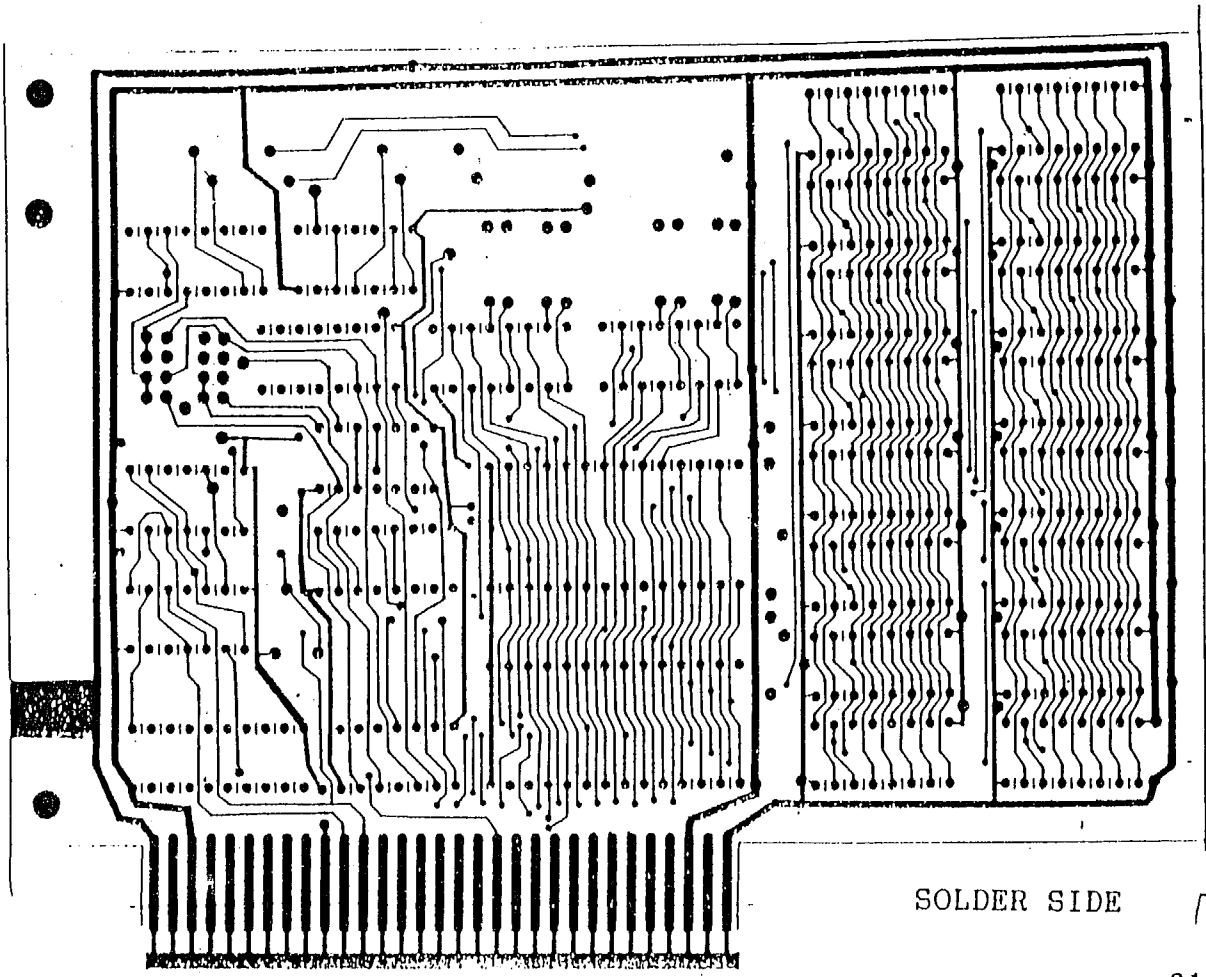


Fig. 9. Printed circuit Board layout of the Memory card