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FOUR CHANNEL AUDIO CASSETTE BASED

DATA RECORDER

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DOCUMENT CONTROL AND DATA SHEET

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FOUR CHANNEL AUDIO CASSETTE BASED DATA RECORDER

R.N.Misra

ABSTRACT

A four channel data recording system based on audio cassette recorder has been designed. The channels have sampling rate of 5 per second and can be paralleled to provide two channels of 10 per second or one channel of 20 per second. The system has been designed around a 8085A microprocessor and has facilities for software debugging as well. The current date, time and three character station code can be entered through the keyboard, which gets displayed on the seven segment display during the execution of the main recording program. Time is updated by software and station and time codes are recorded along with the data in the beginning of the data block. The instrument has facility to read the data from the cassette tape for verification and transfer to floppy or hard disk of a PC, if so desired.

Keywords: Data Recorder, Audio Cassette, Microprocessor, 8085A, Instrumentation.

1. INTRODUCTION

Audio cassette recorder is a cost effective device for unattended recording of data. It can be easily driven under microprocessor control to realise a data recording instrument that can replace a pen and ink type recorder. A four channel data recorder based on 8085A microprocessor has been designed for such applications. The microprocessor controls the multiplexer, data acquisition, storage and subsequent recording on the audio cassette in block mode. It also updates a real time clock under software control. The current time, day of the year, year and station code are recorded in the beginning of every block to facilitate data analysis. The instrument has a keyboard, fifteen nos of 7 segment displays and a set of eight LED's which facilitate control of the instrument. The keyboard is used for entering time and station code and initiating the data recording. The seven segment displays indicate memory address and contents during the initialisation as in common microprocessor kits and station code, year, day of the year and current time during the operation of the instrument. The eight LED's display recording status. The keyboard and the displays have been located on the front panel, which has a gentle slope to provide comfort to the operator. The system reset is provided on the keyboard and the power on-off, as well as record /play switches have been located on the rear panel of the instrument. It can also be used as a microprocessor

kit similar to SDK-85 on power-up. An additional switch located on the rear panel selects RS232C port for this purpose. The baud rate has been fixed at 1200 by software.

2.0 DESIGN

The block diagram of the instrument has been given in fig.1. It consists of four distinct parts, the microcomputer, keyboard/display, data conversion /tape interface electronics and power supply. These have been covered in the following sections.

2.1 THE MICROCOMPUTER

The microcomputer has been designed around 8085A microprocessor. It is a small, single board computer designed to be software compatible to SDK-85 of Intel. The block diagram of the microcomputer has been given in the fig.2. The board has been covered in detail elsewhere (Ref.1), and only its salient features would be discussed here.

The microcomputer uses 8212 latch for generation of stable low address lines A0-A7 and 8155 as general I/O device. The 8253 and 8251 have been used for generation of various timing signals and sending serial data to the cassette tape write electronics. MR*, MW*, IOW* and IOR* signals have been generated from RD*, WR* and IO/M* signals of the 8085A with the help of three to eight decoder type 74LS138. Another 74LS138 has been used for generation of chip select signals for memory and I/O. A dual 2 to 4

decoder type 74LS155 has been used for generation of chip select signals for 4K EPROM type 2732 and the two 8K RAM's type 6264. While the 74LS155 has been wired on a piggyback board, The two 6264's have been accommodated in one socket of 6116 by mounting those one over the other. Chip select lines of 2732 and 6264 as well as A12, Vcc and WE*(MW*) have been wired point to point. The memory and I/O maps and decoding logic has been given in fig.3.

2.2 KEYBOARD AND DISPLAY

A keyboard consisting of 24 single contact key switches has been used for controlling the system. A set of eight LED's are used for displaying the status information and fifteen 7 segment LED displays for station code and time. The display codes for alphanumeric data stored in ASCII and segment assignments of 7 segment displays have been given in appendix C and D. The keyboard and display have been accommodated on a single pcb which has been mounted just behind the front panel. The circuit diagram of the keyboard display unit has been given in fig.6. It is based on the keyboard display controller type 8279 of INTEL. The scan lines SC0-SC2 of 8279 are decoded in a 3 to 8 decoder type 74LS138, the first three outputs O0, O1, O2 of which have been used for scanning the key matrix. Two additional decoders of the same type have been used for decoding all the four scan lines SC0-SC3 for scanning the common anodes of the 7 segment displays as well as eight status LED's. The high current requirement is

fulfilled by the use of 16 driver transistors. The return lines RL0-RL7 are connected to the key matrix. The cathodes of the 7 segment displays as well as eight status LED's are driven in parallel by eight transistors controlled by the eight output lines A0-A3 and B0-B3 of the 8279. The leftmost digit is driven by the output O0 of 74LS138 while the successive digits are driven by other outputs of this decoder and the next one. The output O7 of the second 74LS138 controls the eight status LED's. As shown in the memory map the keyboard controller IC is located at 1800h. The register select line A0 of the 8279 is connected to the address line A8 and therefore the command/status register is mapped at 1900h and the data register at 1800h.

2.3 DATA CONVERSION AND TAPE INTERFACE

The circuit diagram of the data pcb has been given in the fig.4. One D/A converter type AD7533 has been connected to the port A of 8155 to generate the analog output corresponding to the digital input. The conversion of the input analog signal into digital form is accomplished by comparing the same to the output of the D/A converter referred above, in a comparator type LM311, and testing the output of the latter at port line PB0 of the 8155. The successive approximation algorithm has been implemented in software. The two output lines of the port C of 8155 have been used for multiplexing four analog inputs into one and also demultiplexing output of the D/A convertor into four

lines. A dual four to one multiplexer/demultiplexer type CD4052 has been used for this purpose. It is operated at +5 volts and can therefore handle signals of 0-5 volt range. The third line of 8155 is used for enabling the S/H circuit realised by four sections of the quad op-amp type LM324. The input lines have been buffered by another LM324 and protected by a set of diode clamps.

The cassette tape recorder interface includes data write as well as data read interface. The data write interface has been realised by a pair of JK flip-flops of CD4027, one binary counter type CD4040 and a few gates. The USART 8251 has been programmed to operate in X16 clock mode. Accordingly the counter chain of 8253 is also initialised to generate 76800 Hz clock to get a data rate of 4800 from 8251. The dividing factors of the counter in 8155 as well as those of 8253 have been given in fig .1. The X16 clock of 76800 Hz also drives a counter type CD4040 to generate X2 clock. The set input of the first JK flip-flop is driven by the serial data line of 8251 and its J and K inputs are held at logical ONE. The X2 clock is connected to the clock input of the JK flip-flop and therefore Q output of the latter remains at state ONE for logical ONE output from 8251 and toggles at every positive transition of the clock if the output of 8251 is logical ZERO. The Q output of the first JK FF drives the J&K inputs of the second JK FF, the clock of which is also two times the bit rate. The output of the second JK FF is

the required Biphase-Mark signal. It is attenuated and shaped in a R-C network to limit its upper end of frequency spectrum. Biphase-Mark coding is especially suitable for use in tape recorder applications as it is not affected by the signal inversion in record reproduce electronics internal to the cassette tape recorder. Biphase-Mark is characterised by two zero crossings for one bit period for logical ONE and only one for logical ZERO. The waveforms have been given in fig.5. This scheme has been described in detail in Ref.7.

Coming to the data recovery, it is necessary to point out that the phase shifts inherent in the record reproduce process have no effect on so far as audio applications are concerned, however, the phase equalisation is needed for proper decoding of the recorded waveform. This has been accomplished in the circuit by an op-amp type 741 or a section of 324. The output of the phase equaliser in turn drives a zero crossing detector implemented by a comparator LM311 to generate a nearly square wave. The rising and falling edges of this signal are made to produce narrow pulses of about 5 microsecond width with the help of an XOR gate CD4030. Time period between these pulses gives estimate of ONE and ZERO in the recorded data. Pulses separated by about one bit period represent ZERO and two pulses separated by half bit period indicate logical ONE. This signal can be decoded by hardware using phase lock loop as explained in Ref.7, or else software technique can be used to decipher data. The

latter has been utilized in the present system to reduce hardware.

Some of the cassette tape recorders require isolated or floating contacts for the operation of the Remote function. A pcb type relay has therefore been used for the purpose. It is driven by a transistor which in turn is controlled by port line PC3 of 8155.

2.4 POWER SUPPLY I

Power supply is of straight forward design and needs no special treatment. The circuit diagram of the power supply has been given in fig 7. An alternative power supply with provision for battery backup has also been designed.

2.5 POWER SUPPLY II

The instrument draws about one ampere at 5 volts, 0.5 amperes at +12 Volts and 0.1 amperes at -12 Volts. Previous models of the instrument derived this power from a linear regulator standard power supply energised by 230 V AC power source (power supply I). The instrument requires initialization at every power on sequence and therefore frequent power failures defeat the very purpose of unattended operation. A power supply system normally running on 230 V ac power source and switching over to

12V lead acid car battery has therefore been designed. A raw dc of +15 Volts is generated from 230 V ac, which in turn drives a switched mode power supply through a power diode OR gate. The battery is normally kept at trickle charge at C/1000 rate and supplies power during power failures. A battery of 10 Ah capacity can run the instrument for about ten hours. The SMPS is based on the design described in Ref. 8. It uses SG3524 IC as control element and utilizes a transformer wound on the U-core of the horizontal deflection transformer of 12/14 in. TV. It generates +12V, -12V and +5V, out of which +5V is regulated through feedback. 12V supplies, both positive as well as negative, have only about 2 percent regulation, which is however sufficient for the various circuits. The SMPS is adequately shielded by enclosing it in an aluminium box to reduce the interference to the other circuits. The circuit diagram of the power supply II has been given in Fig. 8.

2.6 CONSIDERATIONS FOR THE CASSETTE TAPE RECORDER

Virtually any model of standard monophonic audio cassette tape recorder can be used with the present system. However a separate tape recorder requires extensive cabling apart from power connection which adds to the confusion. One of the models of the instrument have therefore been designed to include a built in tape recorder. Car cassette player mechanisms are fairly compact

and can easily be converted into a mono recorder by adding erase head and replacing the read/write head by mono one. The car cassette deck has only one lever for tape forward and reverse motion as well as eject function. The tape starts moving just after insertion of the cassette but REMO function can be implemented by stopping the motor. The record/reproduce switch has been installed on the tape pcb and is accessible from the outside. It is of the push button type having six poles and two way connections. The BEL1895 has been used for audio amplifier section. The circuit is of standard type and dc bias and dc erase has been used (Ref. 9 and 10).

2.7 OPERATION AND SOFTWARE DETAILS

The first 4K bytes of memory is earmarked for the monitor program. It is updated version of the one included in the SDK-85 kit and can be used in the similar way. It is used for entry of date, time and station code as well as data read and debugging purposes. The operational software of the instrument is located at 2800h-2FFFh and it is to be copied into the 1000h-17FFh area of RAM prior to use. This can be conveniently done with the help of program located at 3C80h. The memory buffer of 16K bytes has been split in to two parts of 8K each located at 4000h and 6000h. These are designated as buffer I and buffer II respectively. While one of the buffers is used for storage of data being currently acquired, the other one is used for transferring the data acquired in the previous cycle, to the cassette. The data collection rate totals to 20

samples per second for all the four channels which may be distributed to realise two channels of 10 per sec rate ,four channels of 5 per sec rate or just a single channel of 20 per second.Data is stored in the buffer in the sequence of channels 1,2,3,4.

First 16 bytes of each of the buffers constitute the identification information which includes time of acquiring the present data and station code and the rest of the memory of this block contains the collected data. The order of the identification bytes has been given in the appendix G .The recording rate is 4800 bits per second and therefore 8k bytes of data would require only about 20 seconds to record on to cassette.A leader consisting of continuous 4800 Hz is recorded for two seconds after the tape is set in motion .A sequence of 128 ZERO's and 128 ONES is recorded after this tone for synchronization purposes.It is followed by a sync byte A5 ,two bytes of byte count and a blank.The data is recorded after this leader.The checksum of the data is recorded in the last byte which is followed by 128 ZERO's and 128 ONES's once again.The tape is stopped after recording a small length of tape containing 4800 Hz tone.Thus the tape recorder runs for about 25 seconds with a gap of 400 seconds.Thus a C-60 cassette would last for about 8 hours per side.The C-90 cassette can also be used to increase the time but as the tape is thinner ,it is more likely to get stuck.

The software consists of the following modules:

2.7.1. Initialization; It loads the various addresses in different pointers, initializes the I/O devices, displays time and enables interrupts to start data collection operation. The clock starts ticking and thus confirms the operation of the system. The multiplexer control LED's also flicker. The flow chart of this module along with that of the A/D converter has been given in the appendix A. The interrupt line RST7.5 is used for all the operations, clock update, display update as well as data acquisition. The interrupt vector is modified by each of the software modules to point to the next module, to enable the operation of the following module at the occurrence of the next interrupt.

2.7.2. Clock module; It updates the current time at the 60 pps time base generated in the timer chain. The time is stored in the RAM as well as displayed on the seven segment displays. Clock is of 24 hour type and day of the year is counted upto 3 digits. Year is not updated as it is not needed. The flow chart of the clock and display modules have been given in the appendix B. The interrupt vector is altered to point to the display module at the end of this subroutine.

2.7.3. Display module; This module updates the display on receipt of the interrupt. The 60 pps pulse referred above is used to interrupt the microprocessor. The clock update, display update and the data acquisition procedure take place on the occurrence of interrupt sequentially. Thus

each of these operations take place 20 times per second. The display subroutine modifies the interrupt vector to point to the data acquisition module.

2.7.4. Data conversion; This subroutine is the basic one for this system. It stores one byte of data in RAM, advances channel count, converts the analog signal to digital by successive approximation method and updates various pointers. It also checks for buffer full to initiate recording process and switchover the buffers. Data recording is a simple affair, data is presented to the USART 8251 byte by byte in software loop, which serialises and sends it to tape write electronics.

As it has been mentioned earlier, only the RST7.5 interrupt line has been used for the system. As there is ample time between interrupts, data acquisition and recording can take place simultaneously.

2.7.5. Data read or verify; The data read operation has been realised by software. The data read operation is usually performed after data collection and hence microprocessor can be made use of for this purpose. The recorded data from the tape is fed to an edge detector which generates an interrupt signal. This signal is routed to RST7.5 by means of a logic gate under software control. A software counter provides the count between each edge which is read through interrupt subroutine. The counter is driven by a 300 Khz pulse train, which in turn is taken from the output of the 8155 timer's terminal. The interrupt subroutine reads the counter and again resets

and restarts the counter. A hardware counter implemented in 8253 with interrupt was used because software counters using timing loops could provide very small counts for such a fast data rate. The decision level therefore could not be precisely fixed, resulting in poor reliability of the decoder. With a dedicated counter and high frequency clock, the tolerance on the decision level became sufficiently high to enable error free decoding. The decoding scheme has been shown in appendix E with the help of a flow chart. It decodes longer intervals between pulses as ZERO and two pulses of smaller interval as ONE. This method could even be used for a data rate of 7200 bps with success.

3.0 CONCLUSION

A four channel data recording system utilizing the standard audio cassette medium has been designed. It has been successfully used for the recording of Ionospheric Scintillations at PRL Ahmedabad and Department of Physics, Saurashtra university, Rajkot. It can easily be used to record any other information. Marginal software changes can be made in the software to increase the recording time at the cost of channel bandwidth. It would prove to be quite convenient for unattended data gathering.

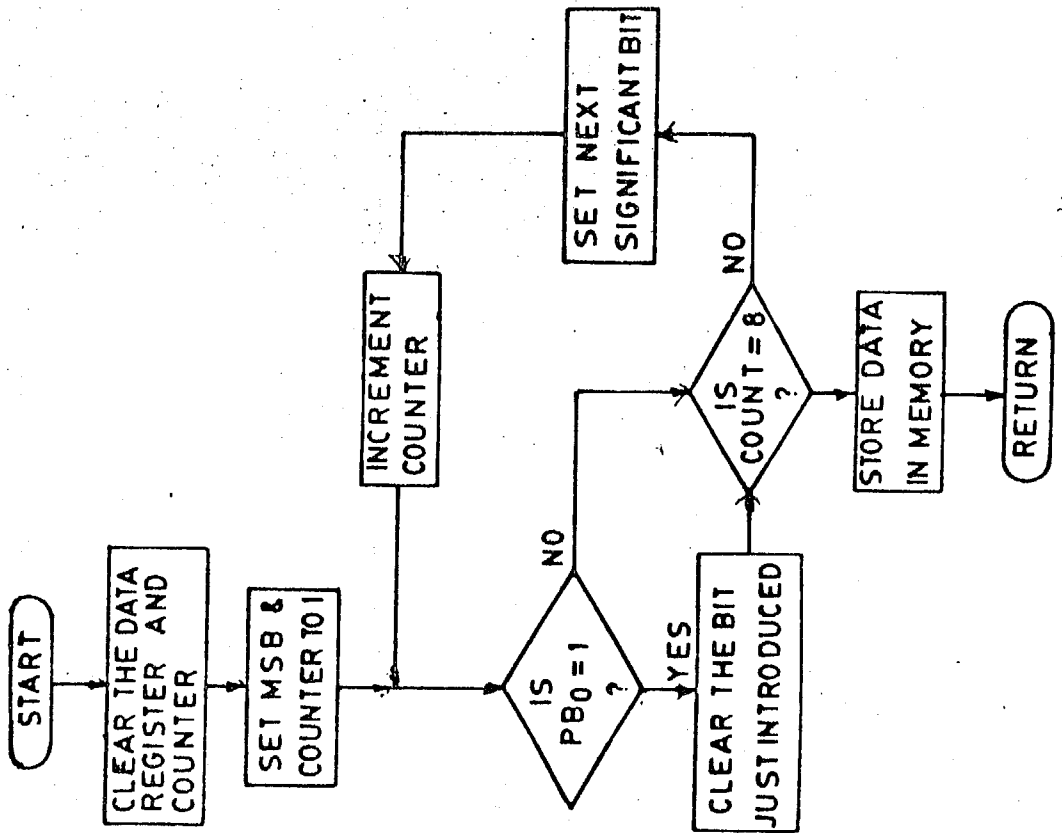
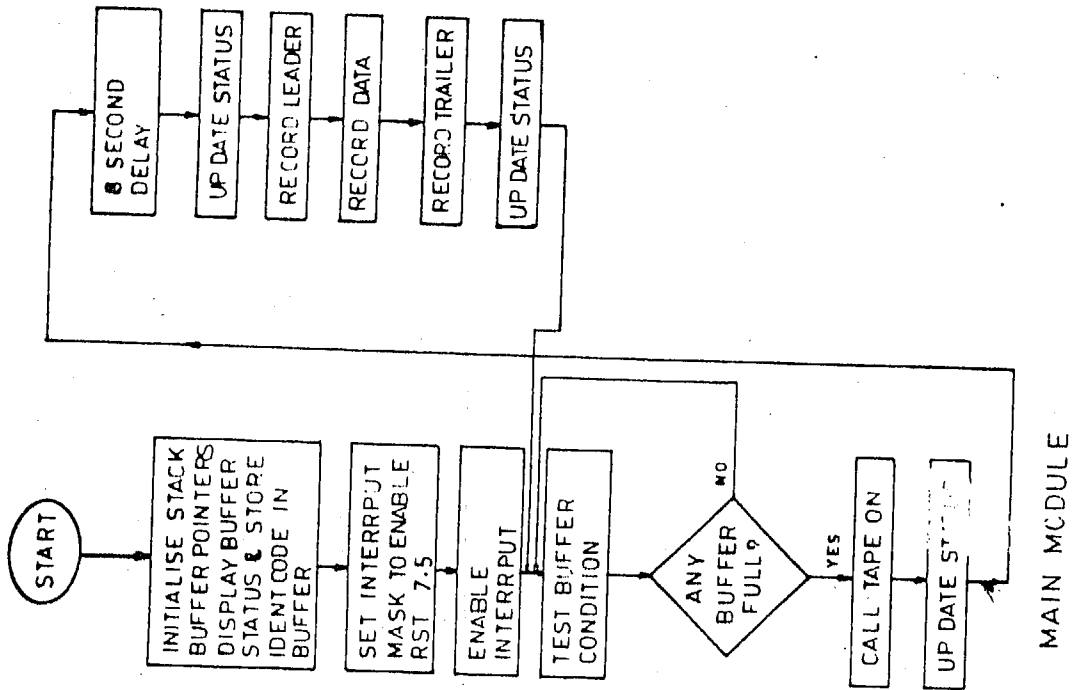
ACKNOWLEDGEMENTS

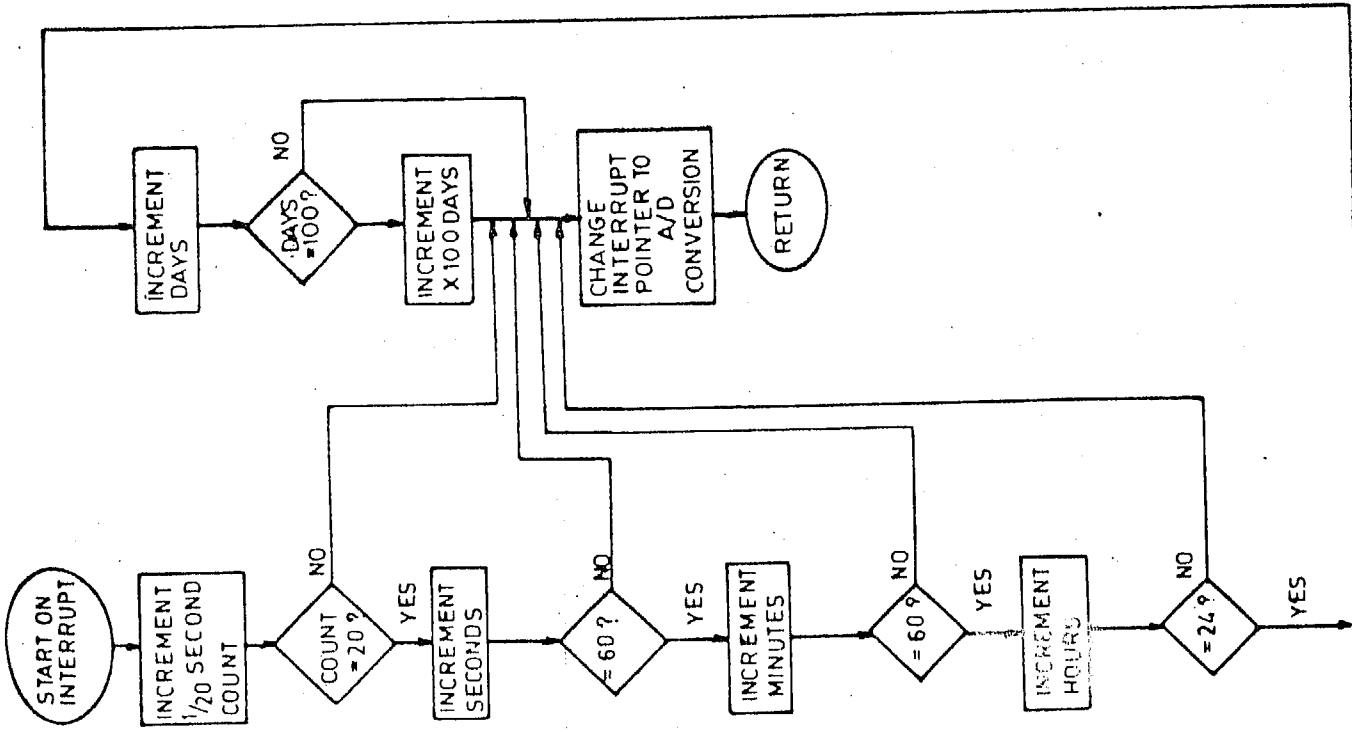
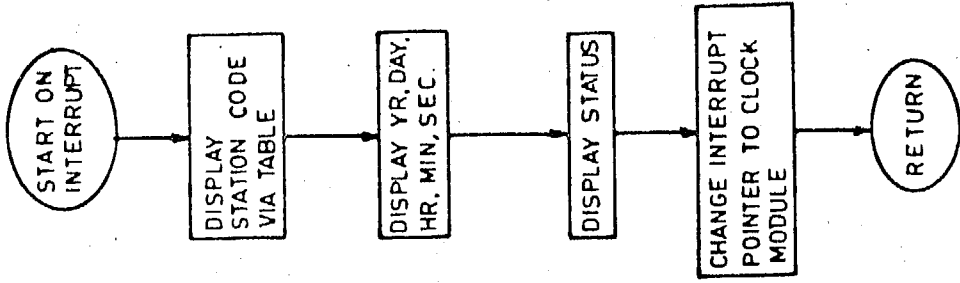
This instrument is the upgraded version of the Ionospheric Scintillation Recorder designed by the author earlier and described in Ref.2 .The hardware and software refinements were implemented by Mr.Akhilesh Kumar during his tenure at PRL during 1988-89.Messrs. M.B.Dadhania,R.I.Patel,and Mr.Dineh Patel of A.V.P.T. Rajkot contributed toward the design and fabrication of SMPS and Tape Recorder electronics.Mr.H.D.Parikh did all the electronic assembly of the instrument and the diagrams included in the document were drawn by Mr.G.A.Panchal.The instrument was designed at the suggestion of Dr.Harish Chandra and Dr.G.D.Vyas took all the pains to check the proper operation in field.Facilities provided by Prof.K.N.Iyer of the Department of Physics ,Saurashtra University ,Rajkot during the field trial of this instrument and help made available during that period from his colleagues is thankfully acknowledged.

REFERENCES

1. A LOW COST TOUCH KEYBOARD CRT TERMINAL, R. N. Misra and I. T. Kripalani, PRL Technical note TN-86-53, March 1986.
2. A MICROPROCESSOR BASED IONOSPHERIC SCINTILLATION DATA RECORDER, R. N. Misra and M. B. Dadhanian, PRL Technical Note TN-86-56, October 1986.
3. MCS-80/85 Family users manual, 1972, Intel Corporation, 3065 Bowers Avenue Santa Clara, California 95051, USA.
4. SDK-85 System Design Kit users manual, 1978, Intel Corporation, 3065 Bowers Avenue, Santa Clara, California 95051, USA.
5. Components Data Catalog 1980, Intel Corpn.
6. Data Acquisition Components and Subsystems 1980, Analog Devices, Route One Industrial Park, P.O. Box 280, Norwood, Massachusetts, 02062, USA.
7. Smith, P. and Zokoczy, P. I. 'DATA RECORDING ON AUDIO CASSETTE', Wireless World, Feb. 1982, pp50-52 and 62.
8. CONTROL IC's FOR SMPS APPLICATIONS, A. K. Maini, Electronics For You, November 1989, pp105-114.
9. DATA SHEET BEL 1895, Bharat Electronics Limited Bangalore.
10. RADIO CASSETTE RECORDER, S. Das Gupta, Electronics For You, April 1986, pp79-86

APPENDIX A





APPENDIX B

SEVEN SEGMENT ASCII DISPLAY CODES

1	2	3	4	1	2	3	4	1	2	3	4	1	2	3	4
20	00	BL	30	F3	0	□	40	35	□	50	37	P	P		
21	28	!	31	60	1		41	77	A	51	CD	Q	Q		
22	22	*	32	B5	2	□	42	C7	B	52	05	R	R		
23	00	#	33	F4	3	□	43	93	C	53	D6	S	S		
24	00	\$	34	66	4	□	44	ES	D	54	87	T	T		
25	00	%	35	D6	5	□	45	B7	E	55	E3	U	U		
26	00	&	36	D7	6	□	46	17	F	56	C1	V	V		
27	20	'	37	70	7	□	47	D3	G	57	C1	W	W		
28	93	(38	F7	8	□	48	47	H	58	25	X	X		
29	F0)	39	76	9	□	49	40	I	59	E6	Y	Y		
2A	00	*	3A	77	A	□	4A	E1	J	5A	B5	Z	Z		
2B	64	+	3B	C7	B	□	4B	67	K	5B	93	[[
2C	08	,	3C	93	C	□	4C	83	L	5C	46	\	\		
2D	04	-	3D	E5	D	□	4D	45	M	5D	F0]]		
2E	08	.	3E	B7	E	□	4E	75	N	5E	32	~	~		
2F	21	/	3F	17	F	□	4F	03	O	5F	80	'	'		

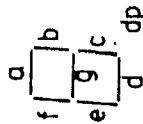
- 1. ASCII CODE
- 2. DISPLAY CODE
- 3. ASCII CHARACTER
- 4. DISPLAYED CHARACTER

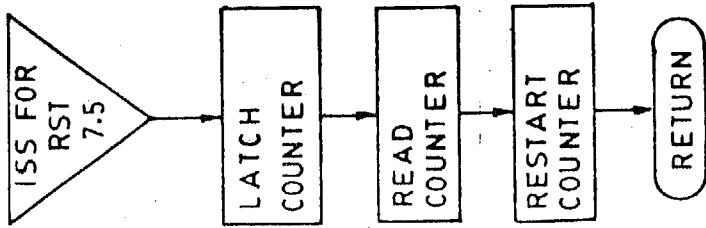
NOTE: INPUT CODES 3A TO 3F ARE USED FOR HEX [NON ASCII]

DISPLAY DATA FORMAT

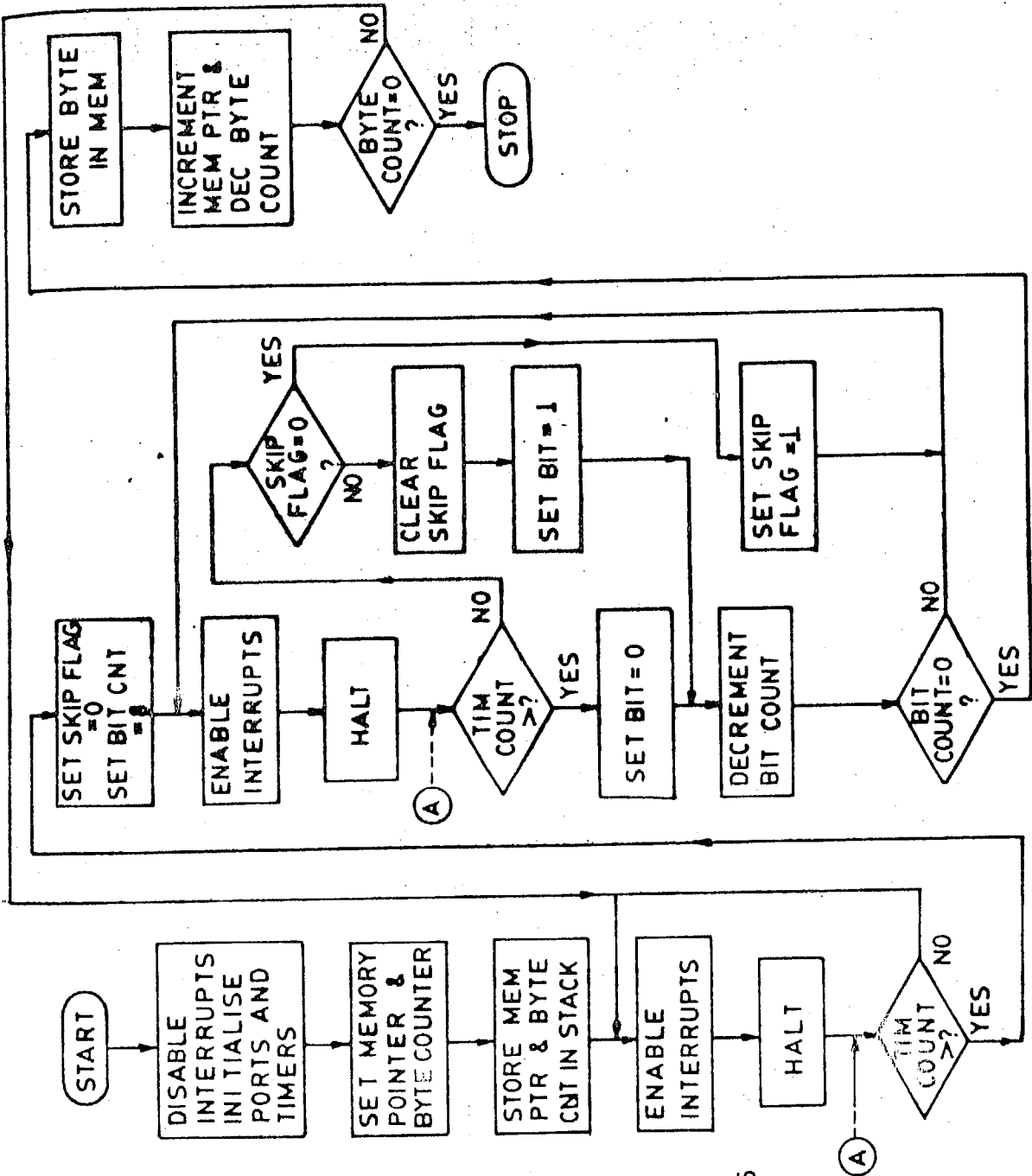
8279	DISPLAY	A3	A2	A1	A0	B3	B2	B1	B0
	RAM OUTPUTS								
	DATA BITS	D7	D6	D5	D4	D3	D2	D1	D0
	SEGMENTS	d	c	b	a	d.P.	g	f	e

'1' - LED is OFF
'0' - LED is ON





(A) ISS FOR RST 7.5 GIVES COUNT



APPENDIX F

STEP BY STEP OPERATION

Information regarding the current time ,and station code has to be initially loaded in the microprocessor memory starting from the address 20A2h. Seconds ,minutes,hours,units and tens of day of the year ,hundreds of the day of the year, a leading zero and lastly the last two digits of the year are stored in the RAM in this sequence.ASCII codes of the three prominent letters of the station name are entered after the year data.This information gets displayed on the seven segment displays after the program starts running.Clock is updated automatically by the program.All the information is lost on power down and initialisation needs to be done again all over.

Contents of Display RAM to be loaded at the start of the recording.

ADDRESS	CONTENTS
20A2H	SECONDS
20A3H	MINUTES
20A4H	HOURS
20A5H	UNITS AND TENS OF DAY OF THE YEAR
20A6H	HUNDREDS OF DAY OF THE YEAR WITH LEADING ZERO.
20A7H	YEAR
20A8H	ASCII 1, STATION CODE

20A9H

ASCII 2, STATION CODE

20AAH

ASCII 3, STATION CODE

After loading this information in RAM ,copy the program
by: GO 3C80.Now the instrument can start functioning by:
GO 12A0.

DATA READ AND TRANSFER TO PC

The read subroutine is located at 1400H.One block of
data can be read in the following way:

GO 3C80 ;copy the software in RAM

GO 1400 ;REWIND THE TAPE: PRESS PLAY BUTTON

Now one block of data will get stored in RAM at 4000-
5FFF and the header information i.e. time, station code
etc. would be displayed .The control returns to monitor
and more blocks can be read in the same way.

Transfer of a block of data to a floppy disk would
require insertion of DOS diskette in the PC ,followed by
terminal emulation software.As soon as terminal emulation
software takes control,the baud rate of the COMM port is
set to 1200 bps.Now the switch at the back of the
instrument labelled TTY/KBD is flipped over to TTY and
reset button pressed.The instrument responds by giving
Signon message on the PC screen.

Now the tape recorder is prepared for data read
operation ,tape is inserted and software copy as well as
data read commands given as explained before.For data
transfer to the PC, the program at 16C0 is used. GO 16C0
command is issued but the final CR is withheld.The file

transfer is initiated by specifying the drive number filename etc. For example

a: scint.dat would store the block under filename scint1.

Now the CR should be given to start data transfer. The data is simultaneously displayed on the screen. Data bytes are split in two ASCII characters and stored in ASCII form. End of data is indicated by signon message. The transfer operation can be terminated at this stage. More blocks may be read and transferred to floppy or hard disk in the same way.

APPENDIX G

Temporary Storage;

Stack	20A0
1/20 seconds	20A1
Seconds	20A2
Minutes	20A3
Hours	20A4
Days	20A5
Days*100	20A6
Year	20A7
Station code I	20A8
Station code II	20A9
Station code III	20AA
Optional	20AB
Data Pointer	20AC, 20AD (Number of bytes stored)
Memory Pointer	20AE, 20AF (Memory address where the new data is to be stored)
Status	20B3
Lowaddress of	20B4
Interrupt routine	

Header constitutes data from locations 20AB to 20A2 stored in reverse order followed by six 00's.

Memory Map;

0000-0FFF	Monitor
1000-17FF	Run Location for Recorder Program
1800-1FFF	Keyboard/Display

2000-20FF	8155 RAM
2800-37FF	Not used
3800-3FFF	Recorder Program in EPROM
4000-5FFF	Buffer I
6000-7FFF	Buffer II
8000-FFFF	Not used

I/O Map and port assignments;

00H	8251
08H	8253
counter 0,	/10
counter 1,	/2560 60 PPS:Rate
counter 2,	/2 76.8 Khz:Square wave
20H	8155
port A	D/A Converter
port B, PB0	Comparator, rest not used
port C:	
PC0	Channel select
PC1	Channel select, 4 inputs
PC2	Write/Read control, RST 7.5
PC3	Motor On, Cassette Recorder
PC4	MUX Enable
PC5	Free

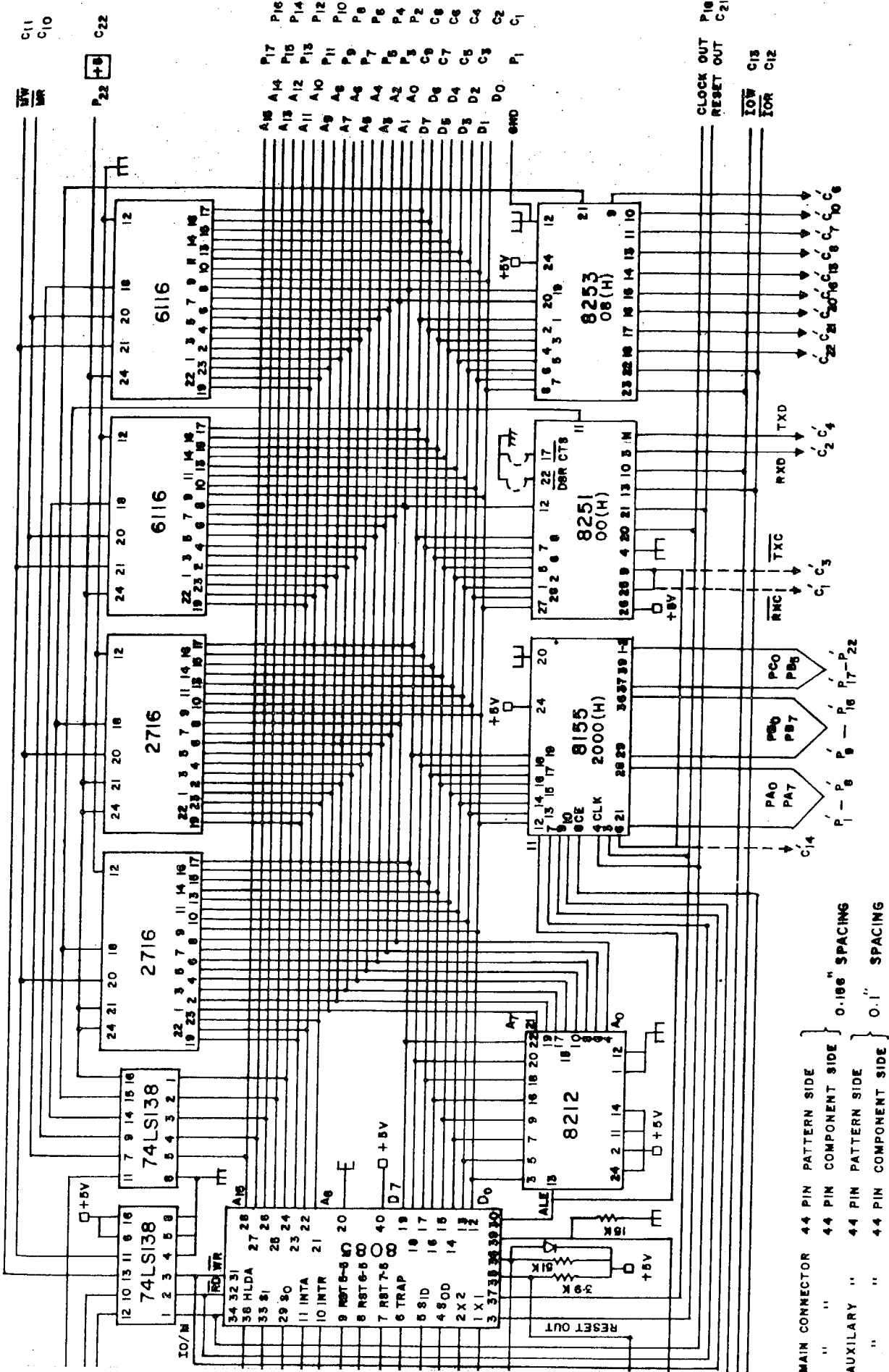
APPENDIX H

BIT Assignments of the STATUS byte

Bit 0/Bit 1	Channel select
Bit 2	Write Buffer A, 0 Empty, 1 Full
Bit 3	Write Buffer B, do
Bit 4	T/R Motor ON, 0 OFF, 1 ON
Bit 5	Data recording, 0 off, 1 on
Bit 6	Buffer A, 0 Empty, 1 Full
Bit 7	Buffer B, 0 Empty, 1 Full

STATUS LED'S

LSB							MSB
X	X	X	X	X	X	X	X
CHANNEL	WRITE	WRITE	T/R	DATA	BUFF A	BUFF B	
SELECT	BUFF A	BUFF B	MOTOR	REC	FULL	FULL	
			ON	ON			



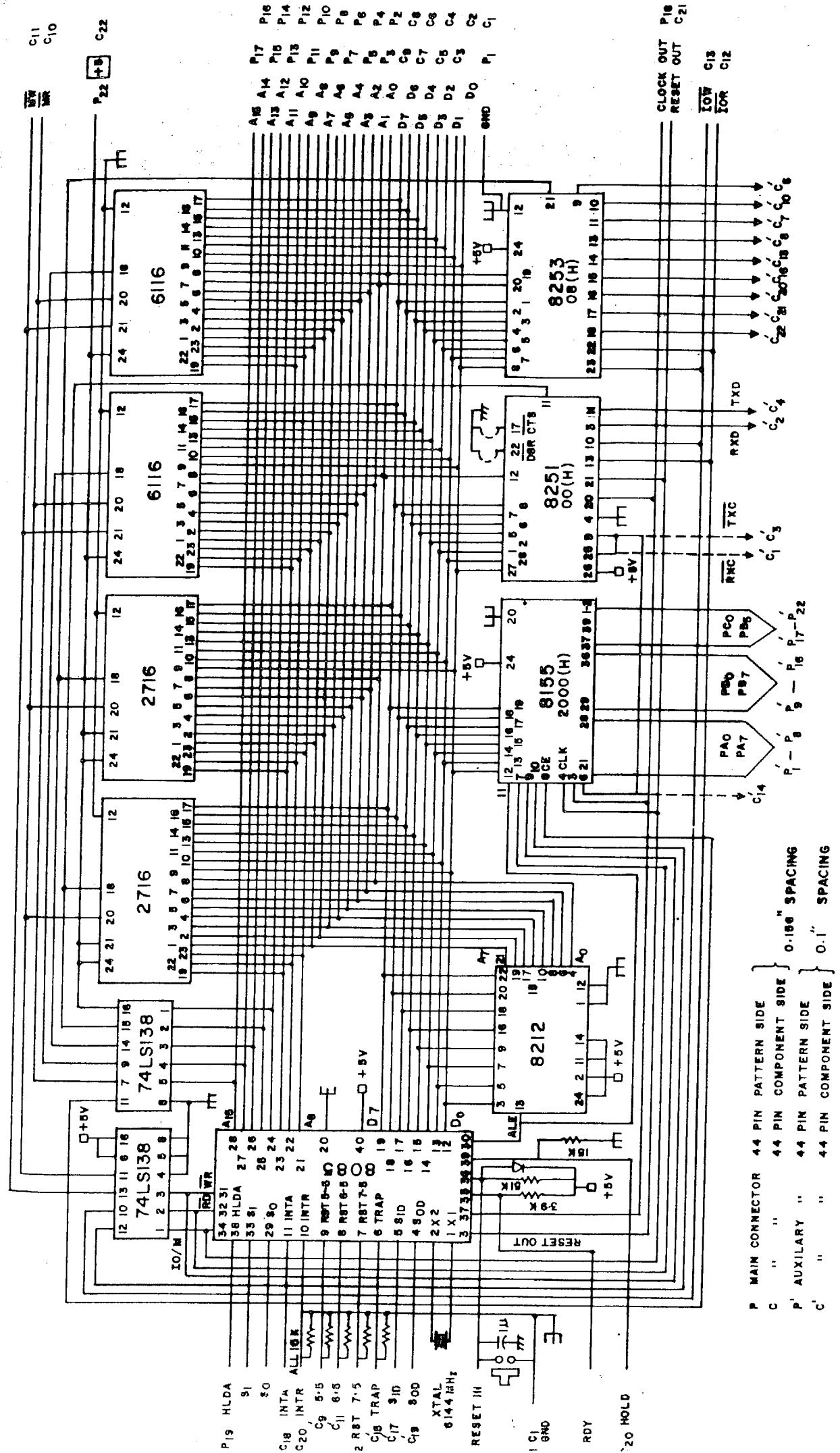
C11
C10
P22 +8
C22

P17 P16 P15 P14 P13 P12 P11 P10 P9 P8 P7 P6 P5 P4 P3 P2 P1
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D7 D6 D5 D4 D3 D2 D1 D0
GND

CLOCK OUT P18
RESET OUT C21
LOW FOR C13
FOR C12

MAIN CONNECTOR 44 PIN PATTERN SIDE } 0.106" SPACING
 " " 44 PIN COMPONENT SIDE }
 AUXILIARY " 44 PIN PATTERN SIDE } 0.1" SPACING
 " " 44 PIN COMPONENT SIDE }

8085 A BASED SINGLE CARD MICROCOMPUTER



C11
C10

P22 +5 C22

P16 P14 P12 P10 P8 P6 P4 P2 C8 C6 C4 C2 C1
P17 P15 P13 P11 P9 P7 P5 P3 P1
A15 A14 A13 A12 A11 A10 A9 A8 A7 A6 A5 A4 A3 A2 A1 A0
D7 D6 D5 D4 D3 D2 D1 D0
GND

CLOCK OUT P18
RESET OUT C21
LOW FOR C13
FOR C12

- P MAIN CONNECTOR 44 PIN PATTERN SIDE
- C " " 44 PIN COMPONENT SIDE } 0.156" SPACING
- P' AUXILIARY " " 44 PIN PATTERN SIDE
- C' " " 44 PIN COMPONENT SIDE } 0.1" SPACING

APPENDIX J

Addresses of important subroutines(hex)

1.Keyboard monitor	004E
2.Serial monitor	03FA
3.Time delay via DE	05F1
4.Byte write	1039/1560
5.Byte read	1050/15C0
6.Block write ,HL mem pointer,BC byte count	10B0
7.Leader/Trailer,128 00's& 128 FF's	10C0
8.Two second delay	10F8
9.Clock	1100
10.A/D converter calling location	1160
11.A/D converter subroutine	1650
12.Motor on	11E0
13.Motor off	11F0
14.Main program for recording	1210
15.RST 7.5 vector,A/D converter	1270
16. do ,clock	1280
17. do ,display	1290
18.Entry point for main program	12A0
19.Copy header	12DE
20.RST 7.5 ISS header	12FB
21.Disply packed BCD	1300
22.Split nibble	131C
23.Display alphanumeric	1340
24.Initialize ports and timers	1360

25. Start record mode	1391
26. Start read mode	1398
27. Main call for initialisation	13A0
28. Code table for alphanumeric data for display on seven segment LED's	13C0-13FF
29. Read one block	1400/1600
30. Copy header ,used by read	1450
31. Copy self to 1000 ,runs at 3C80	1480
32. Write sync and byte count, called by record	14A0
33. Loop FF	14C0
34. Checksum generation in Accumulator	14E0
35. Start recording	1500
36. Initialise 8251	1530
37. Wait char used by 8251	1560
38. Initialise for read	1570
39. RST 7.5 ISS location for read operation	15A0
40. Byte read	15C0
41. Block read and display	1600
42. A/D converter	1650
43. Test D/A converter, generate ramp	1680
44. Test count between pulses in read mode data stored at 4000, 2000 values	1690
45. Data Transfer Program	16C0

APPENDIX K
SYSTEM SPECIFICATIONS

1.No. of channels	one to four
2.Input range	0-5 Volts
3.Sampling rate (total)	20 per sec
4.Data recording medium	3.8 mm tape (audio cassette)
5.Recording density	230 char per in
6.Tape speed	47.6 mm per sec
7.Number of tracks	one per side
8.Interrecord gap	95 mm approx
9.Recording mode and format	1 start bit , 8 bit serial data, LSB first,1 stop bit , no parity
10.Recording rate	4800 bps
11.Data block size	8096 bytes
12,Data volume on one C-60 cassette	1.5 Mbytes
13.Power source	230V AC/12V Battery
14.Power consumption	15 Watts
15.Size WXD _X H (mm)	305X380X76
16.Weight (excluding tape recorder)	3.3 Kg.

Note: The recording rate may be reduced to 2400 bps to reduce the number of errors. In that case the volume of data on C-60 cassette also drops to 800 Kbytes. It would require the following changes in the software:

address,1364	3E08;divide by 8 to get 38.4 KHz
15C5	3E56;detection threshold for 1
15D3	3E56;or 0

APPENDIX L

PROGRAM LISTING

```

1039 C38015 JMP 1500 ;BYTE WRITE
1050 C3C015 JMP 15C0 ;BYTE READ

WRITE BYTE IN E REG REPEAT AS IN D REG

10A0 1680 MVI D,80 ;128 TIMES
10A2 4B MOV C,E ;WRITE VIA C REG
10A3 D5 PUSH D
10A4 CD3910 CALL 1039 ;BYTE WRITE FROM C REG
10A7 D1 POP D
10A8 15 DCR D
10A9 C2A210 JNZ 10A2 ;WRITE ALL BYTES
10AC C9 RET

BLOCK WRITE, HL MEM POINTER, BC BYTE COUNT

10B0 C5 PUSH B
10B1 4E MOV C,M
10B2 CD3910 CALL 1039 ;CALL BYTE WRITE
10B5 23 INX H
10B6 C1 POP B
10B7 0B DCX B
10B8 78 MOV A,B
10B9 B1 ORA C
10BA C2B010 JNZ 10B0 ;REPEAT TILL
10BD C9 RET

RECORD LEADER, 128 00'S AND 128 FF'S

10C0 C5 PUSH B
10C1 1E00 MVI E,00 ;00, 128 TIMES
10C3 CDA010 CALL 10A0
10C6 1EFF MVI E,FF ;THEN FF ALSO
10C8 CDA010 CALL 10A0
10CB C1 POP B
10CC C9 RET

8 SECOND DELAY VIA DOUBLE LOOP

D5 D5 PUSH D
111000 LXI D,0010 ;OUTER COUNT LOOP
D5 D5 PUSH D
11FFFF LXI D,FFFF ;INNER COUNT LOOP
1308 CDF105 CALL 05F1 ;MONITOR UTILITY
130C D1 POP D
130D 1B DCX D
130E 7A MOV A,D
130F B3 ORA E
1310 C2D410 JNZ 10D4 ;OUTER LOOP
1311 D1 POP D

10E0 10A3 LDA 20B3 ;STATUS BYTE
10E1 F800 ORI 80 ;BIT 7=1
10E2 32B320 STA 20B3 ;STORE BACK
10E3 11F01F LXI D,1FF0 ;BYTE COUNT 2000-10H
10E4 CDD012 CALL 12DB ;COPY STATION CODE TIME
10E5 C9 RET

BUFFER CHANGEOVER A TO B

3AB320 LDA 20B3 ;STATUS BYTE
F800 ORI 80 ;BIT 7=1
32B320 STA 20B3 ;STORE BACK
11F01F LXI D,1FF0 ;BYTE COUNT 2000-10H
CDD012 CALL 12DB ;COPY STATION CODE TIME
C9 RET

2 SECONDS DELAY

D5 D5 PUSH D
110400 LXI D,0004 ;REST IS PART OF 8 SEC
C3D410 JMP 10D4

CLOCK SUBROUTINE

21A020 LXI H,20A0
CD2511 CALL 1125
FE20 CPI 20
C0 RNZ
CD2511 CALL 1125
FE60 CPI 60
C0 RNZ
FE60 CPI 60
C0 RNZ
FE24 CPI 24
C0 RNZ
CD2511 CALL 1125
FE24 CPI 24
C0 RNZ
CD2511 CALL 1125
K6FF ANI FF
C0 RNZ
CD2511 CALL 1125
C9 RET

LOAD ZERO AND ADVANCE MEM POINTER
USED BY CLOCK

3600 MVI H,00
1127 25 INX H
1128 34 INR M
1129 7E MOV A,M
112A 37 STC
112C 3F CMC
112D 27 DAA
112E 77 MOV H,A
C9 RET

DISPLAY SUBROUTINE

```

```

1186 JZ 10E4
1199 MVI B,40
119B LDA 20B3
119E F640
11A0 STA 20B3
11A3 LXI D,1FF0
11A6 CDDE12
11A9 RET

```

```

CAR410
2640
3AB320
F640
STA 20B3
LXI D,1FF0
CALL 12DB
RET

```

```

1186
1199
119B
119E
11A0
11A3
11A6
11A9

```

CHANNEL CHANGEOVER

```

PUSH B
LDA 20B3
MOV C,A
INR A
ANI 03
MOV B,A
MOV A,C
RECALL OLD STATUS
SUPPRESS LO 2
PUT NEW IN PLACE
NEW STATUS

```

```

C5
SAB320
4F
E603
47
79
K6FC
B0
32B320
C1
C9

```

```

11B0
11B1
11B4
11B5
11B6
11B8
11B9
11BC
11BD
11C0
11C1

```

MUX CONTROL

```

PUSH B
IN 23
ANI FC
MOV C,A
LDA 20B3
ANI 03
ORA C
OUT 23
POP B
RET

```

```

C5
DB23
E6FC
4F
3AB320
E603
B1
D323
C1
C8

```

```

11C3
11C4
11C6
11C8
11C9
11CE
11CF
11D1
11D2

```

START PULSE

```

IN 23
ORI 20
OUT 23
IN 23
ANI 1F
OUT 23
RET

```

```

11D3
11D5
11D7
11D9
11DB
11DD
11DE

```

MOTOR ON

```

IN 23
ORI 08
OUT 23
LDA 20B3
ORI 10

```

```

DB23
F608
D323
3AB320
F610

```

```

11E0
11E2
11E4
11E6
11E9

```

```

;STN CODE ASCII
;3 BYTES ASCII
;CODE 827
;CNTRL 8279
;CALL DISPLAY2
;NUMERIC DATA
;YEAR DAY ETC
;SIX BYTES
;CALL DISPLAY1
;STATUS,8 LED'S
;GET STATUS
;COMPLEMENT
;DISPLAY

```

```

PUSH H
PUSH B
PUSH PSW
LXI H,20A6
MVI B,03
MVI A,90
STA 1800
CALL 1340
MVI A,93
STA 1800
LXI H,20A7
MVI B,06
CALL 1300
MVI A,8F
STA 1900
LDA 20B3
CMA
STA 1800
POP PSW
POP B
POP H
RET

```

```

E5
C5
F5
21AB20
0603
3E90
320019
CD4013
3E93
320019
21A720
0606
CD0013
3E9F
320019
3AB320
2F
320018
F1
C1
E1
C8

```

A/D CONVERTER

```

;ENABLE MUX
;BYTE COUNT
;IN DE
;BUFFER ADDR IN HL
;CALL CONVERT
;ADVANCE MEM POINTER
;BYTE COUNT
;TEST COUNT
;JUMP IF
;BUFFER FULL
;ELSE STORE BACK
;COUNT AND MEM
;POINTER
;CHANNEL CHANGEOVER
;MUX CONTROL
;DISABLE MUX

```

```

LHLD 20AC
XCHG
LHLD 20AE
CALL 1650
INX H
DCX D
MOV A,D
ORA E
CZ 1183
SHLD 20AE
XCHG
SHLD 20AC
POP D
POP H
CALL 11B0
CALL 11C3
IN 23
ORI 10
OUT 23
RET

```

```

1160
1161
1162
1164
1166
1168
116C
116F
1172
1173
1174
1175
1176
1179
117C
117D
1180
1181
1182
1185
1188
118A
118C
118E

```

```

;H =60H ? IF YES

```

```

E5
D5
DB23
E6EF
D323
2AAC20
EB
2AAE20
CD5016
23
1B
7A
B3
C99311
22AE20
EB
22AC20
D1
E1
CDB011
CDC311
DB23
F610
D323
C8

```

```

1193
1194

```

BUFFER FULL

```

MOV A,H
CPI 60

```

```

7C
FE60

```

```

UPDATE AND DISPLAY MOTOR STATUS
3AB320 LDA 20B3 ;STATUS BYTE
E610 ANI 10 ;UPDATE
CA3011 JZ 1130 ;DISPLAY
C9 RET

```

MAIN PROGRAM FOR RECORDING

```

1200 1210 1211 1212 1213 1214 1215 1216 1217 1218 1219 1220 1221 1222 1223 1224 1225 1226 1227 1228 1229 1230 1231 1232 1233 1234 1235 1236 1237 1238 1239 1240 1241
3AB320 LDA 20B3 ;STATUS BYTE
F620 ORI 20 ;RECORDING ON
32B320 STA 20B3 ;STORE BACK
E604 ANI 04 ;TST BIT2
110020 LXI D,20000 ;BLOCK SIZE
CA2212 JZ 1222 ;BUF1 FULL THEN JMP
1000 MVI D,00 ;
210040 LXI H,4000 ;MEM POINTER
DAD D ;ADD DE FOR NEW ADDR
LXI B,20000 ;BYTE COUNT
CALL 1500 ;CALL RECORD BLOCK
3AB320 LDA 20B3 ;STATUS
E6DF ANI DF ;BIT 6=0
32B320 STA 20B3 ;STORE BACK
MOV A,H ;
CPI 60 ;H=60? HL =BUFF2
C24412 JNZ 1244 ;ELSE JUMP OVER
3AB320 LDA 20B3 ;STATUS
E673 ANI 73 ;BITS 0,1,5,6,7
F608 ORI 08 ;BIT 3 =1
C35012 JMP 1250 ;JUMPOVER

```

BUFFER 2IN USE

```

1244 1246 1249 124C 124E 1250 1253
FE80 CPI 80 ;H=80
C21106 JNZ 0611 ;IF NOT SHOW ERR
3AB320 LDA 20B3 ;STATUS BYTE
E6B3 ANI B3 ;BITS 0,1,4,5,7
F604 ORI 04 ;BIT 2=1
32B320 STA 20B3 ;STORE STATUS
C3C312 JMP 12C3 ;JUMP TEST BUFF
AND RECORD

```

RST 7.5 VECTOR ,A/D CONVERTER

```

1270 1273 1275 1278 1279 127A 127B 127C 127D
CD6011 CALL 1160 ;CALL A/D CONVERT
3E60 MVI A,60 ;LO ADDRESS FOR CLOCK
32B420 STA 20B4 ;STORED AT RST 7.5
F1 POP PSW ;VECTOR
E1 POP H
D1 POP D
C1 POP B
FB EI
C9 RET

```

```

11EB 32B320 STA 20B3
11EE C9 RET

```

MOTOR OFF

```

11F0 DB23 IN 23
11F2 E6F7 ANI F7
11F4 D323 OUT 23
11F6 3AB320 LDA 20B3
11F8 E6EF ANI EF
11FB 32B320 STA 20B3
11FE C9 RET

```

REPEAT ALL BYTES

C2CF12 JNZ 12CF
C9 RET

12D7
12DA

COPY HEADER

D5 PUSH D
C5 PUSH B
11AB20 LXI D,20AB
01000A LXT B,0A00
1A LDAX D
77 MOV M,A
23 INX H
1B DCX D
05 DCR B
C2E312 JNZ 12E3
3600 MVI M,00
23 INX H
0D DCR C
C2EB12 JNZ 12EB
C1 POP B
D1 POP D
C9 RET

12DB
12DC
12DD
12DE
12E0
12E3
12E4
12E5
12E6
12E7
12E8
12EB
12ED
12EE
12EF
12F2
12F3
12F4

RST 7.5 ISS HEADER

C5 PUSH B
D5 PUSH D
E5 PUSH H
F5 PUSH PSW
3AB420 LDA 20B4
6F MOV L,A
2612 MVI H,12
E9 PCHL

12F5
12F6
12F7
12F8
12F9
12FC
12FD
12FE
12FF

DISPLAY BCD PACKED IN ONE BYTE

0E02 MVI C,02
CD1C13 CALL 131C
E5 PUSH H
21F920 LXI H,20F9
7E MOV A,M
CD2D13 CALL 132D
320018 STA 1000
23 INX H
0D DCR C
C20913 JNZ 1309
E1 POP H
2B DCX H
05 DCR B
C20013 JNZ 1300
C8 RET

1300
1302
1305
1306
1309
130A
130D
1310
1311
1312
1315
1316
1317
1318
131B

RST 7.5 VECTOR FOR CLOCK

:CALL CLOCK SUBROUTINE
:LO ADDR FOR DISPLAY
:STORED AT RST 7.5
:VECTOR

CD0011 CALL 1100
3E90 MVI A,90
32B420 STA 20B4
F1 POP PSW
E1 POP H
D1 POP D
C1 POP B
FB EI
C9 RET

1280
1283
1285
1288
1289
128A
128B
128C
128D

RST 7.5 VECTOR FOR DISPLAY

:CALL DISPLAY
:LO ADDR FOR A/D
:STORED AT RST 7.5
:VECTOR

CD3011 CALL 1130
3E70 MVI A,70
32B420 STA 20B4
F1 POP PSW
E1 POP H
D1 POP D
C1 POP B
FB EI
C9 RET

1290
1293
1295
1298
1299
129A
129B
129C
129D

MAIN PROGRAM

LXI SP,20A0
LXI H,7004
SHLD 20B3
LXI H,1FF0
SHLD 20AC
CALL 13A0
MVI A,0B
SIH
MVI A,10
OUT 23
LXI H,4000
CALL 12DB
SHLD 20AE
EI
LDA 20B3
ANI C0
JZ 12C0
JMP 1210

31A020
210470
22B320
21F01F
22AC20
CDA013
3E0B
30
3E10
D323
210040
CDD112
22AE20
FB
3AB320
E00
CAC312
C31012

12A0
12A3
12A6
12A9
12AC
12AF
12B2
12B4
12B5
12B7
12B8
12BC
12BF
12C2
12C3
12C8
12C9
12CB

BLOCK WRITE, HL MEM POINTE
DE BYTE COUNTER

:DATA IN C
:BYTE WRITE
:NEXT LOC
:BYTE COUNT

4E MOV C,M
CD3810 CALL 1039
23 INX H
1B DCX D
7A MOV A,D
B3 ORA E

12CF
12D0
12D3
12D4
12D5
12D6

INITIALISATION OF PORTS AND TIMERS

```

3E3E MVI A, 3E
D30B OUT 0B
3E24 MVI A, 04
D308 OUT 08
3E20 MVI A, 00
D308 OUT 08
3E7C MVI A, 7C
D30B OUT 0B
3E20 MVI A, 00
D309 OUT 09
3E14 MVI A, 14
D309 OUT 09
3E2E MVI A, 2E
D30B OUT 0B
3E00 MVI A, 00
D30A OUT 0A
3E06 MVI A, 06
D30A OUT 0A
3E40 MVI A, 40
D325 OUT 25
3E0A MVI A, 0A
D324 OUT 24
3E0D MVI A, CD
D320 OUT 20
C9 RET
RECORD MODE

```

```

1360
1362
1364
1368
1369
136A
136E
1370
1372
1374
1378
137A
137C
137E
1380
1382
1384
1386
1388
138A
138C
138E
1390

```

```

;CNTR0,MODE3,LSB FIRST
;DIVIDE BY 4
;OUT PUT 76.8 KHZ
;CNTR1,MODE2,LSB FIRST
;DIVIDE BY 1400H,5120
;DECIMAL,OUTPUT 60 PPS
;CNTR2,MODE3
;DIVIDE BY 600H
;1536 DECIMAL:NOT USED
;CNTR 8155
;DIVIDE BY 10,LOAD MSB 00
;LSB OAH
;START
;BIT2 C PORT=0
;BIT2 C PORT=1

```

```

;CNTR0,MODE3,LSB FIRST
;DIVIDE BY 4
;OUT PUT 76.8 KHZ
;CNTR1,MODE2,LSB FIRST
;DIVIDE BY 1400H,5120
;DECIMAL,OUTPUT 60 PPS
;CNTR2,MODE3
;DIVIDE BY 600H
;1536 DECIMAL:NOT USED
;CNTR 8155
;DIVIDE BY 10,LOAD MSB 00
;LSB OAH
;START
;BIT2 C PORT=0
;BIT2 C PORT=1

```

```

;CNTR0,MODE3,LSB FIRST
;DIVIDE BY 4
;OUT PUT 76.8 KHZ
;CNTR1,MODE2,LSB FIRST
;DIVIDE BY 1400H,5120
;DECIMAL,OUTPUT 60 PPS
;CNTR2,MODE3
;DIVIDE BY 600H
;1536 DECIMAL:NOT USED
;CNTR 8155
;DIVIDE BY 10,LOAD MSB 00
;LSB OAH
;START
;BIT2 C PORT=0
;BIT2 C PORT=1

```

```

;CNTR0,MODE3,LSB FIRST
;DIVIDE BY 4
;OUT PUT 76.8 KHZ
;CNTR1,MODE2,LSB FIRST
;DIVIDE BY 1400H,5120
;DECIMAL,OUTPUT 60 PPS
;CNTR2,MODE3
;DIVIDE BY 600H
;1536 DECIMAL:NOT USED
;CNTR 8155
;DIVIDE BY 10,LOAD MSB 00
;LSB OAH
;START
;BIT2 C PORT=0
;BIT2 C PORT=1

```

```

;CNTR0,MODE3,LSB FIRST
;DIVIDE BY 4
;OUT PUT 76.8 KHZ
;CNTR1,MODE2,LSB FIRST
;DIVIDE BY 1400H,5120
;DECIMAL,OUTPUT 60 PPS
;CNTR2,MODE3
;DIVIDE BY 600H
;1536 DECIMAL:NOT USED
;CNTR 8155
;DIVIDE BY 10,LOAD MSB 00
;LSB OAH
;START
;BIT2 C PORT=0
;BIT2 C PORT=1

```

```

;GET BYTE
;THEN HI
;NIBBLE
;ONLY LO NIBBLE
;SAVE
;NEXT BYTE
;LO NIBBLE
;AT NEXT PLACE

```

```

1391
1393
1395
1397
1398
139A
139C
139E
13A0
13A3
13A6
13A8
13AB
13AE

```

```

;DATA IN E REG
;INIT D
;SAVE HL
;HL POINTS TO TABLE
;FOR DISPLAY ON 7 SEG
;GET TABLE ENTRY FOR
;ASCII CODE &
;COMPLEMENT
;DISPLAY REG
;NEXT CHAR
;COUNT CHAR
;DISPLAY ALL CHAR

```

```

;DATA IN E REG
;INIT D
;SAVE HL
;HL POINTS TO TABLE
;FOR DISPLAY ON 7 SEG
;GET TABLE ENTRY FOR
;ASCII CODE &
;COMPLEMENT
;DISPLAY REG
;NEXT CHAR
;COUNT CHAR
;DISPLAY ALL CHAR

```

```

;DATA IN E REG
;INIT D
;SAVE HL
;HL POINTS TO TABLE
;FOR DISPLAY ON 7 SEG
;GET TABLE ENTRY FOR
;ASCII CODE &
;COMPLEMENT
;DISPLAY REG
;NEXT CHAR
;COUNT CHAR
;DISPLAY ALL CHAR

```

```

;DATA IN E REG
;INIT D
;SAVE HL
;HL POINTS TO TABLE
;FOR DISPLAY ON 7 SEG
;GET TABLE ENTRY FOR
;ASCII CODE &
;COMPLEMENT
;DISPLAY REG
;NEXT CHAR
;COUNT CHAR
;DISPLAY ALL CHAR

```

```

;DATA IN E REG
;INIT D
;SAVE HL
;HL POINTS TO TABLE
;FOR DISPLAY ON 7 SEG
;GET TABLE ENTRY FOR
;ASCII CODE &
;COMPLEMENT
;DISPLAY REG
;NEXT CHAR
;COUNT CHAR
;DISPLAY ALL CHAR

```

CODE TABLE TO DISPLAY ALPHANUMERIC DATA ON
7 SEGMENT DISPLAYS

1300 00 28 22 00 00 00 20 93 F0 00 04 08 04 08 21
 1305 F3 00 B5 F4 66 D6 D7 70 F7 76 77 C7 93 E5 B7 17
 1310 35 77 C7 93 E5 97 17 D3 47 40 E1 87 83 45 46 C5
 1315 37 CD 05 D8 87 E3 C1 C1 25 E6 B5 93 46 F0 32 80

READ SUBROUTINES

1400 C30016 JMP 1600 ;NEW READ AT 1600H

PART OF OLD RED PROGRAM, NOT USED

1403 CDA013 CALL 13A0
 1406 CDE011 CALL 11E0
 1409 CDF810 CALL 10F8
 140C 210030 LXI H,3000
 140F C5 PUSH B
 1410 CDC014 CALL 14C0
 1413 FEA5 CPI A5
 1415 CA2014 JZ 1420
 1418 CD5010 CALL 1050
 141B C31314 JMP 1413

141E 00 NOP
 141F 00 NOP
 1420 CD5010 CALL 1050
 1423 4F MOV C,A
 1424 C5 PUSH B
 1425 CD5010 CALL 1050
 1428 C1 POP B
 1429 47 MOV B,A
 142A C5 PUSH B
 142B CD5010 CALL 1050
 142E 77 MOV H,A
 142F 23 INX H
 1430 C1 POP B
 1431 0B DCX B
 1432 78 MOV A,B
 1433 B1 ORA C
 1434 C22014 JNZ 142A
 1437 CD5010 CALL 1050
 143A 32B020 STA 20B6
 143D CD0011 CALL 11F0
 1440 CD5014 CALL 1450
 1443 CD3011 CALL 1130
 1446 CF RST 1

COPY HEADER

1450 C5 PUSH B

1451 210040 LXI H,4000 ;MEM POINTER
 1454 11AB20 LXI D,20AB ;HEADER DESTINATION
 1457 060A MVI B,0A ;BYTE COUNT
 1459 7E MOV A,M ;MOVE BYTE FROM MEM
 145A 12 STAX D ;VIA HL TO DE
 145B 23 INX H
 145C 1B DCX D
 145D 05 DCX B
 145E C26914 JNZ 1459 ;TILL 10 BYTES OVER
 1461 C1 POP B
 1462 C9 RET

READ BLOCK, NOT USED

1470 C5 PUSH B
 1471 CD6010 CALL 1050
 1474 77 MOV H,A
 1475 23 INX H
 1476 00 NOP
 1477 C1 POP B
 1478 0B DCX B
 1479 78 MOV A,B
 147A B1 ORA C
 147B C27020 JNZ 2070
 147E C9 RET

COPY PROGRAM TO 1000H, IT WORKS AT 3080H

1480 31A020 LXI SP,20A0 ;INIT STACK
 1483 210038 LXI H,3000 ;SOURCE START
 1486 110010 LXI D,1000 ;DESTINATION
 1489 01FF07 LXI B,07FF ;BYTE COUNT
 148C 7E MOV A,M ;MOVE
 148D 12 STAX D ;DATA TO NEW LOC
 148E 23 INX D
 148F 13 INX H
 1490 0B DCX B
 1491 78 MOV A,B
 1492 B1 ORA C
 1493 C28C3C JNZ 803C ;FOR ALL BYTES
 1496 CF EST 1 ;JUMP TO MONITOR

WRITE SYNC BYTE AND BYTE COUNT

14A0 C5 PUSH B
 14A1 0EA5 MVI C,A5 ;SYNC BYTE=A5H
 14A3 CD3910 CALL 1039 ;BYTE WRITE
 14A6 C1 POP B
 14A7 C5 PUSH B
 14A8 CD3910 CALL 1039 ;DATA IN BC IS BYTE
 14AB C1 POP B ;COUNT;WRITE IT
 14AC 78 MOV A,B ;C FIRST THEN
 14AD C5 PUSH B ;B

```

14AE MOV C,A
14AF CALL 1039
14B2 POP B
14B3 RET

14C0 LOOP FF,WAIT FOR 32 FF'S
14C1 PUSH D
14C2 MVI D,20
14C3 PUSH D
14C4 CALL 1050
14C7 POP D
14C8 CPI FF
14CA JNZ 14C1
14CD DCR D
14CE JNZ 14C3
14D1 CALL 1050
14D4 CPI FF
14D6 JZ 14D1
14D9 POP D
14DA RET

CHECKSUM
C5 PUSH B
D5 PUSH D
E5 PUSH H
1E00 MVI E,00
1E05 XRA A
1E06 MOV A,M
1E07 ADD E
1E08 MOV E,A
1E09 INX H
1E0A DCX B
1E0B MOV A,B
1E0C ORA C
1E0D JNZ 14E6
14F0 MOV A,E
14F1 POP H
14F2 POP D
14F3 POP B
14F4 RET

START RECORDING
CDE014 CALL 14E0
32B520 STA 20B5
E5 PUSH H
E6 PUSH D
C5 PUSH B
CDE011 CALL 11E0
-50C CDD010 CALL 10D0
150F CDC010 CALL 10C0
1512 POP B

MOV C,A
CALL 1039
POP B
RET

LOOP FF,WAIT FOR 32 FF'S
PUSH D
MVI D,20
PUSH D
CALL 1050
POP D
CPI FF
JNZ 14C1
DCR D
JNZ 14C3
CALL 1050
CPI FF
JZ 14D1
POP D
RET

CHECKSUM
PUSH B
PUSH D
PUSH H
MVI E,00
XRA A
MOV A,M
ADD E
MOV E,A
INX H
DCX B
MOV A,B
ORA C
JNZ 14E6
MOV A,E
POP H
POP D
POP B
RET

START RECORDING
CALL 14E0
STA 20B5
PUSH H
PUSH D
PUSH B
CALL 11E0
CALL 10D0
CALL 10C0
POP B

CALL 14A0
POP D
POP H
CALL 10B0
LDA 20B5
MOV C,A
CALL 1039
CALL 10C0
CALL 11F0
RET
INITIALISE 8251
XRA A
OUT 01
OUT 01
OUT 01
MVI A,40
OUT 01
MVI A,4E
OUT 01
MVI A,11
OUT 01
IN 23
ORI 04
D323 OUT 23
21CE20 LXI H,20CE
36C3 MVI H,C3
23 INX H
36F5 MVI H,F5
23 INX H
3612 MVI H,12
C9 RET

WAIT FOR CHAR TO OUTPUT
DB01 IN 01
E601 ANI 01
CA6015 JZ 1580
79 MOV A,C
D300 MOV A,0
C9 RET

INITIALISATION FOR READ MODE
3K10 MVI A,10
D30B OUT 0B
3EFF MVI A,FF
D328 OUT 08
3E40 MVI A,40
D32F OUT 25
3E0A MVI A,0A
D324 OUT 24
3E08 MVI A,08
320018 STA 1800
3ECC MVI A,CC

WRITE SYNC A5 AND
BYTE COUNT
BLOCK WRITE
CHECKSUM
WRITE IT
BY BYTE WRITE
TRAILER
MOTOR OFF

CLEAR ACC
OUTPUT 00 3 TIMES
TO INIT 8251
RESET
MODE
CHANGE RECORD MODE

RST 7.5 VECTOR
RELOCATE TO
:12F5H

CNTR0,MODE0
LOAD FF IN LSB ONLY
:8155 CNTR
DIVIDE BY 10 AND PORT
INIT
INIT 8279
:6155 START

```

```

15E2 EI
15E3 D1
15E4 C1
15E5 C9
      POP H
      POP D
      POP B
      RET

      WAIT FOR ONE PULSE, CALLED FOR COUNTS
      LESS THAN THRESHOLD

3E00 MVI A,00 ;BIT IS ONE FOR
BB CMP K ;K=00
CAFC15 JZ 15FC ;THEN INCREMENT
1D DCE K ;ELSE DECREMENT E
37 STC ;CARRY=1
C3DA15 JMP 15DA ;JUMP BACK

```

```

15E2 EI
15E3 D1
15E4 C1
15E5 C9
      POP H
      POP D
      POP B
      RET

      WAIT FOR ONE PULSE, CALLED FOR COUNTS
      LESS THAN THRESHOLD

3E00 MVI A,00 ;BIT IS ONE FOR
BB CMP K ;K=00
CAFC15 JZ 15FC ;THEN INCREMENT
1D DCE K ;ELSE DECREMENT E
37 STC ;CARRY=1
C3DA15 JMP 15DA ;JUMP BACK

```

```

15FC 1C INR K
15FD C3D115 JMP 15D1
      DATA READ PROGRAM
      IT READS ONE BLOCK AND DISPLAYS
      HEADER ON DISPLAY
L1600 16AF
1600 F3 DI ;DISABLE INTERRUPTS
1601 31A020 LXI SP,20A0 ;STACK INIT
1604 CD7016 CALL 1570 ;INIT PORTS TIMERS
1607 CDE011 CALL 11E0 ;MOTOR ON
160A CDF810 CALL 10F8 ;DELAY 2 SECONDS
160D 3EFF MVI A,FF ;COUNT IN CNTR0
160F D308 OUT 08 ;MEM POINTER
1611 210040 LXI H,4000 ;LOOP FF
1614 C5 PUSH B ;SYNC FOUND
1615 CDC014 CALL 14C0 ;IF YES THEN JMPF
1618 FEAS CPI A5 ;ELSE READ ONE BYTE
161A CA2316 JZ 1623 ;TEST SYNC AGAIN
161D CDC015 CALL 15C0
1620 C31816 JMP 1618

```

```

1623 CDC015 CALL 15C0 ;BYTE READ
1626 4F MOV C,A ;SAVE IN C
1627 C5 PUSH B ;SAVE
1628 CDC015 CALL 15C0 ;READ NEXT
1629 C1 POP B
162A 47 MOV B,A ;THIS ONE IN B
162B C5 PUSH B ;BC HAS BYTE COUNT
162E CDC015 CALL 15C0 ;READ NEXT
1631 77 MOV M,A ;STORE IN MEMOET
1632 23 INX H
1633 C1 POP B
1634 08 DCX B
1635 78 MOV A,B

```

```

1623 CDC015 CALL 15C0 ;BYTE READ
1626 4F MOV C,A ;SAVE IN C
1627 C5 PUSH B ;SAVE
1628 CDC015 CALL 15C0 ;READ NEXT
1629 C1 POP B
162A 47 MOV B,A ;THIS ONE IN B
162B C5 PUSH B ;BC HAS BYTE COUNT
162E CDC015 CALL 15C0 ;READ NEXT
1631 77 MOV M,A ;STORE IN MEMOET
1632 23 INX H
1633 C1 POP B
1634 08 DCX B
1635 78 MOV A,B

```

```

1623 CDC015 CALL 15C0 ;BYTE READ
1626 4F MOV C,A ;SAVE IN C
1627 C5 PUSH B ;SAVE
1628 CDC015 CALL 15C0 ;READ NEXT
1629 C1 POP B
162A 47 MOV B,A ;THIS ONE IN B
162B C5 PUSH B ;BC HAS BYTE COUNT
162E CDC015 CALL 15C0 ;READ NEXT
1631 77 MOV M,A ;STORE IN MEMOET
1632 23 INX H
1633 C1 POP B
1634 08 DCX B
1635 78 MOV A,B

```

```

1623 CDC015 CALL 15C0 ;BYTE READ
1626 4F MOV C,A ;SAVE IN C
1627 C5 PUSH B ;SAVE
1628 CDC015 CALL 15C0 ;READ NEXT
1629 C1 POP B
162A 47 MOV B,A ;THIS ONE IN B
162B C5 PUSH B ;BC HAS BYTE COUNT
162E CDC015 CALL 15C0 ;READ NEXT
1631 77 MOV M,A ;STORE IN MEMOET
1632 23 INX H
1633 C1 POP B
1634 08 DCX B
1635 78 MOV A,B

```

```

1623 CDC015 CALL 15C0 ;BYTE READ
1626 4F MOV C,A ;SAVE IN C
1627 C5 PUSH B ;SAVE
1628 CDC015 CALL 15C0 ;READ NEXT
1629 C1 POP B
162A 47 MOV B,A ;THIS ONE IN B
162B C5 PUSH B ;BC HAS BYTE COUNT
162E CDC015 CALL 15C0 ;READ NEXT
1631 77 MOV M,A ;STORE IN MEMOET
1632 23 INX H
1633 C1 POP B
1634 08 DCX B
1635 78 MOV A,B

```

SERVICE ROUTINE RST 7.5, READ MODE

```

15A0 3E00 MVI A,00 ;LATCH CNTR0 AND READ
15A2 D30B OUT 0B
15A4 DB08 IN 08
15A6 2F CMA ;ITS CONTENTS
15A7 4F MOV C,A ;COMPLEMENT IT
15A8 3E10 MVI A,10 ;SAVE IN C
15AA D30B OUT 0B ;THEN INIT CNTR0
15AC 3EFF MVI A,FF ;AGAIN
15AE D308 OUT 08 ;LOAD FF TO DOWN COUNT
15B0 C9 RET

```

READ BITS AND COMPILER BYTE, BYTE READ
DATA RETURNED IN A REG

```

C5 PUSH B
D5 PUSH D
E5 PUSH H
EI
HLT

MVI A,28
CMP C
JNC 15C3
MVI E,00
MVI B,08
MVI D,00
EI
HLT

MVI A,28
CMP C
JNC 15C3
MVI E,00
MVI B,08
MVI D,00
EI
HLT

MVI A,28
CMP C
JNC 15F0
CMC
MOV A,D
RAR
MOV D,A
DCR B
JNZ 15D1
MOV A,D

```


HEXDUMP OF RECORDER PROGRAM

```

1000 DB 23 F8 08 D3 23 D5 16 13 15 C2 09 10 D1 DB 23
1010 E6 37 D3 23 C9 CD 00 10 D6 16 52 16 C2 1B 10 D1
1020 0F DB 22 17 DA 21 10 DB 22 17 D2 27 10 C9 79 17
1030 4F DC 15 10 CD 00 10 FB C9 C3 6E 15 21 10 F3 CD
1040 2E 10 05 C2 3B 10 CD 21 10 C8 FF FF FF FF FF
1050 C3 C0 15 00 16 00 14 DB 22 E6 4E C2 58 10 DB
1060 D2 E8 40 CA 5E 10 05 CA 78 10 7A FE 40 CD 88 10
1070 22 64 10 CD 90 10 C3 54 10 7A FE 40 CD 88 10
1080 85 10 CD 90 10 79 C9 FF F5 79 17 4F F1 C9 FF FF
1090 DB 22 E6 40 C2 90 10 DB 22 E6 4E CA 97 10 C9 FF
10A0 16 4B D5 CD 39 10 D1 15 C2 A2 10 C9 FF FF FF
10B0 C5 8E CD 39 10 C1 0B 78 B1 C2 B0 10 C9 FF FF
10C0 C5 1E 00 CD A6 10 1E FF CD A0 10 C1 C9 FF FF FF
10D0 D4 11 10 00 D5 11 FF FF CD F1 65 D1 1B 7A B3 C2
10E0 06 10 D1 C9 3A B3 20 F6 80 32 B3 20 11 F0 1F CD
10F0 DB 12 C9 FF FF FF FF D6 11 04 00 C3 D4 10 FF

1100 21 A0 20 CD 25 11 FE 20 C0 1D 25 11 FE 60 C0 CD
1110 25 11 FE 60 C0 CD 25 11 FE 24 00 CD 25 11 E8 FF
1120 C0 CD 25 11 C9 30 00 23 34 7E 37 3F 27 77 C9 FF
1130 E6 C5 F5 21 A8 20 06 03 3E 80 32 00 19 CD 40 13
1140 3E 83 32 00 19 21 A7 20 08 06 CD 00 19 3E 8F 32
1150 00 19 3A B3 20 2F 32 00 18 F1 C1 E1 C9 FF FF FF
1160 E5 D6 DB 23 E6 FF D3 23 2A AC 20 EB 2A AE 20 CD
1170 50 1E 23 1B 7A B3 CC 93 11 22 A8 20 EB 22 AC 20
1180 01 18 CD B0 11 CD C3 11 DB 23 F6 10 D3 23 C9 FF
1190 FF FF FF 7C FE 60 CA E4 10 26 40 3A B3 20 F6 40
11A0 92 B3 20 11 F0 1F CD DB 12 C9 FF FF FF FF FF
11B0 C5 3A B3 20 4F 3C E6 03 47 79 E6 FC B0 32 B3 20
11C0 C1 C9 FF C5 DB 23 E6 FC 4F 3A B3 20 E6 03 B1 D3
11D0 23 C1 C9 DB 23 F6 20 D3 23 DB 23 E6 1F D3 23 C9
11E0 DB 23 F6 08 D3 23 3A B3 20 F6 10 32 B3 20 C9 FF
11F0 DB 23 E6 F7 D3 23 3A B3 20 E6 FF 32 B3 20 C9 F7

1200 3A B3 20 E6 10 CA 30 11 C9 FF FF FF FF FF FF FF
1210 3A B3 20 F6 20 B3 20 E6 04 11 00 20 CA 22 12
1220 16 00 21 00 40 19 01 00 20 CD 00 15 3A B3 20 F6
230 DF 32 B3 20 7C FE 80 C2 44 12 3A B3 20 E6 73 E8
240 08 C3 60 12 FE 80 C2 11 06 3A B3 20 E6 B3 F6 04
250 32 B3 20 C3 C3 12 FF FF FF FF FF FF FF FF FF
260 3 FF FF FF FF FF FF FF FF FF FF FF FF FF FF
1270 CD 60 11 3E 80 32 B4 20 F1 E1 D1 C1 FB C9 FF FF
1280 CD 00 11 3E 80 32 B4 20 F1 E1 D1 C1 FB C9 FF FF
1290 CD 30 11 3E 70 32 B4 20 F1 E1 D1 C1 FB C9 FF FF
12A0 31 A0 20 21 04 70 22 B3 20 21 F0 1F 22 AC 20 CD
12B0 A0 13 0E 0B 30 10 D3 23 21 00 40 CD DB 12 22
12C0 AE 20 FB 3A B3 20 E6 C0 CA C3 12 C3 10 12 FF 4E
12D0 CD 39 10 23 1B 7A B3 C2 CF 12 C8 D6 C0
12E0 01 06 0A 1A 77 23 1B 05 C2 E3 12 36 00 23 0D C2
12F0 EB 12 C1 D1 C9 C5 D5 E5 F5 3A B4 20 6F 26 12 E8

```

1600 F3 31 A0 20 CD 70 15 CD E0 11 CD F8 10 3E FF D3
1610 08 21 00 40 C5 CD C0 14 FE A5 CA 23 16 CD C0 15
1620 C3 18 16 CD C0 15 4F C5 CD C0 15 C1 47 C5 CD C0
1630 15 77 23 C1 0B 78 B1 C2 2D 18 CD C0 15 32 B6 20
1640 CD E0 11 CD 60 14 CD 30 11 CF FF FF FF FF FF
1650 C5 01 80 80 79 D3 21 DB 22 1F D2 61 16 78 2F A1
1660 4F 3E FE A0 CA 6F 16 78 0F 47 B1 4F C3 55 16 71
1670 C1 C9 FF FF FF FF FF FF FF FF FF FF FF FF
1680 31 A0 20 CD A0 13 3E 00 D3 21 3C C3 88 16 FF FF
1690 F3 31 A0 20 CD 70 15 21 00 40 11 FF 1F 3E 0B 30
16A0 FB 76 71 23 1B 7A B3 C2 A0 18 CF FF FF FF FF FF

APPENDIX N

DETAILS OF RS232C AND INPUT OUTPUT CONNECTORS

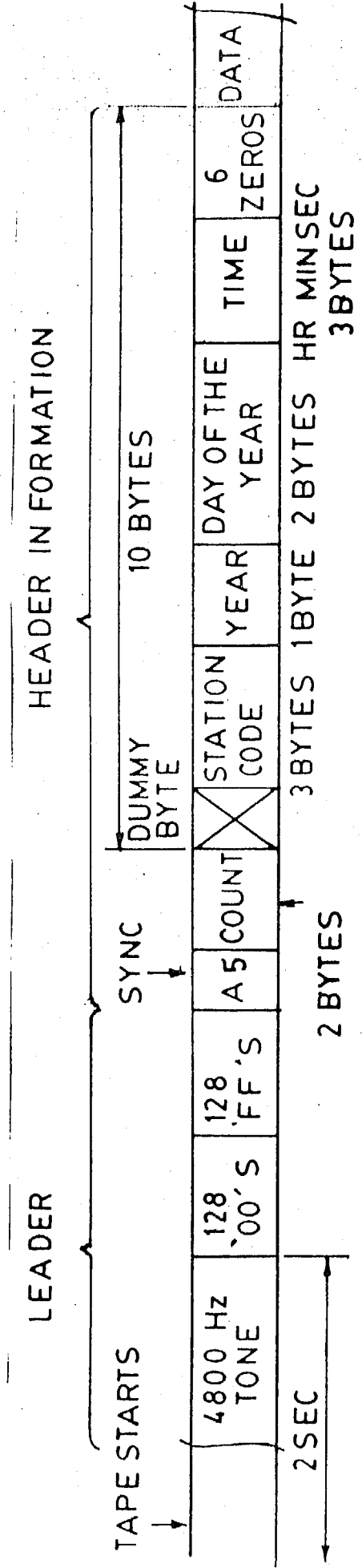
RS232 C,9 PIN FEMALE CONNECTOR D TYPE

1. NC
2. RECEIVE DATA
3. TRANSMIT DATA
4. DTR-----JOINED TO DSR
5. GND
6. DSR
7. RTS-----JOINED TO CTS
8. CTS
9. NC

INPUT OUTPUT CONNECTOR 9 PIN D TYPE FEMALE

1. CHANNEL 1 IN
2. CHANNEL 2 IN
3. CHANNEL 3 IN
4. CHANNEL 4 IN
5. GND
6. CHANNEL 1 OUT
7. CHANNEL 2 OUT
8. CHANNEL 3 OUT
9. CHANNEL 4 OUT

CASSETTE TAPE DATA FORMAT



- NOTES: 1 INTER BLOCK GAP \approx 95 MM TAPE (2 SECONDS)
 2 DATA RECORDED IN 8 BIT SERIAL FORM ONE START BIT (0)
 8 BIT DATA LSB FIRST ONE STOP BIT

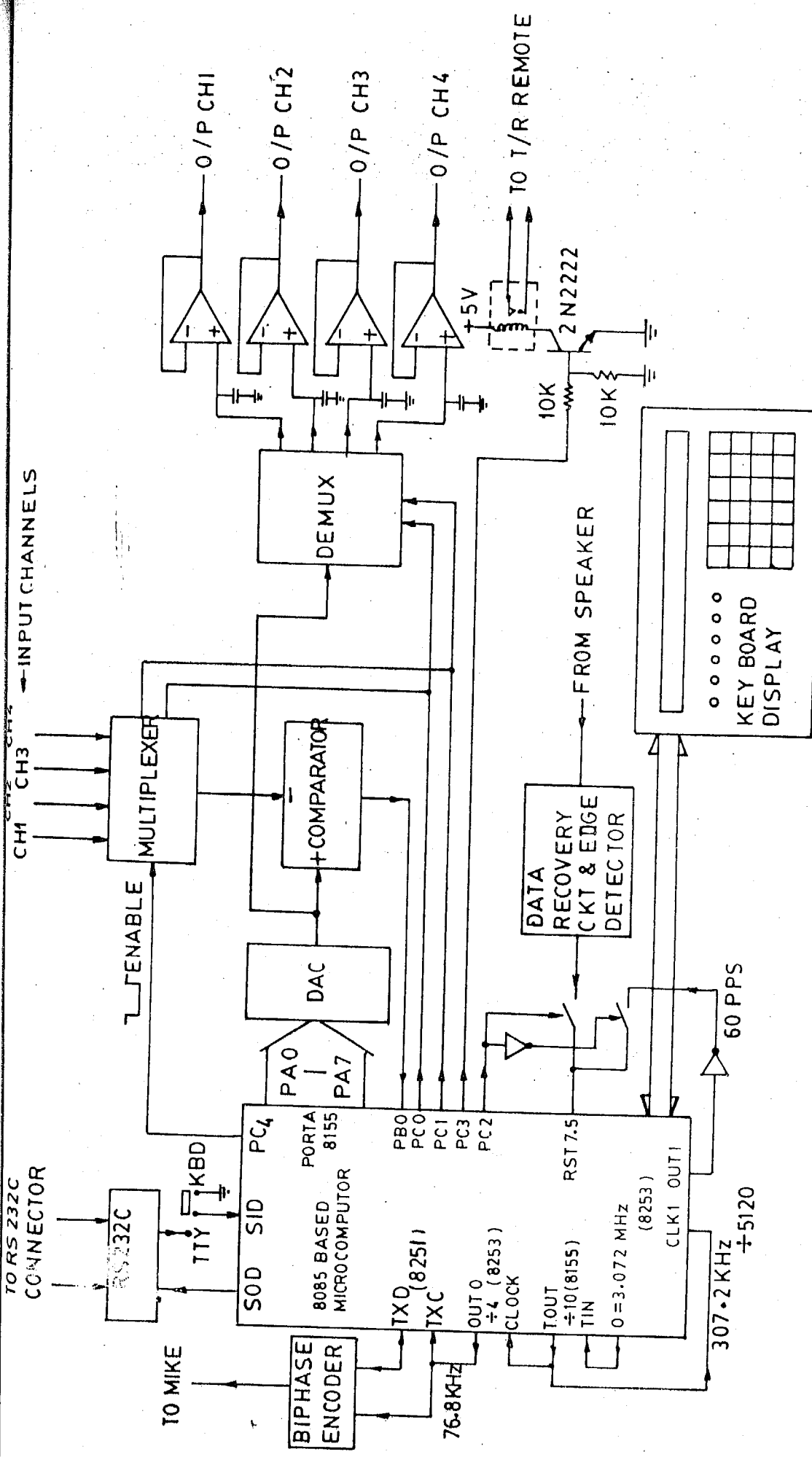


FIG-1 SYSTEM BLOCK DIAGRAM

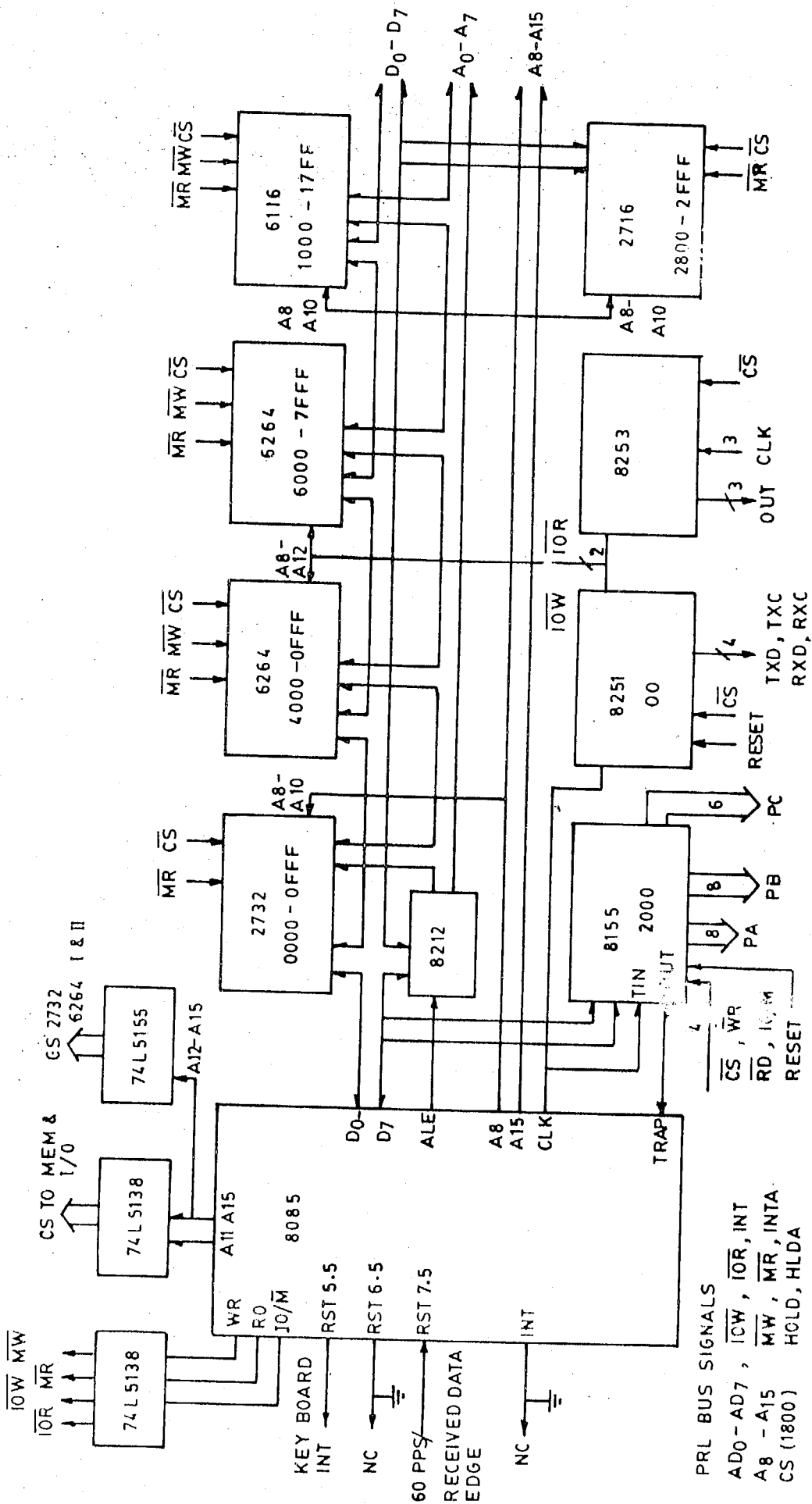
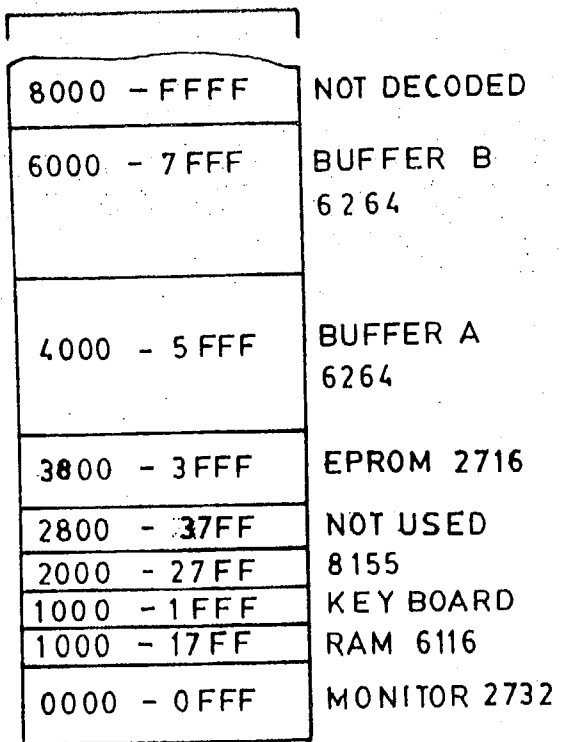
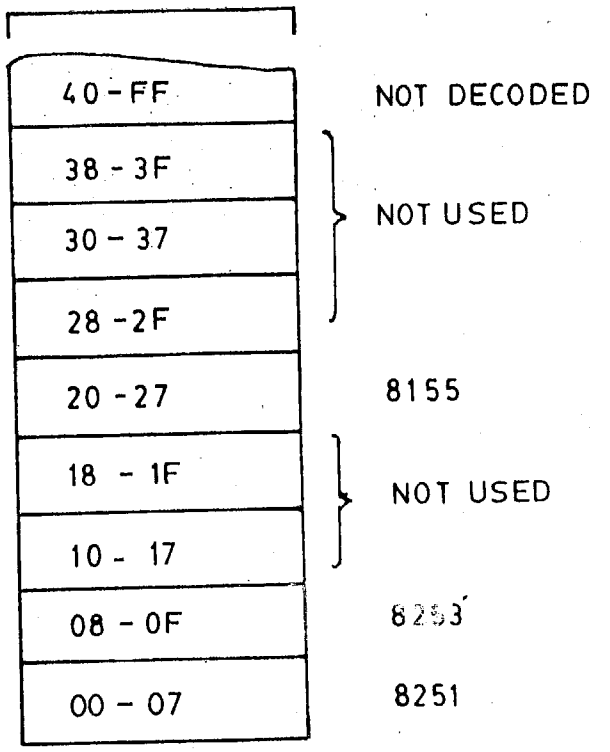


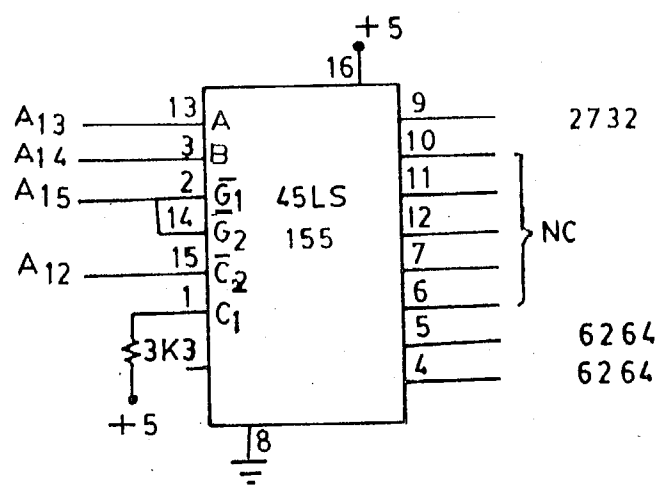
FIG-2 MICROCOMPUTER BLOCK DIAGRAM



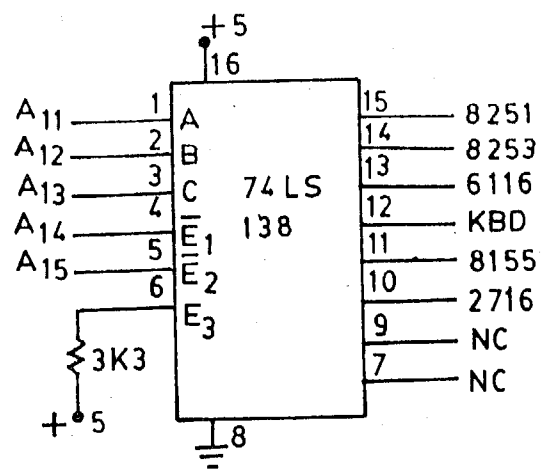
MEMORY MAP



I/O MAP



MEMORY DECODER
(OFF BOARD)



MEM & I/O DECODER

FIG.- 3 MEMORY MAP , I/O MAP AND DECODING LOGIC

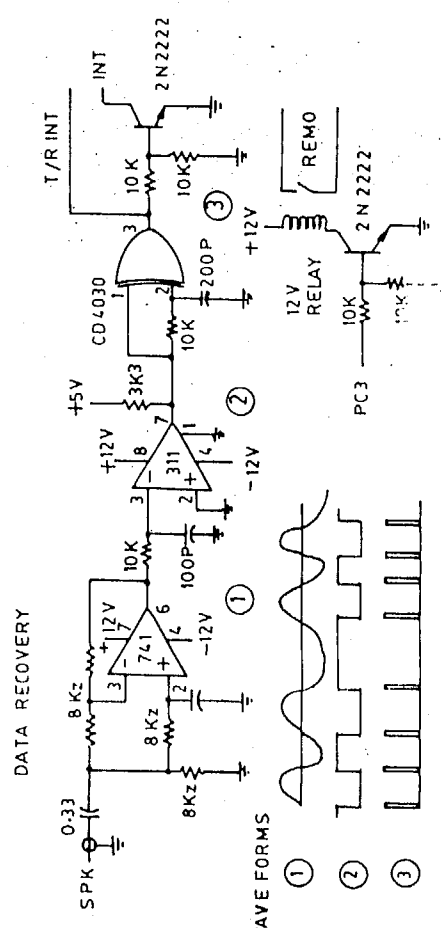
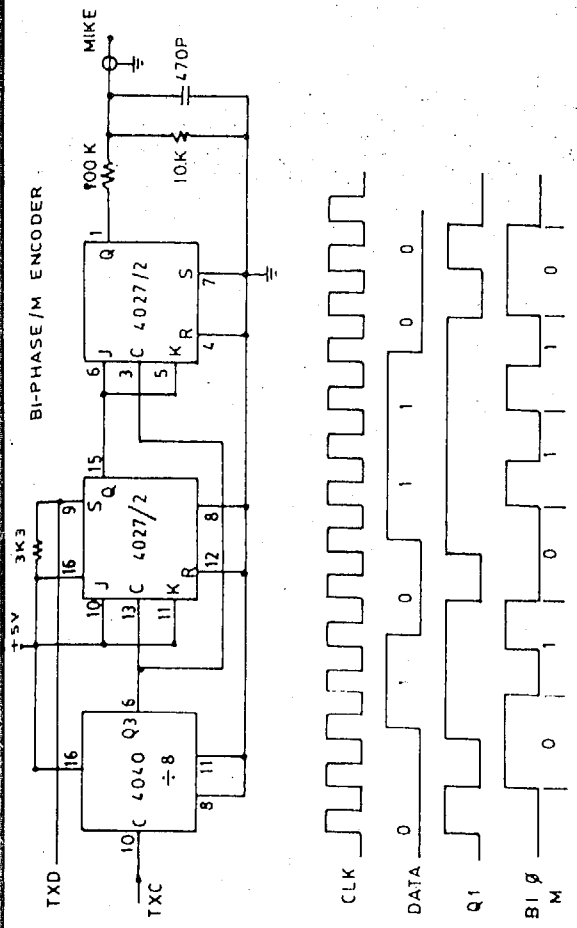


FIG. 5 CASSETTE TAPE READ/WRITE CIRCUIT

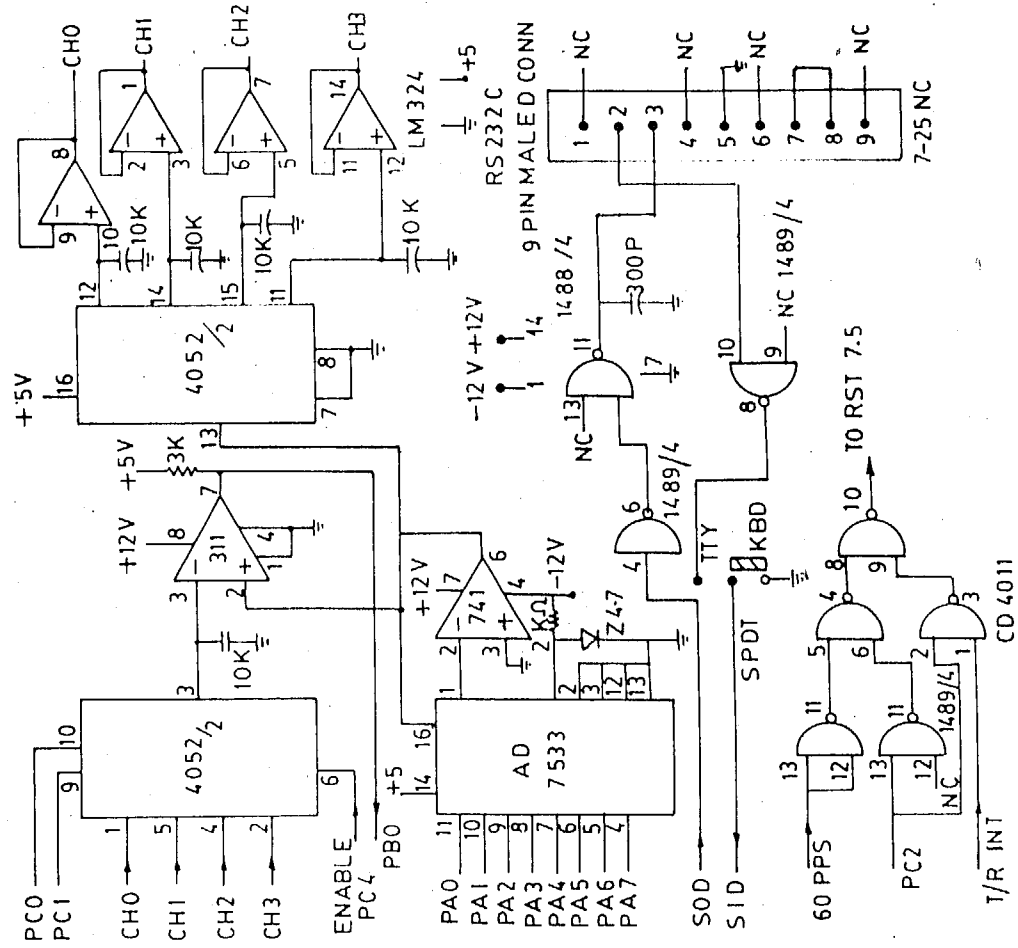


FIG. 4 MUX, DEMUX, D/A, INTERRUPT SELECT AND RS 232C DRIVER

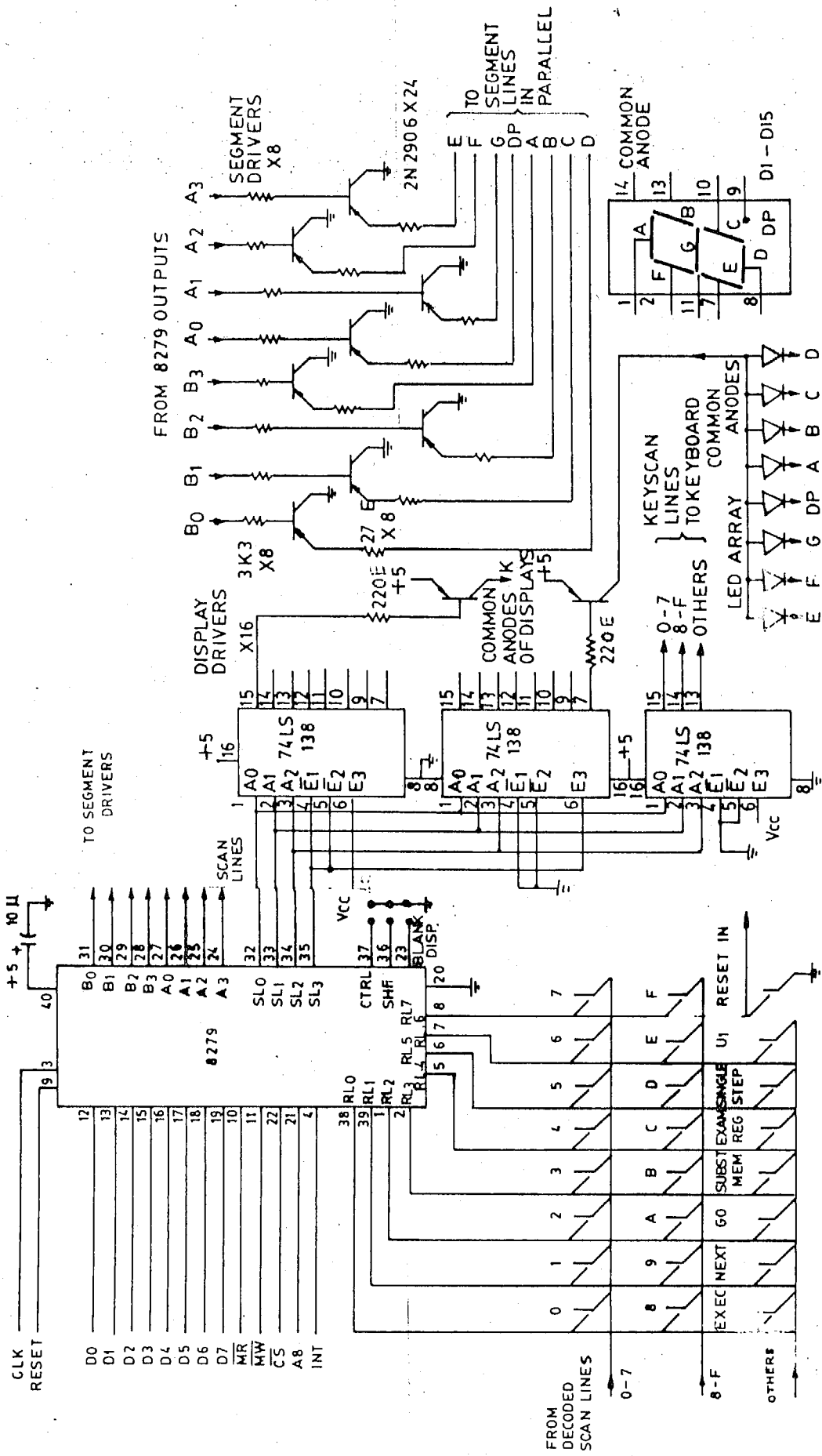


FIG.6 - KEY BOARD & DISPLAY

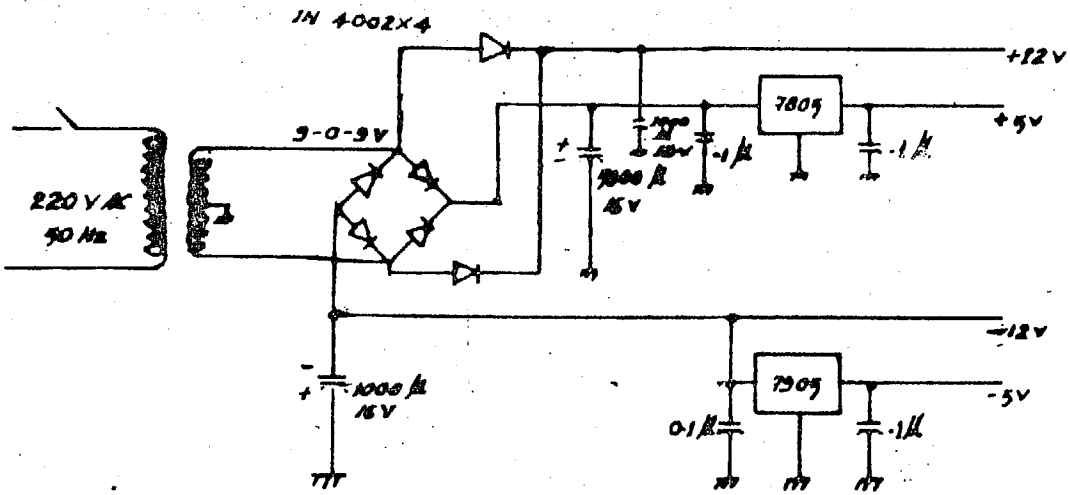
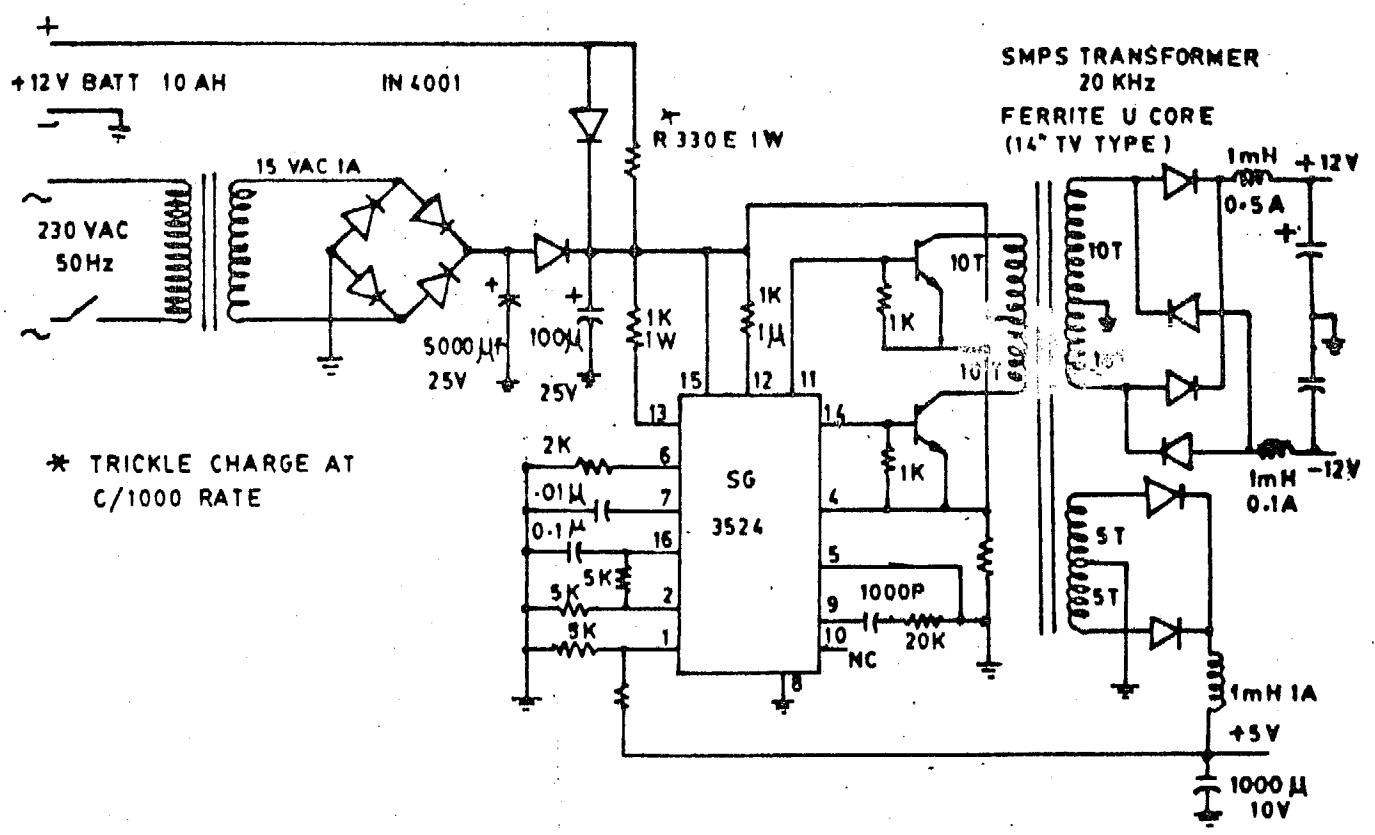


FIG 7 POWER SUPPLY.



* TRICKLE CHARGE AT C/1000 RATE

FIG-8 SWITCH MODE POWER SUPPLY WITH BATTERY BACK UP

CPU CARD (1/0)

KBD DISPLAY

CPU CARD BUS

CASSETTE INTERFACE

COMP. SIDE SOLD SIDE

1	CLK2	PC5
2	OUT 2	PC4
3	GATE 2	PC3
4	SOD	PC2
5	Timer in	PC1
6	SID	PC0
7	CLK1	PB7
8	TRAP	PB6
9	Timerout	PB5
10	GATE 1	PB4
11	RST 7.5	PB3
12	RST 6.5	PB2
13	OUT 0	PB1
14	RST 5.5	PB0
15	OUT 1	PA7
16	GATE 0	PA6
17	CLK 1	PA5
18	GND	PA4
19	TXD	PA3
20	TO OUT TO	PA2
21	RXD	PA1
22	RXC	PA0

COMP. SIDE SOLD SIDE

1	+5V	+5V
2	Reset out	Reset key
3	INTR	HOLD
4	NC	HLDA
5	INTA	Updckout
6	CLKOUT	8155 timer in
7	RST 5.5	A14
8	Reset in	A13
9	MR/IOR	A12
10	W/OW	A11
11	DO	A10
12	DI	A9
13	D2	A8
14	D3	A7
15	D4	A6
16	D5	A5
17	D6	A4
18	D7	A3
19	A8	A2
20	CS(KBDCS)	A1
21	Reset key	A0
22	GND	GND

NEAR LM324

1	-12V
2	GND
3	SPEAKER
4	+12V
5	PC3
6	REM
7	REM
8	NC
9	O/P CH3
10	O/P CH0
11	+5V
12	O/P CH1
13	O/P CH2
14	I/P CH0
15	I/P CH2, RXD
16	I/P CH3
17	I/P CH1
18	PC4
19	PC1
20	PC0
21	-12V
22	TXD

NEAR 4011 R/P AMP

1	GND
2	PA0
3	PA1
4	PA2
5	PA3
6	PA4
7	PA5
8	PA6
9	PA7
10	PC2
11	OUT1
12	NC
13	RST 7.5

ANALOG I/O GAIN

1	CH0 I/P
2	CH1 I/P
3	CH2 I/P
4	CH3 I/P
5	GND
6	CH0 O/P
7	CH1 O/P
8	CH2 O/P
9	CH3 O/P

NOTE:-SPEAKER/MIKE SHOULD BE CONNECTED THROUGH SHIELDED CABLE

FIG. 9 INTERCONNECTION DETAILS

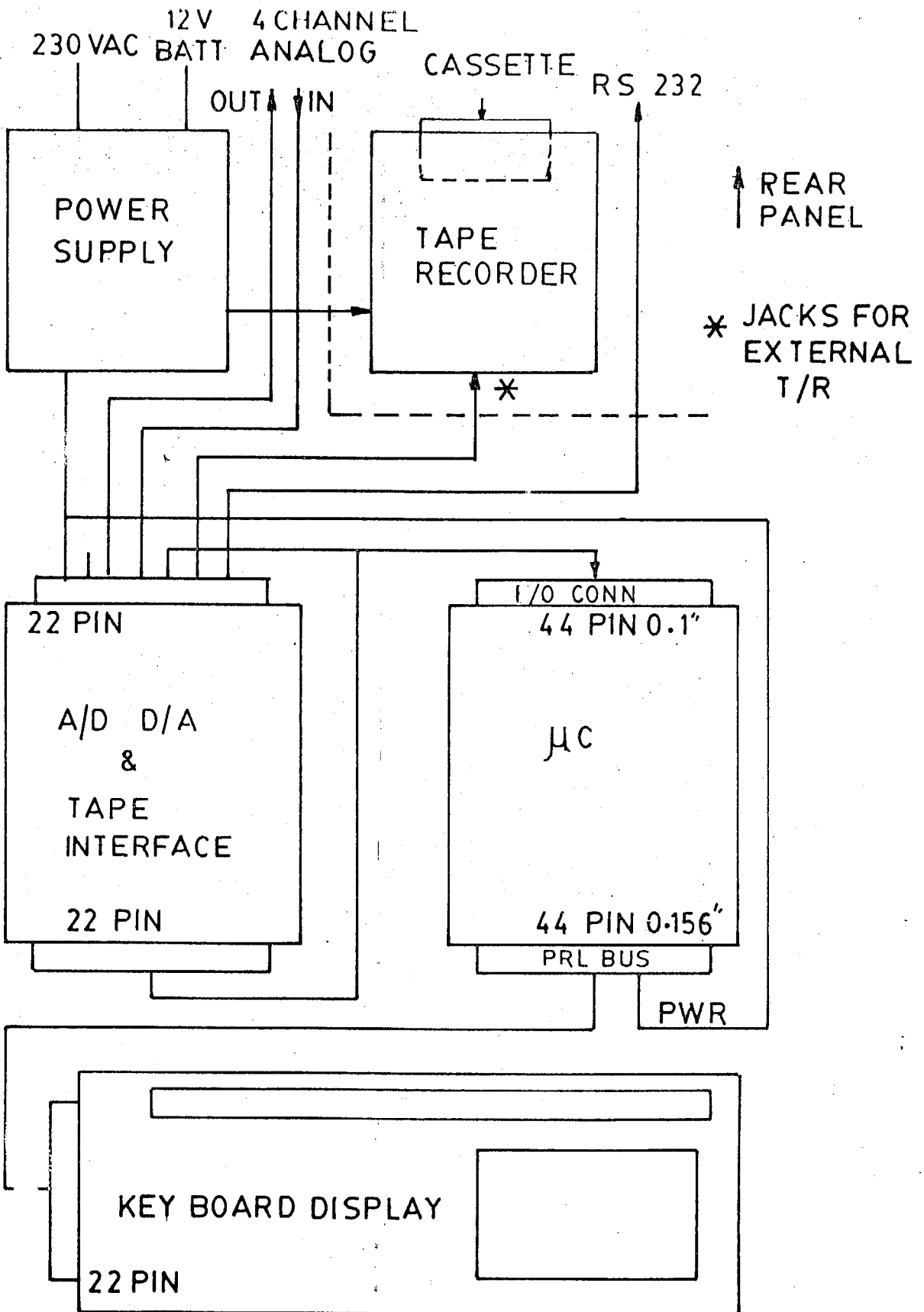


FIG. -10 APPROX LOCATION OF UNITS IN ENCLOSURE & WIRING PLAN

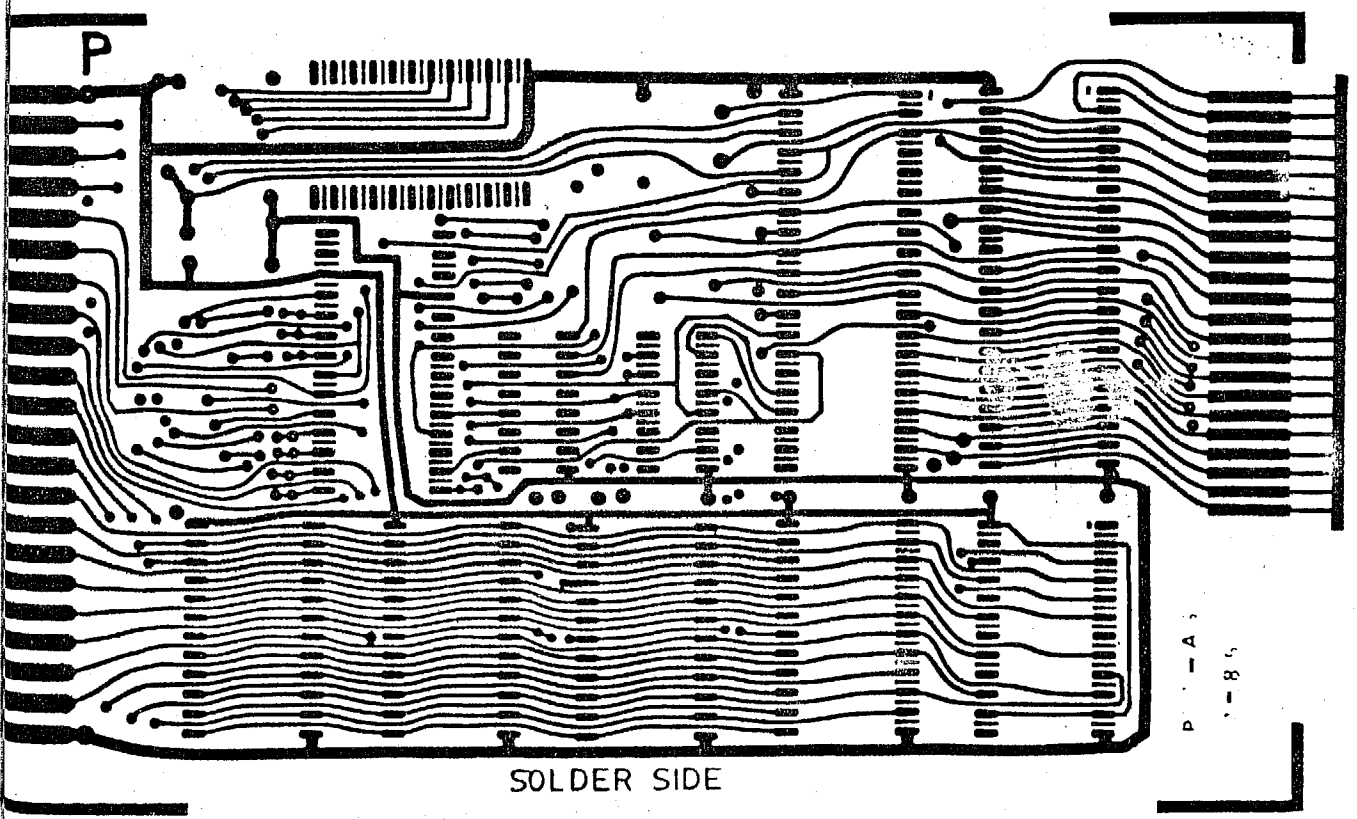
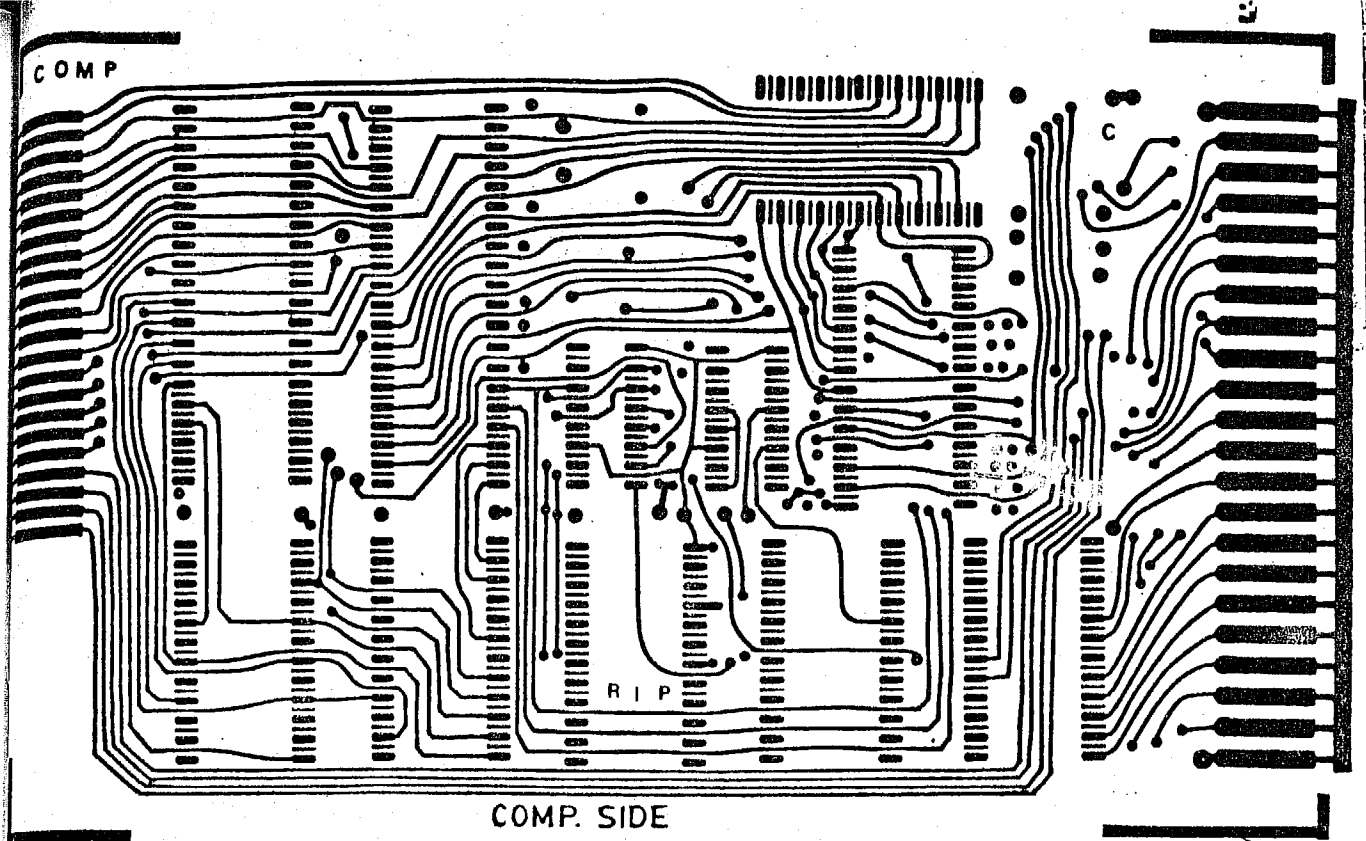
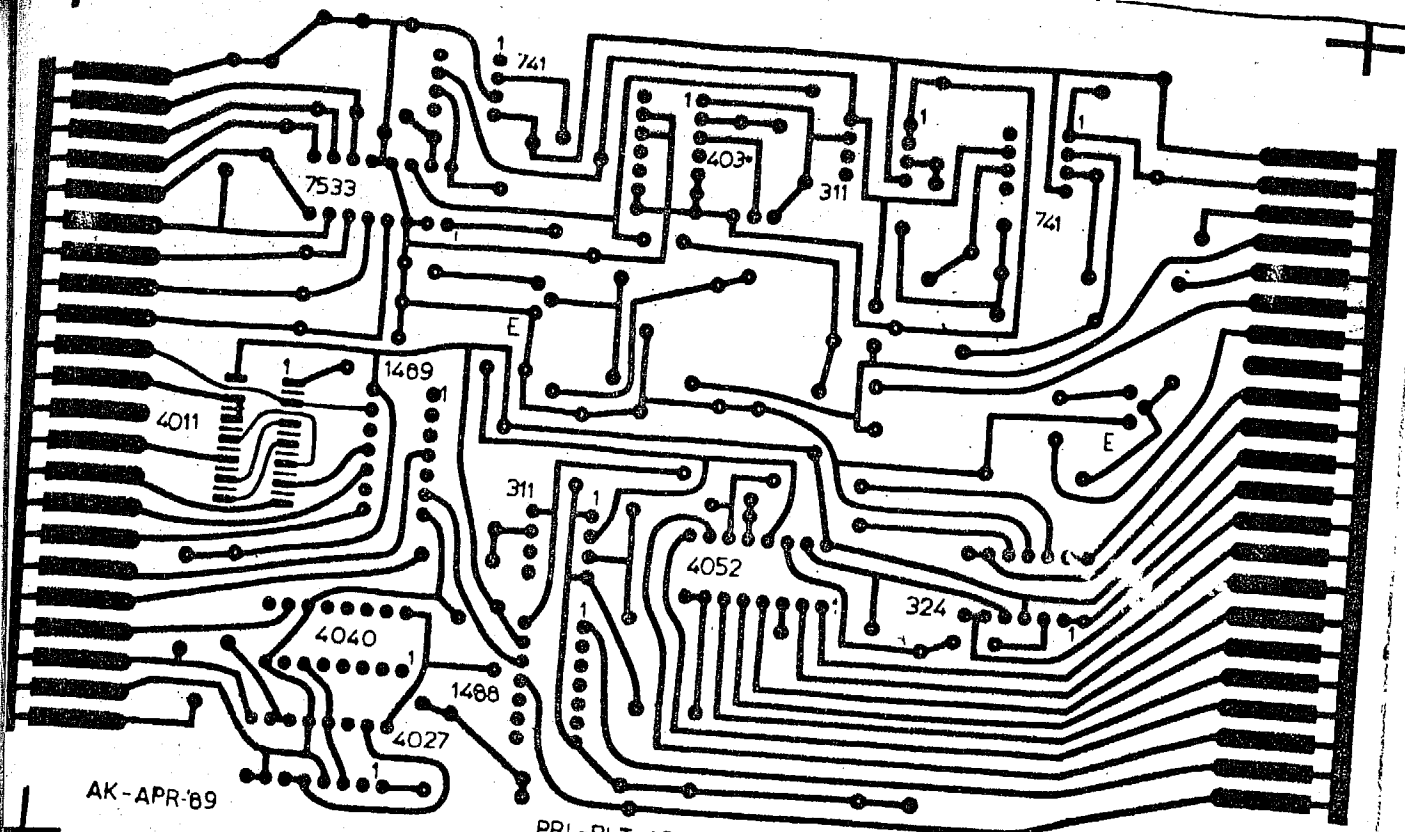


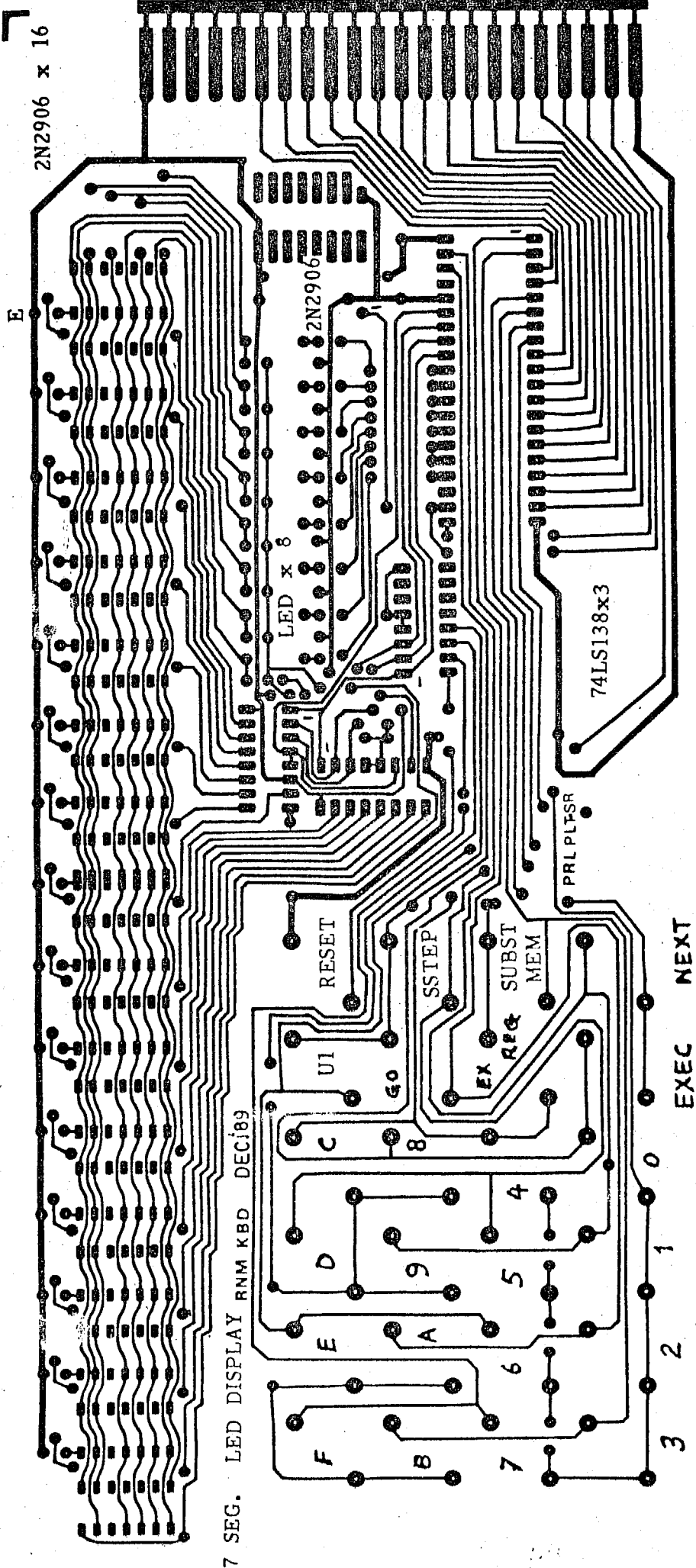
FIG. 11. PCB LAY-OUT. OF MICRO-COMP.



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FIG. 12. PCB LAY OUT OF D/A CARD



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NOTE : JUMPERS NOT SHOWN

FIG. 13 KEYBOARD/DISPLAY CARD (SOLDER SIDE)

FIG. 14

A VIEW OF INSTRUMENT

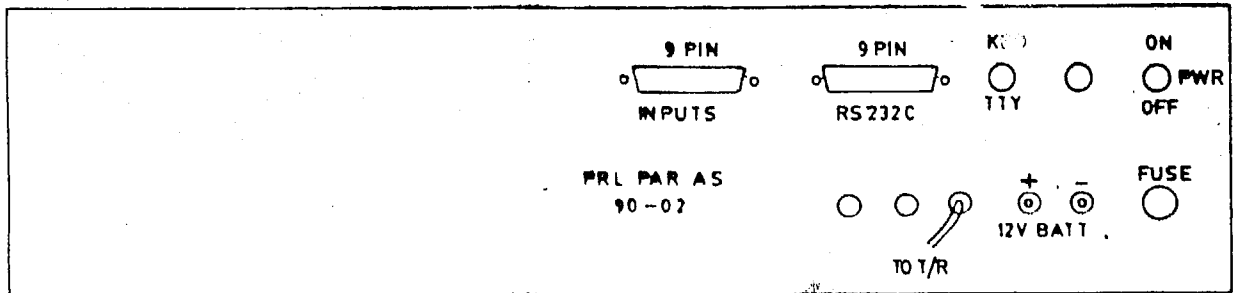
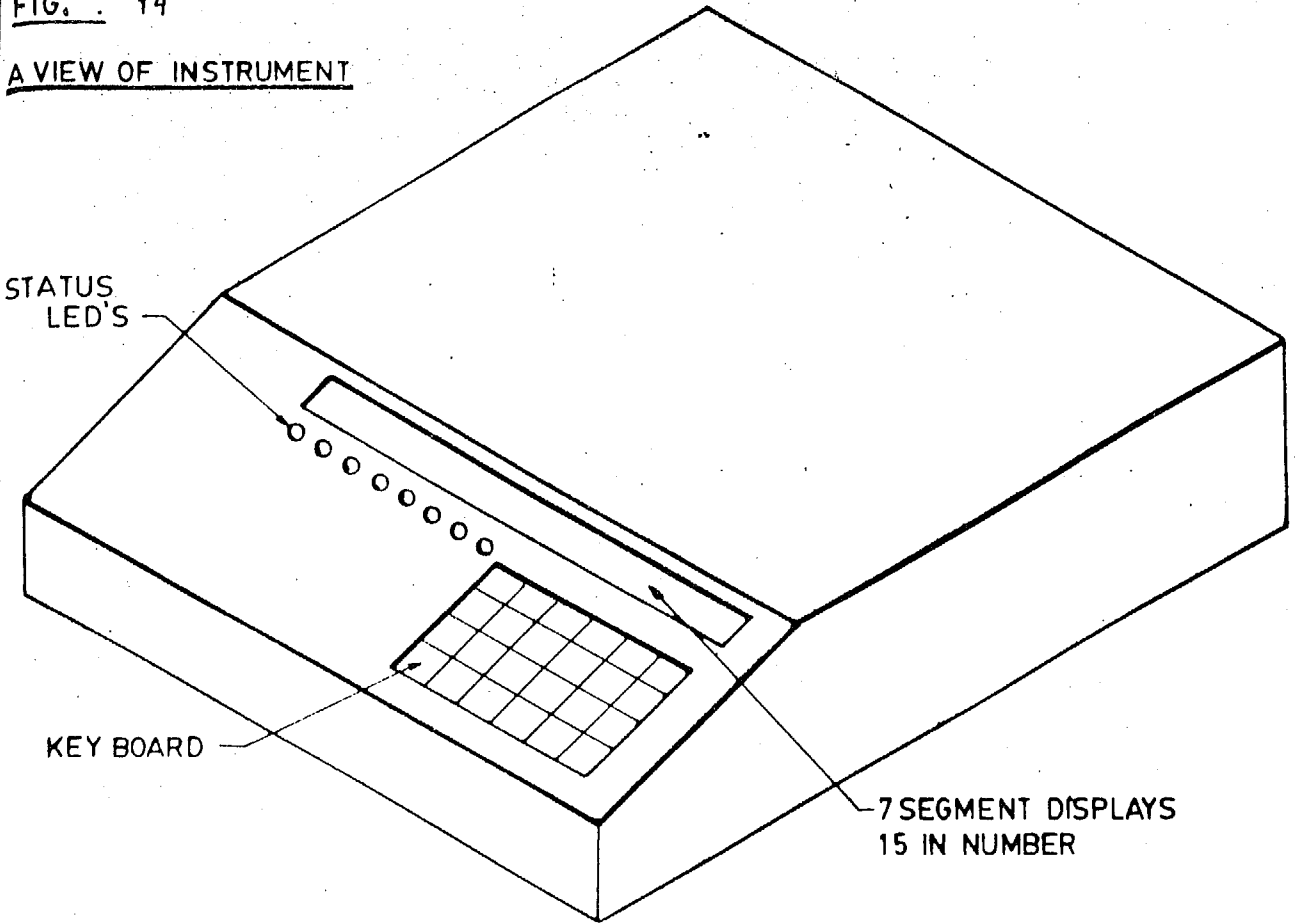


FIG.15 REAR VIEW