P R L

T E C H N I C A L N O T E

TN-89-67

DIGITAL MAGNETIC TAPE RECORDER INTERFACE FOR 8 BIT MICROCOMPUTER

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DIGITAL MAGNETIC TAPE RECORDER INTGERFACE

Abstract

Magnetic tape is the most cost effective medium for data recording. The half inch wide tape with its 9 track format has been extensively used in main frame computer systems for data interchange.An interface circuit has been designed to connect a digital tape drive to a 8 bit microprocessor system.The circuit can handle tape drives of upto 25 inch per second speed and can be used for both reading and writing of data. This system has been successfully employed for preprocessing of rocket instrument data.

DOCUMENT CONTROL AND DATA SHEET

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12. Abstract	:	9 Track digital magnetic tape is standard media for information interchange. The interface enables operation of Magnetic Tape Drive under software control of 8 bit microprocessor, to read and write data from tape to microprocessor memory and vice versa.
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1. Introduction

Data recording on 1/2" wide magnetic tapes in 9 track format is the most popular method used for data archiving and exchange. This medium has been so extensively used for this purpose that it is almost impossible to think of any other means to realise these goals. Data preview and preprocessing require very modest equipment setup along with a suitable tape drive.The preview and preprocessing are better done in the users' laboratory than at a main frame computer for reasons of cost effectiveness,and user interaction. An interface for the digital magnetic tape recorder has been designed which can be driven by any 8 bit microcomputer. It is based on a proprietary Microcomputer BUS designated as PRL BUS which is more or less similar in signals to the PC BUS,but the cards are of 4 1/2"x6 1/2" size. This BUS was chosen on account of the fact that quite a few microprocessor and interface cards based on this BUS have been developed in our group.The interface has onboard parity generate and check logic as well as necessary TTL logic to make it compatible with the tape drives of PERTEC peripheral corporation. It has been successfully employed for preview and plotting of rocket instrumentation data.

2. Salient features of tapes and tape drives

The magnetic tape used for data storage is 1/2" wide and utilizes 9 track format.Out of 9 tracks,8 tracks are used for one byte of data and the ninth track for parity check bit. In case of 7 track format which was in use

earlier, data is recorded as 6 bit code plus parity bit. Track allocation and spacing have been reproduced in Appendix-A. Tape is supplied in spools of 7" and 10.5" diameter which contain 600' and 2400' of tape respectively. A write enable ring is attached to the spool to signal the tape drive that the tape on the deck is to be written on.

The drives are designated by spool size,tape speed, number of tracks and Read/Write head arrangement.There may be single head or a read after write head.The latter enables to verify the record almost at the time of writing itself. Tape speeds vary from 12.5" per second to 120" per second. Low speed drives use tension arm tape loop whereas high speed drives use vacuum column tape loop to enable fast start stop motion of the tape.Speeds of 25" per second, 45" per second and 50" per second are fairly common.The drives are factory set for a particular speed.However,the electrical interfaces are identical and speed matters only as far as time taken for reading and writing of data is concerned.

Data density of 800 CPI (Characters Per Inch) and 1600 CPI are used for NRZI and PE (Phase Encoder) recordings respectively. The electrical interface of the tape drive includes the following signals:

1. Data Read
2. Data Write
3. Control and Status

The outgoing signals from the drive emerge from open collector devices which are to be terminated on the user

interface by a resistor network of 220 and 330 ohms and electrically buffered afterwards through schmitt trigger type inverter. Likewise,the input signals to the drive have resistive termination and a schmitt trigger buffer on the tape drive electronics board. The data read-write electronics contains 9 identical circuits corresponding to each of the data tracks. Electrical specifications and connections of the Tape Drive have been given in Appendix A and B respectively. The odd parity is used in data and therefore parity bit is '1' for all zeros data.This is useful in generation of clock for recovery of data.If all the data lines are 'OR'ed,atleast one of those would have 1 level and thus a clock signal can be easily generated.

3. The Interface

The tape drive is usually operated alongwith some sort of formatter supplied alongwith it.It may be of buffered or unbuffered type. The formatter communicates with the user interface, which is called a "Customer's Controller".The formatter generates all the necessary signals required by the drive including parity etc.Thus,the customer controller gets simplified to a large extent.However,it has been the author's experience that the formatter is more complex piece of equipment and usually fails more frequently than the drive itself. The latter is fairly rugged and can last for very long time. The formatter supplied by the manufacturer alongwith the tape drive are designed to be of universal type, to be used alongwith tape drives of all speeds and hence contain very large number of TTL IC's and

PAL's.

The low speed drives are,however,adequate for most of the day to day data handling purposes.The slow speed drive can easily be interfaced to 8 bit microprocessor through a suitable I/O interface. The design presented here contains 14 TTL IC's, 3 LSI's and has all the facilities to read or write the data within certain limits on data block range.

4. Design

The block diagram of the interface has been given in Fig. 1. The magnetic tape interface has been designed around two Programmable peripheral interface type 8255 and one timer type 8253. The I/O port configuration has been given in Fig.2. One of the 8255's is used in mode I to facilitate data transfer in strobe mode.Read strobe latches the read data lines RD0-RD7 in port B (E9). The data are also presented to a parity generator/checker type DM-8220,parity input of which is RDP (read parity) line.The output of parity checker is latched in a flip-flop (7474) by Read strobe and used for error detection.The A port of the same 8255 (E8) is used for generation of write data WD0-WD7.The parity bit WDP is generated in DM-8220 connected in parallel to the port A.Odd parity is used for read as well as write operation. The write strobe is generated in timer 8253 at a rate of 10 KHz for 12.5" per sec tape speed.8253 has limitations for clock frequency and therefore a divide by 2 circuit has been implemented in the second D flip-flop of 7474 used for latching parity bit,to generate a square wave of 1.5 MHz.This has,in turn,been divided by 5 in one

section of 8253, to get 300 KHz square wave needed for generation of Write Strobe.The 300 KHz square wave drives the second counter (02) which is programmed for mode 2 to generate pulses of 3 microsecond width,at a rate of 10 KHz. These pulses are used for transfering write data to port and generation of Write Data Strobe (WDS) and Write Amplifier Reset (WARS) strobes through gates controlled by PC2 & PC3 of the second 8255 at (E0).

The PA0-PA5 lines of port A of the second 8255 at (E0) are used for tape control signals and PB2-PB7 lines of port B as input for status signals from the drive.PB0 and PB1 have been used for sensing the data flag generated at PC0 line of 8255 I at E8, and the parity check bit output of 7474 respectively.All the I/O lines going to the tape drive have been buffered as shown in Figures 3,4 and 5.The I/O port and timer map and utilization have been summarized in Appendix G. The pin connections of the Tape Interface have been given in Appendix D,and that of PRL BUS in Appendix C. List of components have been given in Appendix J.The PCB artwork and part placement have been given in Figures 8 and 9 respectively.

5. Error detection and correction

As already explained, odd parity is utilized for error detection. 9 track tape format also requires that a cyclic redundancy check character (CRCC) and a linear redundancy check character (LRCC) be written at the end of the block after a gap of 4 character spaces each.LRCC ensures that the total number of magnetization transitions in any track

is even. It is generated by the drive on receipt of WARS pulses. The CRCC,however,has to be supplied by the interface along with its write data strobe WDS.CRCC can be generated by special purpose integrated circuits or by software.It is worth noting that data is written in blocks and hence microprocessor can be effectively used for generation of CRCC just before start of write operation.CRCC utilizes parity bit generation and therefore 8085/Z80 microprocessors with their built-in branch/call on parity instructions are quite appropriate for CRCC generation.CRCC can be used for error correction of data provided errors are confined to only one data line.

6 Generation of the CRC Character

The following algorithm has been used to generate the CRCC.

1. E register is used to store CRC character. DE pair is therefore cleared in the beginning.
2. Data byte is exclusively ORed to the CRCC byte in E register.
3. The parity information is converted into carry bit.
4. Now the result of step 2 alongwith carry are rotated to right, carry goes to bit 7 and bit 0 to carry.
5. If new carry is 1, then result is exclusively ORed by 3C(H) to invert bits 2, 3, 4 and 5, else it remains as it is.
6. This form CRCC and is stored back in E. The programme is repeated till all the data bytes are over.
7. CRCC byte is exclusively ORed by D7 to invert all the

bits except 3 and 5.

8. Parity of the CRCC byte is stored in D register.
9. Contents of D & E., i.e. parity of CRCC and CRCC are stored in 20B6 and 20B5 respectively.

It is interesting to see the characteristics of the CRCC in some detail.

1. It can be all zero character.
2. Its value is such that the LRCC has always odd parity.
3. It has odd parity for even number of data and even parity from odd number of data.

The odd parity of the data byte as well as CRC character is generated in DM-8220.It is,therefore,necessary to use only even block size for data to maintain compatibility of CRCC to the IBM format.This usually poses no special problem. Extra character can always be inserted in the block to make total bytes even.

7. Software

Basic software subroutines to facilitate data read and write have been written. The read and write software including port and timer initialization and generation of CRCC has been accommodated in less than 768 bytes.As explained earlier, memory location 20B5 and 20B6 have been used for storage of CRCC character and its parity.The programme is to be run at memory location 2800 to 2AFF.The subroutines do not take care of select line which should be forced true on the tape recorder without which the operation of tape drive is not possible.These subroutines have been extensively used for data quick look operation.

The flow charts for block write and read operations have been given in Figures (6) and (7).The list of sub- routines and addresses have been given in Appendix H.Subroutines have been written in the machine code for 8085 microprocessor and listed in Appendix I.

8. **Operation**

The block write and read subroutines use register pair H, L as memory pointer and B.C as byte counter.While reading B, C contains the number of bytes read from one block of data. The machine code routines listed in Appendix I may be directly used for read or write with suitable modification in destination/source memory address and value of byte count. The rewind subroutine comes handy for operation from the console.

As all the ports of 8255 are in input mode after reset, the outputs of buffers do not permit normal operation of the tape drives before initialization.The ports and timer may be initialized by programme at 2AC0.Now the tape can be loaded on the drive and brought to load point.The drive has to be brought on line before any command can be issued to it from console.

On the issue of read command,SFC goes to logical one and tape starts moving, the microprocessor looks for the data on RD0- RD7 lines.Data is read on each RDS pulse and stored in RAM pointed by HL.If time gap between successive RDS pulses increases beyond a prescribed limit,the block is assumed to be over and the tape drive is stoped after appropriate delay.BC register contains the byte count

and occurrance of parity error during read operation is indicated by presence of carry bit.

Operation of write command is similar.On write command SFC and SWS signals go to 1.The tape spool should have a write enable ring installed to perform any write operation. The tape starts moving and after a suitable time delay data is written byte by byte by strobe pulse at a rate of 10 KHz. WDS pulses are provided for each byte. CRC character is written after a gap equivalent to 4 characters at the end of the data block.Subsequently WARS pulse is given to the drive to write LRCC 4 characters gaps beyond CRCC.Now the write operation is over and tape is stoped after appropriate time delay.Interrecord gap of 0.6" is split in two parts, 0.5" is provided at the beginning of the write operation and 0.1" at the end.Four inch leader is provided at the Beginning of Tape (BOT) and at every file mark.File mark character 13H is written by a separate subroutine alongwith LRCC.CRCC is not needed for File mark.

9. Conclusion

A small interface card for 1/2" digital tape drive has been designed. It is compatible to 8 bit microcomputer bus and is driven under software control to provide all the necessary control signals to the tape drive.It has been successfully tested for both read as well as write operations.

10. Acknowledgements

The author is thankful to Professors Satya Prakash and B.H.Subbaraya for their appreciation of the development

work carried out in connection with this interface.Thanks are also due to Mr.Nilesh Shah for help during the testing phase and Mr.H.D.Parikh for the neat and correct wiring of the PC card.The tape read sub-routine has been adapted from the original one written by Dr.Surendra Pal in course of his Ph.D. thesis during 1982-85. Mr.V.K.Parmar had contributed towards the fabrication of the earlier model of the circuit.

List of Illustrations

Appendices

A. Nine track NRZI 800 CPI tape format, Interblock gap and electrical Interface Definition (Ref.3).

B. Tape Drive Signals (Ref.3).

C. PRL BUS signals and Card Dimension.

D. Magnetic Tape Interface Signals.

E. 44 Pin edge connector to 25 pin D Connector Harness

F. Tape drive signals on 25 pin D connector adaptor.

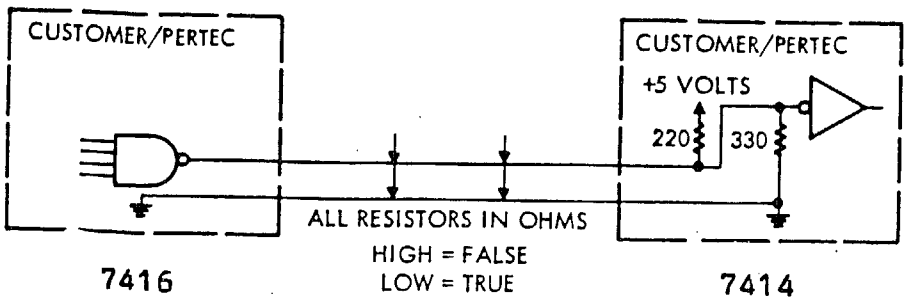
G. I/O Map and Utilization.

H. Sub-routine Address.

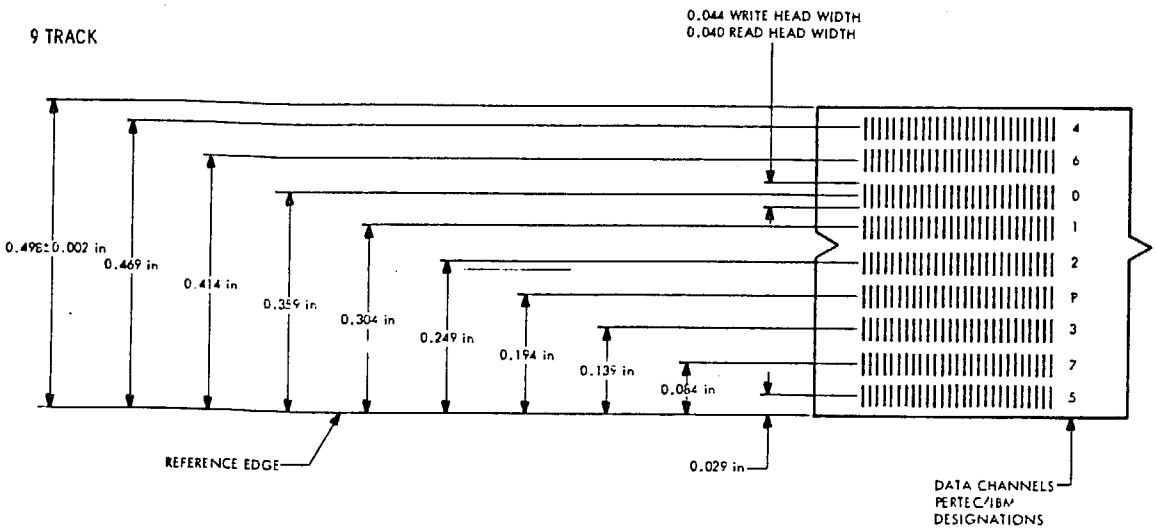
I. Disassembled software and Hex Dump.

J. List of Components.

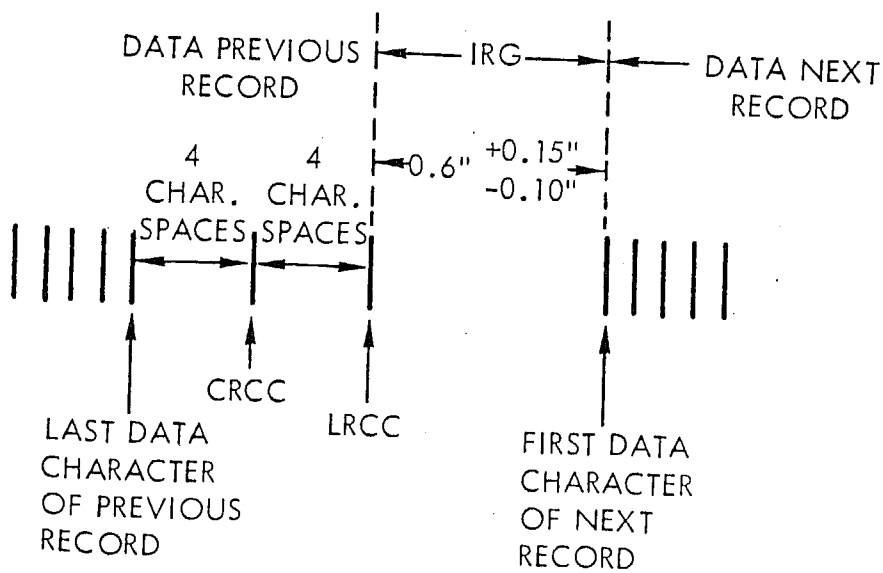
APPENDIX-A



Interface Configuration



9-Track Allocation and Spacing



APPENDIX-B

Interface Connections

Transport Connector	36 Pin Etched PC Edge Connector
Mating Connector	36 Pin ELCO 00-6007-036-980-002

Connector (Reference Figure 2-1)	Live Pin	Ground Pin	Signal*
J101	B	2	→ OVERWRITE (OVW)
	J	8	→ SELECT (SLT)
	C	3	→ SYNCHRONOUS FORWARD Command (SFC)
	E	5	→ SYNCHRONOUS REVERSE Command (SRC)
	H	7	→ REWIND Command (RWC)
	L	10	→ OFF-LINE Command (OFFC)
	K	9	→ SET WRITE STATUS (SWS)
	D	4	→ DATA DENSITY SELECT (DDS) (Optional)
	T	16	← READY (RDY)
	M	11	← ON-LINE Command
	N	12	← REWINDING (RWD)
	U	17	← END OF TAPE (EOT)
	R	14	← LOAD POINT (LDP)
	P	13	← FILE PROTECT (FPT)
	F	6	← DATA DENSITY INDICATOR (DDI)
J102	A	1	→ WRITE DATA STROBE (WDS)
	C	3	→ WRITE AMPLIFIER RESET (WARS)
	L	10	→ WRITE DATA PARITY (WDP)
	M	11	→ WRITE DATA 0 (WD0) } Omit for
	N	12	→ WRITE DATA 1 (WD1) } 7-Channel Head
	P	13	→ WRITE DATA 2 (WD2)
	R	14	→ WRITE DATA 3 (WD3)
	S	15	→ WRITE DATA 4 (WD4)
	T	16	→ WRITE DATA 5 (WD5)
	U	17	→ WRITE DATA 6 (WD6)
	V	18	→ WRITE DATA 7 (WD7)
J103	2	B	← READ DATA STROBE (RDS)
	1	A	← READ DATA PARITY (RDP)
	3	C	← READ DATA 0 (RD0) } Omit for
	4	D	← READ DATA 1 (RD1) } 7-Channel Head
	8	J	← READ DATA 2 (RD2)
	9	K	← READ DATA 3 (RD3)
	14	R	← READ DATA 4 (RD4)
	15	S	← READ DATA 5 (RD5)
	17	U	← READ DATA 6 (RD6)
	18	V	← READ DATA 7 (RD7)

Appendix C

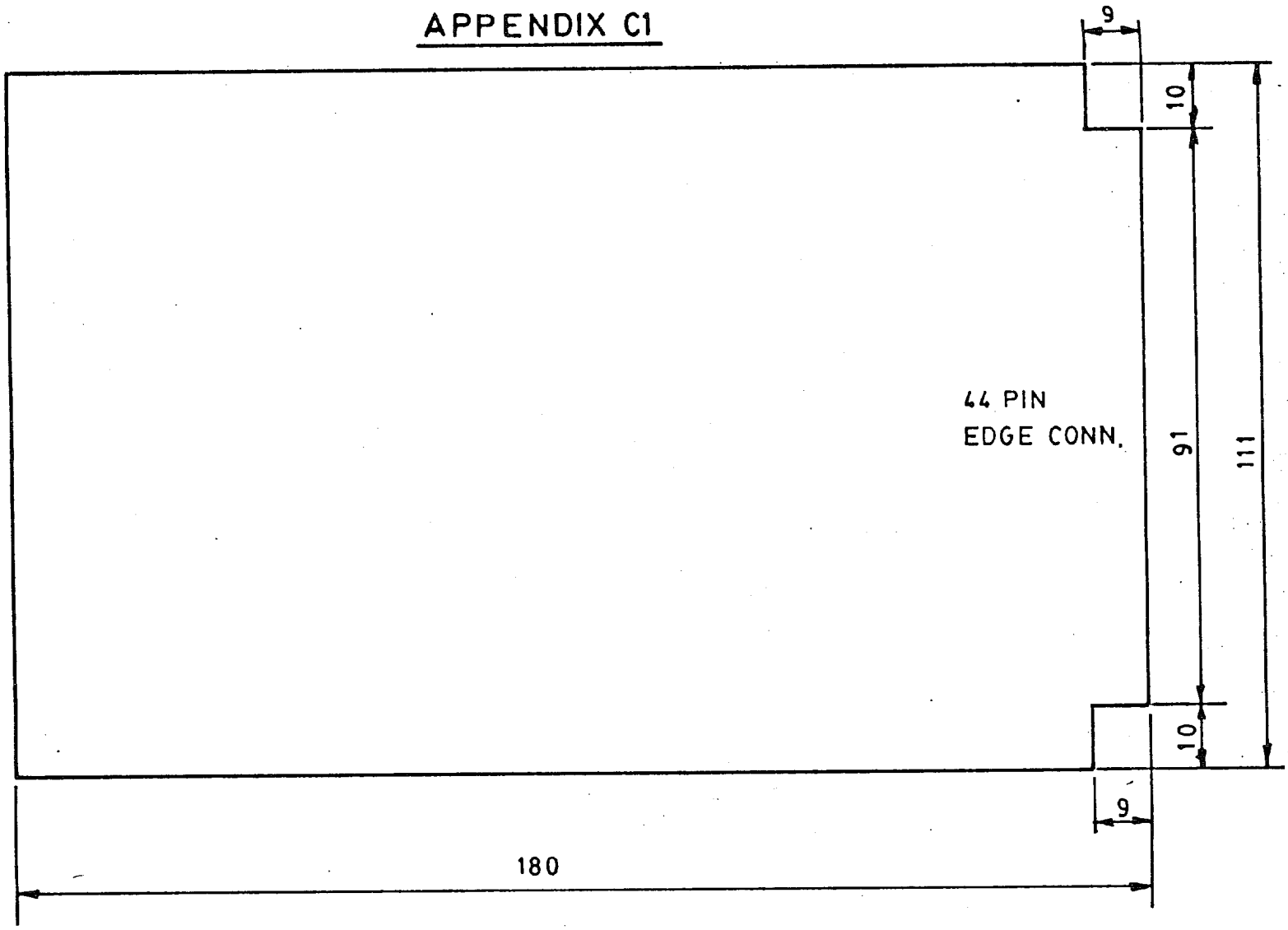
PRL BUS Signals, Connector Type 44 PIN 0.156" Dual Readout

O/E/N 8607 044 21 14

	Component Side		Solder Side
1	GND (Bottom most)	1	GND
2	D0	2	A0
3	D1	3	A1
4	D2	4	A2
5	D3	5	A3
6	D4	6	A4
7	D5	7	A5
8	D6	8	A6
9	D7	9	A7
10	MR *	10	A9
11	MW *	11	A9
12	IOR *	12	A10
13	IOW *	13	A11
14	NC	14	A12
15	NC	15	A13
16	NC	16	A14
17	NC	17	A15
18	INTA	18	CLOCK OUT
19	NC	19	HLDA
20	INTR	20	HOLD
21	RESET OUT	21	RESET (BUTTON)
22	+5V (Topmost)	22	+5V

*INVERTED SIGNALS

APPENDIX C1



CARD DIMENSIONS µP BOARD (ALL DIM ARE IN MM)

Appendix D

MAGNETIC TAPE INTERFACE DETAILS

44 PIN 0.1" CONNECTOR

	Component Side	Solder Side	Remarks
1.	RDP	GND	INPUTS
2.	RD6	RD7	
3.	RD4	RD5	
4.	RD2	RD3	
5.	RDO	RD1	
6.	GND	GND	
7.	NC	RDS	
8.	NC	GND	
9.	NC	REWINDING	
10.	ON LINE	FPT	
11.	LDP	EOT	
12.	NC	RDY	
		NC	OUTPUTS
14.	WARS	WDS	
15.	WDO	WD1	
16.	WD2	WD3	
17.	WD4	WD5	
18.	WD6	WD7	
19.	OFF	WDP	
20.	SRC	SFC	
21.	REWIND	SELECT	
22.	SWS	GND	

Appendix-E

44 PIN CONNECTOR TO TAPE DRIVE INTERFACE

COMPONENT SIDE	DESTINATION	SOLDER SIDE	DESTINATION
1. RDP	-- CON3-1	1 GND	
2. RD6	-- CON3-10	2 RD7	-- CON3-11
3. RD4	-- CON3-8	3 RD5	-- CON3-9
4. RD2	-- CON3-6	4 RD3	-- CON3-7
5. RD0	-- CON3-4	5 RD1	-- CON3-5
6. GND		6 GND	
7. NC		7 RDS	-- CON3-2
8. NC		8 GND	
9. NC		9 REWINDING	-- CON1-8
10. ON LINE	-- CON1-7	10 FPT	-- CON1-9
11. LDP	-- CON1-10	11 FOT	-- CON1-12
12. NC		12 RDY	-- CON1-11
13. NC		13 NC	
14. WARS	-- CON2-2	14 WDS	-- CON2-1
15. WD0	-- CON2-5	15 WD1	-- CON2-6
16. WD2	-- CON2-7	16 WD3	-- CON2-8
17. WD4	-- CON2-9	17 WD5	-- CON2-10
18. WD6	-- CON2-11	18 WD7	-- CON2-12
19. OFF	-- CON1-6	19 WDP	-- CON2-3
20. SRC	-- CON1-2	20 SFC	-- CON1-1
21. REWIND	-- CON1-3	21 SELECT	-- CON1 4
22. SWS	-- CON1-5	22 GND	

NOTE: Destination connector and pin numbers refer to the

25 pin D type connectors and cable adapter interface used to connect the tape drive to the tape controller circuit, signals on the PCB edge connectors on the tape drive have been brought on 25 pin Female D type connectors to simplify the cabling.

Appendix F

MAGNETIC TAPE TO 25 PIN D TYPE FEMALE CONNECTOR

CONNECTOR-1	1	SFC	(J101/C)	14	GND (J101/3)
	2	SRC	(J101/E)	15	GND (J101/5)
	3	REWIND	(J101/H)	16	GND (J101/7)
	4	SELECT	(J101/J)	17	GND (J101/8)
	5	SWS	(J101/K)	18	GND (J101/9)
	6	OFF	(J101/L)	19	GND (J101/10)
	7	ONLINE	(JJ01/M)	20	GND (J101/11)
	8	REWINDING	(J101/N)	21	GND (J101/12)
	9	FPT	(J101/P)	22	GND (J101/13)
	10	LDP	(J101/R)	23	GND (J101/14)
	11	RDY	(J101/T)	24	GND (J101/16)
	12	EOT	(J101/U)	25	GND (J101/17)
	13	OVW	(J101/B)	26	GND (J101/2)
CONNECTOR-2	1	WDS	(J102/A)	14	GND (J102/1)
	2	WARS	(J102/C)	15	GND (J102/3)
	3	WDP	(J102/L)	16	GND (J102/10)
	4	NC		17	NC
	5	WD0	(J102/M)	18	GND (J102/11)
	6	WD1	(J102/N)	19	GND (J102/12)
	7	WD2	(J102/P)	20	GND (J102/13)
	8	WD3	(J102/R)	21	GND (J102/14)
	9	WD4	(J102/S)	22	GND (J102/15)
	10	WD5	(J102/T)	23	GND (JJ02/16)
	11	WD6	(J102/P)	24	GND (J102/17)

	12	WD7	(J102/U)	25	GND (J102/18)
	13	NC			
CONNECTOR-3	1	RDP	(J103/1)	14	GND (J103/A)
	2	RDS	(J103/2)	15	GND (J103/B)
	3	NC		16	NC
	4	RD0	(J103/3)	17	GND (J103/C)
	5	RD1	(J103/4)	18	GND (J103/D)
	6	RD2	(J103/8)	19	GND (J103/J)
	7	RD3	(J103/9)	20	GND (J103/K)
	8	RD4	(J103/14)	21	GND (J103/R)
	9	RD5	(J103/15)	22	GND (J103/S)
	10	RD6	(J103/17)	23	GND (J103/U)
	11	RD7	(J103/18)	24	GND (J103/V)
	12	NC		25	NC
	13	NC			

NOTE: J101, J102 and J103 are PCB edge connectors on the Control and Data PCBs of the tape drive.

APPENDIX - G

I/O MAP AND UTILIZATION

1. 8255 II : I/O device at E0 (H)

   Control Word : 8A, Mode 0

   PA OUTPUT : PCLO OUTPUT

   PB INPUT : PCHI INPUT

PA0	OFF	PB0	DATA FLAG (PC0 E8(H))
PA1	REWIND	PB1	PARITY ERROR FLAG
PA2	SELECT	PB2	RDY
PA3	SWS	PB3	LDP
PA4	SFC	PB4	EOT
PA5	SRC	PB5	FPT
PA6	NOT USED	PB6	ON LINE
PA7	NOT USED	PB7	REWINDING
PC2	WARS CONTROL		PC0, PC1, PC4-PC7
PC3	WDS CONTROL		NOT USED

2. 8255 I : I/O device at E8 (H)

   Control Word : AF

   Mode 1 : PA - OUTPUT E8 (H)

   PB - INPUT E9 (H)

   PC3,4 - NOT USED

   PC6 - 10 KHz Strobe for data write.

   PC0 - Data Flag

   PC2 - RDS Read Strobe

3. 8253 : Timer at E4 (H)

   Counter 0 : Mode 3, divide by -5, Control Word 36.

Counter 1	:	Not used
Counter 2	:	Mode 2, divide by -31, Control Word B4 for 10 KHz strobe.

APPENDIX H

Sub-routine Addresses

2800 - 2C Initialization

2830 - 2855 Data write on tape calls; Block write 28AO
; Delay 2A20, Counter 10 KHzpulses
; Initialize 2810

2860 - 287F File gap and File Mark
Calls; file mark write 2880
; Delay 2A20 for counter 10 KHz
; Initialize 2800
; LRCC write (Part of it 288E)

2880 - 289A File Mark
Calls; Wait byte write at 28FO

28A0 - 28C3 Block Write
Calls; CRCC write 28DO
; LRCC write 288E
Part of File Mark

28DO - 28E2 CRCC Write

28FO - 28FA Wait byte write, wait for single pulse

2900 - 299F Blank

29AO - 29AA Rewind (Use after initialization only)

29BO - 2A00 Block Read

2A10 - 2A19 Initialization Calls (executable)

2A20 - 2A2E Delay counts 10 KHz pulses

2A30 - 2A41 Block Read and transfer to RAM 3000 (H)
byte 800 (H)

2A80 - 2AB2 CRCC Generate

2ACO - Set carry etc.

2AC8 Byte reverse

2ADO - 2AF9 Block and Memory write with CRCC

```
.L2800 2824
          *
.BL*
.L2800 2824      'INITIALISATION OF PORTS  & TIMERS

2800    3E8A      MVI A,8A    ;PORT A E0(H) INPUT,PORT B
2802    D3E3      OUT E3      ;OUTPUT,PC HI INPUT,PC LO OUTPUT,
2804    3EAF      MVI A,AF    ;PORT A E8 OUTPUT,PB INPUT MODE 1
2806    D3EB      OUT EB      ;MODE 1
2808    3EB4      MVI A,B4    ;COUNTER 2 MODE 2 8253
280A    D3E7      OUT E7      ;LODE LSB
280C    3E1F      MVI A,1F    ;31 DECIMAL,TO MSB
280E    D3E6      OUT E6      ;
2810    3E00      MVI A,00    ;00 TO MSB
2812    D3E6      OUT E6
2814    3E36      MVI A,36    ;COUNTER 0 IN MODE 3
2816    D3E7      OUT E7
2818    3E05      MVI A,05    ;05 TO LSB
281A    D3E4      OUT E4
281C    3E00      MVI A,00    ;00 TO MSB
281E    D3E4      OUT E4
2820    3E05      MVI A,05    ;ENABLE INTERRUPT OF PORT B E9
2822    D3EB      OUT EB      ;BIT SET PC2
2824    C9        RET

. *
.L2830 2855      'RECORD'

2830    31A020    LXI SP,20A0 ;INIT STACK
2833    CD0028    CALL 2800   ;CALL PORT TIMER INIT
2836    210030    LXI H,3000  ;MEM POINTER
2839    01FF07    LXI B,07FF  ;BYTE COUNTER
283C    3E18      MVI A,18    ;SWS & SFC TRUE
283E    D3E0      OUT E0
2840    11A801    LXI D,01A8  ;DELAY FOR 0.5 IN TAPE TRAVEL
2843    CD202A    CALL 2A20   ;COUNT 10 KHZ PULSES,424 NO
2846    CDA028    CALL 28A0   ;CALL BYTE WRITE
2849    113C00    LXI D,003C  ;60 DELAY LOOPS TO GIVE 0.1
284C    CD202A    CALL 2A20   ;IN TAPE TRAVEL
284F    3E00      MVI A,00    ;SWS & SFC FALSE
2851    D3E0      OUT E0      ;
2853    C3E003    JMP 03E0    ;BACK TO MONITIR

. *
.L2860 287F      'FILE MARK

2860    31A020    LXI SP,20A0 ;INIT STACK
2863    CD0028    CALL 2800   ;CALL INIT PORT INIT
2866    3E18      MVI A,18    ;SWS SFC TRUE
2868    D3E0      OUT E0
286A    11A80B    LXI D,0BA8  ;COUNT 2984 PULSES 10 KHZ
286D    CD202A    CALL 2A20   ;TO GIVE TAPE TRAVEL OF 3.5 IN
2870    CD8028    CALL 2880   ;CALL FILE MARK WRITE
2873    113C00    LXI D,003C  ;GAP OF 0.1 IN TAPE
2876    CD202A    CALL 2A20   ;
2879    3E00      MVI A,00    ;SWS SFC FALSE
287B    D3E0      OUT E0
287D    C3E003    JMP 03E0    ;OVER

. *
.L2880 289A      'WTITE FILE MARK'

2880    3E08      MVI A,08    ;WDS ON
2882    D3E2      OUT E2
2884    3E13      MVI A,13    ;FILE MARK CHAR
2886    D3E8      OUT E8      ;OUT
2888    CDF028    CALL 28F0   ;WAIT FOR HANDSHAKE
288B    110800    LXI D,0008  ;8 PULSES
288E    CD202A    CALL 2A20   ;DELAY
2891    3E04      MVI A,04    ;WARS ON
2893    D3E2      OUT E2      ;TO WRITW LRCC
2895    D3E8      OUT E8      ;DUMMY
2897    CDF028    CALL 28F0   ;WAIT HANDSHAKE
289A    C9        RET

. *
.L28A0 28C3                   ;BLOCK WRITE

28A0    3E08      MVI A,08    ;ENABLE WDS
28A2    D3E2      OUT E2
28A4    7E        MOV A,M     ;GET ONE BYTE DAY DATA
28A5    D3E8      OUT E8      ;OUTPUT
28A7    23        INX H       ;NEXT LOC
28A8    0B        DCX B       ;BYTE COUNT DECREMENT
28A9    78        MOV A,B
28AA    B1        ORA C       ;COUNT IN BC
28AB    F5        PUSH PSW    ;SAVE FLAGS
28AC    DBEA      IN EA       ;TEST INTERUPT FLAG
28AE    17        RAL         ;
28AF    D2AC28    JNC 28AC    ;WAIT FOR HAND SHAKE
28B2    F1        POP PSW     ;STATUS
28B3    C2A428    JNZ 28A4    ;OUT MORE BYTES?
28B6    3E00      MVI A,00    ;ELSE DISABLE WDS
28B8    D3E2      OUT E2      ;
28BA    CDD028    CALL 28D0   ;CALL WRITE CRCC
28BD    110400    LXI D,0004  ;WAIT FOR 4 WORD PULSES
28C0    CD8E28    CALL 288E   ;THEN WRITE LRCC
28C3    C9        RET

. *
.L28D0 28E2          'CRCC WRITE'

28D0    110400    LXI D,0004 ;WAIT 4 PULSES
28D3    CD202A    CALL 2A20
28D6    3E08      MVI A,08    ;ENABLE WDS
28D8    D3E2      OUT E2
28DA    3AB520    LDA 20B5    ;GET CRCC DATA
28DD    D3E8      OUT E8      ;OUTPUT CRCC
28DF    CDF028    CALL 28F0   ;WAIT PULSE THEN OFF
28E2    C9        RET

. *
.L28F0 28FA       'WAIT PULSE END  AND OFF '

28F0    DBEA      IN EA       ;TEST INTERRUPT LINE
28F2    17        RAL
28F3    D2F028    JNC 28F0    ;LOOP FOR IT
28F6    3E00      MVI A,00    ;WDS AS WELL AS WARS
28F8    D3E2      OUT E2      ;OFF
.L2910 2917       'INIT SOU'
```

APPENDIX-I

```
.L29A0 29A9          'REWIND'

29A0    3E02        MVI A,02    ;OUT 1
29A2    D3E0        OUT E0
29A4    3E00        MVI A,00    ;THEN 0
29A6    D3E0        OUT E0      ;FOR REWIND PULSE
29A8    C3E003      JMP 03E0

. *
. *
.L29B0 292A00        'READ BLOCK HL MEM POINTER COUNT
                         RETURNED IN BC
29B0    D5          PUSH D      ;SAVE REGS
29B1    E5          PUSH H
29B2    0E00        MVI C,00    ;INIT C TO 00
29B4    3E10        MVI A,10    ;SFC IS TRUE
29B6    D3E0        OUT E0
29B8    110008      LXI D,0800  ;DELAY
29BB    CDF105      CALL 05F1
29BE    DBE9        IN E9       ;READ ONCE ,DUMMY
29C0    1600        MVI D,00    ;
29C2    14          INR D       ;INCREMENT D
29C3    7A          MOV A,D     ;D TO A
29C4    FEF0        CPI F0      ;LOOP FO H TIMES
29C6    C2CA29      JNZ 29CA    ;IF NOT THEN SKIP
29C9    15          DCR D       ;D=D-1
29CA    DBE1        IN E1       ;READ FLAG
29CC    1F          RAR
29CD    D2C229      JNC 29C2    ;WAIT FOR RDS HANDSHAKE
29D0    1F          RAR
29D1    D2D629      JNC 29D6    ;TEST PARITY FLAG,IF PAR ERR
29D4    0E01        MVI C,01    ;REG C WILL HAVE 1
29D6    DBE9        IN E9       ;READ NORMAL
29D8    77          MOV M,A     ;STORE IN RAM
29D9    23          INX H       ;NEXT LOC
29DA    7A          MOV A,D     ;TRIAL COUNT
29DB    FE0D        CPI 0D      ;13
29DD    DAC029      JC 29C0     ;LESS THAN 13,THEN READ AGAIN
29E0    FE50        CPI 50      ;LESS THAN 50
29E2    D2C029      JNC 29C0    ;MORE THAN 50 THEN READ
29E5    115700      LXI D,0057  ;INTERMEDIATE VALUE
29E8    CDF105      CALL 05F1   ;DELAY
29EB    3E00        MVI A,00    ;SFC IS FALSE
29ED    D3E0        OUT E0
29EF    116414      LXI D,1464  ;MORE DELAY
29F2    CDF105      CALL 05F1
29F5    D1          POP D       ;HL DATA IN DE
29F6    D5          PUSH D      ;SAVE
29F7    CD510F      CALL 0F51   ;HL-DE IN BC,COUNT OF BYTES READ
29FA    C5          PUSH B      ;READ
29FB    79          MOV A,C     ;PAR FLAG
29FC    1F          RAR         ;TO CARRY
29FD    C1          POP B       ;
29FE    E1          POP H
29FF    D1          POP D
2A00    C9          RET

.
 *
.
 *
.
 *
```

```
29F8    D3E2        OUT E2      ;OFF
.L2A10 2A19          'INIT CALL'

2A10    31A020      LXI SP,20A0
2A13    CD0028      CALL 2800
2A16    C3E003      JMP 03E0

2A19    FF          RST 7

. *
.L2A20 2A2E          'DELAY BY PULSE COUNT '

2A20    D3E8        OUT E8      ;DUMMY OUT FOR FLAG
2A22    DBEA        IN EA       ;TEST INTERRUPT FLAG
2A24    17          RAL         ;BIT IN CARRY
2A25    D2222A      JNC 2A22    ;LOOP FOR FLAG
2A28    1B          DCX D       ;COUNT DE REG
2A29    7A          MOV A,D     ;FOR EACH PULSE
2A2A    B3          ORA E       ;
2A2B    C2202A      JNZ 2A20    ;TEST AND COUNT NEXT PULSE
2A2E    C9          RET

. *
.L2A30 2A3F          'BLOCK READ'    MAIN

2A30    31A020      LXI SP,20A0 ;INIT STACK
2A33    CD0028      CALL 2800   ;INIT POI       &TIMER
2A36    210030      LXI H,3000  ;RAM POINTER
2A39    01FF07      LXI B,07FF  ;BYTE COUNT OPTIONAL
2A3C    CDB029      CALL 29B0   ;CALL BLOCK READ
2A3F    C3E003      JMP 03E0    ;END

. *
 *
.
.
.
. *
. *
.L2AD0 2AF9          'BLOCK WRITE'  MAIN

2AD0    31A020      LXI SP,20A0 ;INIT STACK
2AD3    CD0028      CALL 2800   ;INIT PORT TIMER
2AD6    210030      LXI H,3000  ;DATA SOURCE POINTER
2AD9    010004      LXI B,0400  ;BYTE COUNT
2ADC    CDB02A      CALL 2A80   ;CALL CRCC GENERATE
2ADF    3E18        MVI A,18    ;SWS SFC TRUE
2AE1    D3E0        OUT E0
2AE3    11A801      LXI D,01A8  ;0.5 IN TAPE TRAVEL
2AE6    CD202A      CALL 2A20   ;BY DELAY
2AE9    CDA028      CALL 28A0   ;CALL BLOCK WRITE
2AEC    113C00      LXI D,003C  ;DELAY 0.1 IN TAPE
2AEF    CD202A      CALL 2A20   ;TRAVEL
2AF2    3E00        MVI A,00    ;SWS    SFC OFF
2AF4    D3E0        OUT E0      ;END
2AF6    C3E003      JMP 03E0

2AF9    FF          RST 7

.
```

```
L2A80 2ACF      'CRCC GENERATE HL MEM POINTER BC BYTE
                      COUNTER
2A80    C5      PUSH B          ;SAVE
2A81    D5      PUSH D
2A82    E5      PUSH H
2A83    110000  LXI D,0000      ;INIT DE 0000
2A86    7E      MOV A,M         ;GET BYTE ONE
2A87    B7      ORA A           ;NO CHANGE
2A88    37      STC             ;SET CARRY
2A89    3F      CMC             ;CARRY=0
2A8A    3E00    MVI A,00        ;A=00
2A8C    ECC02A  CPE 2AC0        ;SET CARRY TO 1 FOR PAR EVEN
2A8F    AA      XRA D           ;XOR TO D REG
2A90    1F      RAR             ;ROTATE RIGHT WITH CARRY
2A91    F5      PUSH PSW        ;SAVE STATUS
2A92    7E      MOV A,M         ;GET BYTE AGAIN
2A93    AB      XRA E           ;NOW XOR TO E REG
2A94    5F      MOV E,A         ;SAVE IT BACK IN E REG
2A95    F1      POP PSW         ;RESTORE FLAGS
2A96    7B      MOV A,E         ;OLD DATA BACK IN A
2A97    1F      RAR             ;ROTATE RIGHT
2A98    1600    MVI D,00        ;D=00
2A9A    DCC82A  CC 2AC8         ;IF CARRY =1,XOR TO 3C,D=01
2A9D    5F      MOV E,A         ;SAVE IN E REG
2A9E    23      INX H           ;NEXT LOC
2A9F    0B      DCX B           ;COUNT BYTE
2AA0    78      MOV A,B
2AA1    B1      ORA C
2AA2    C2862A  JNZ 2A86        ;REPEAT IF MORE DATA
2AA5    7A      MOV A,D         ;GET DATA IN D REG
2AA6    EE01    XRI 01          ;INVERT BIT 0,IT IS PAR OF CRCC
2AA8    32B620  STA 20B6        ;STORE AT 20B6 (H)
2AAB    7B      MOV A,E         ;GET DATA IN E REG
2AAC    EED7    XRI D7          ;INVERT BITS 0 1 2 4 6 7
2AAE    32B520  STA 20B5        ;STORE CRCC I AT 20B5(H)
2AB1    E1      POP H
2AB2    D1      POP D
2AB3    C1      POP B
2AB4    C9      RET
 *
.L2AC0 2ACF       'SET CARRY TO 1 AND A REG 01

2AC0    37      STC
2AC1    3E01    MVI A,01
2AC3    C9      RET

2AC4    FF      RST 7

2AC5    FF      RST 7

2AC6    FF      RST 7

2AC7    FF      RST 7
                      'XOR TO 3C(H) INIT D TO 01
2AC8    EE3C    XRI 3C
2ACA    1601    MVI D,01
2ACC    C9      RET
```

HEX DUMP

D2800 2AFF

```
2800 3E 8A D3 E3 3E AF D3 EB 3E B4 D3 E7 3E 1F D3 E6
2810 3E 00 D3 E6 3E 36 D3 E7 3E 05 D3 E4 3E 00 D3 E4
2820 3E 05 D3 EB C9 FF FF FF FF FF FF FF FF FF FF FF
2830 31 A0 20 CD 00 28 21 00 30 01 FF 07 3E 18 D3 E0
2840 11 A8 01 CD 20 2A CD A0 28 11 3C 00 CD 20 2A 3E
2850 00 D3 E0 C3 E0 03 FF FF FF FF FF FF FF FF FF FF
2860 31 A0 20 CD 00 28 3E 18 D3 E0 11 A8 0B CD 20 2A
2870 CD B0 28 11 3C 00 CD 20 2A 3E 00 D3 E0 C3 E0 03
2880 3E 08 D3 E2 3E 13 D3 E8 CD F0 28 11 08 00 CD 20
2890 2A 3E 04 D3 E2 D3 E8 CD F0 28 C9 FF FF FF FF FF
28A0 3E 08 D3 E2 7E D3 E8 23 0B 78 B1 F5 DB EA 17 D2
28B0 AC 28 F1 C2 A4 28 3E 00 D3 E2 CD D0 28 11 04 00
28C0 CD BE 28 C9 FF FF FF FF FF FF FF FF FF FF FF FF
28D0 11 04 00 CD 20 2A 3E 08 D3 E2 3A B5 20 D3 E8 CD
28E0 F0 28 C9 FF FF FF FF FF FF FF FF FF FF FF FF FF
28F0 DB EA 17 D2 F0 28 3E 00 D3 E2 C9 FF FF FF FF FF
2900 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2910 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2920 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2930 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2940 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2950 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2960 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2970 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2980 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2990 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
29A0 3E 02 D3 E0 3E 00 D3 E0 C3 E0 03 FF FF FF FF FF
29B0 D5 E5 0E 00 3E 10 D3 E0 11 00 08 CD F1 05 DB E9
29C0 16 00 14 7A FE F0 C2 CA 29 15 DB E1 1F D2 C2 29
29D0 1F D2 D6 29 0E 01 DB E9 77 23 7A FE 0D DA C0 29
29E0 FE 50 D2 C0 29 11 57 00 CD F1 05 3E 00 D3 E0 11
29F0 64 14 CD F1 05 D1 D5 CD 51 0F C5 79 1F C1 E1 D1
2A00 C9 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2A10 31 A0 20 CD 00 28 C3 E0 03 FF FF FF FF FF FF FF
2A20 D3 E8 DB EA 17 D2 22 2A 1B 7A B3 C2 20 2A C9 FF
2A30 31 A0 20 CD 00 28 21 00 30 01 FF 07 CD B0 29 C3
2A40 E0 03 FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2A50 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2A60 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2A70 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
2A80 C5 D5 E5 11 00 00 7E B7 37 3F 3E 00 EC C0 2A AA
2A90 1F F5 7E AB 5F F1 7B 1F 16 00 DC C8 2A 5F 23 0B
2AA0 78 B1 C2 86 2A 7A EE 01 32 B6 20 7B EE D7 32 B5
2AB0 20 E1 D1 C1 C9 FF FF FF FF FF FF FF FF FF FF FF
2AC0 37 3E 01 C9 FF FF FF FF EE 3C 16 01 C9 FF FF FF
2AD0 31 A0 20 CD 00 28 21 00 30 01 00 04 CD 80 2A 3E
2AE0 18 D3 E0 11 A8 01 CD 20 2A CD A0 28 11 3C 00 CD
2AF0 20 2A 3E 00 D3 E0 C3 E0 03 FF FF FF FF FF FF FF
 *
 *
 *
```

APPENDIX J

LIST OF COMPONENTS

Integrated Circuits

1.	U1, U5, U8	7414
2.	U2	7474
3.	U3	7400
4.	U4	7404
5.	U6, U9	8255
6.	U7, U16	DM8220
	PARITY GENERATOR CHECKER	
7.	U10	Free Socket
8.	U11	7410
9.	U12, U15, U17	7416
10.	U13	8253
11.	U14	74LS138
12.	U18	74LS245

Resistors

1. R1 = 330 Ohms
2. R2 = 220 Ohms

Capacitors

1. C1, C3 0.1 MF Ceramic
2. C2 10 MF10V TANTALUM

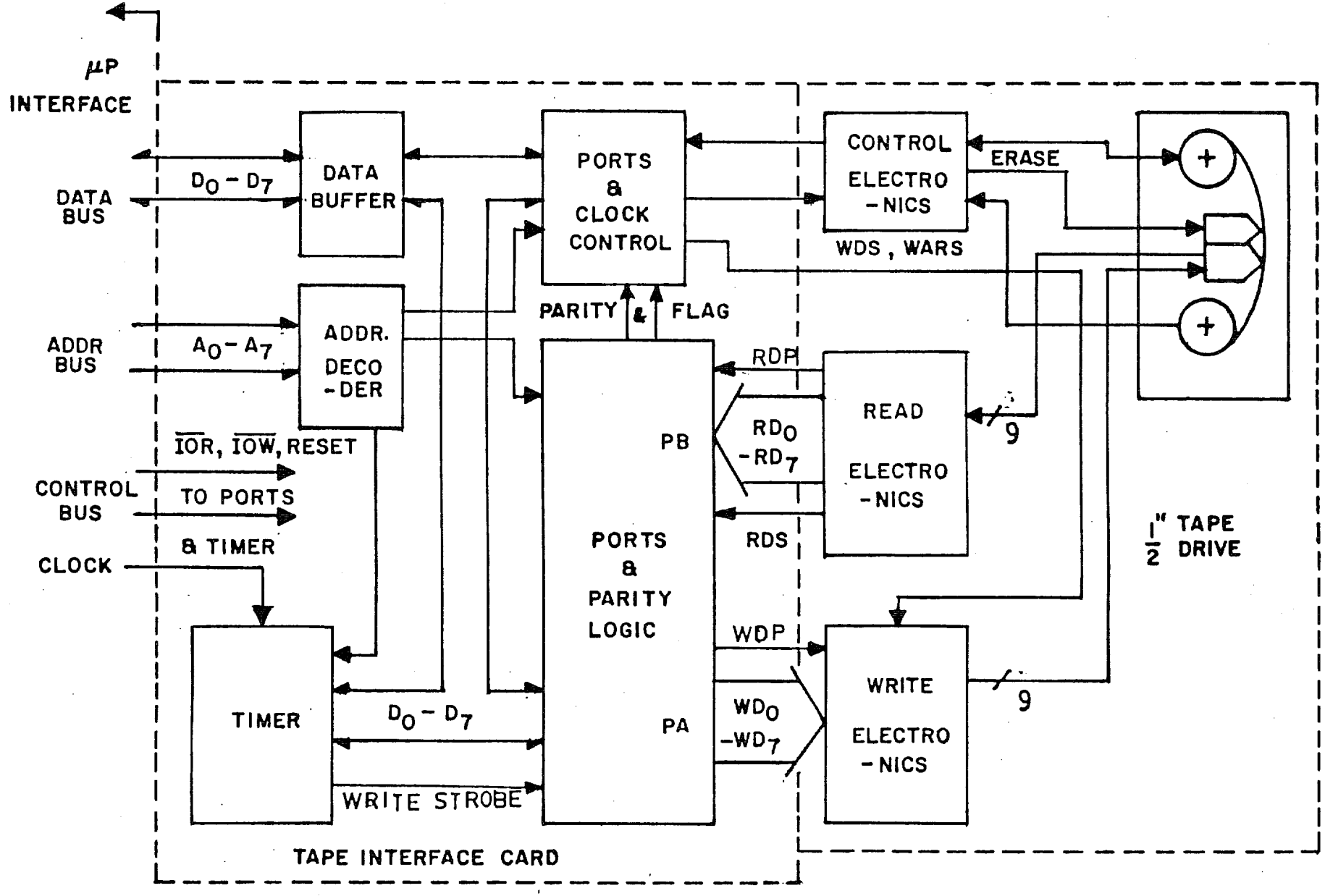


FIG. 1 BLOCK DIAGRAM OF MAGNETIC TAPE INTERFACE

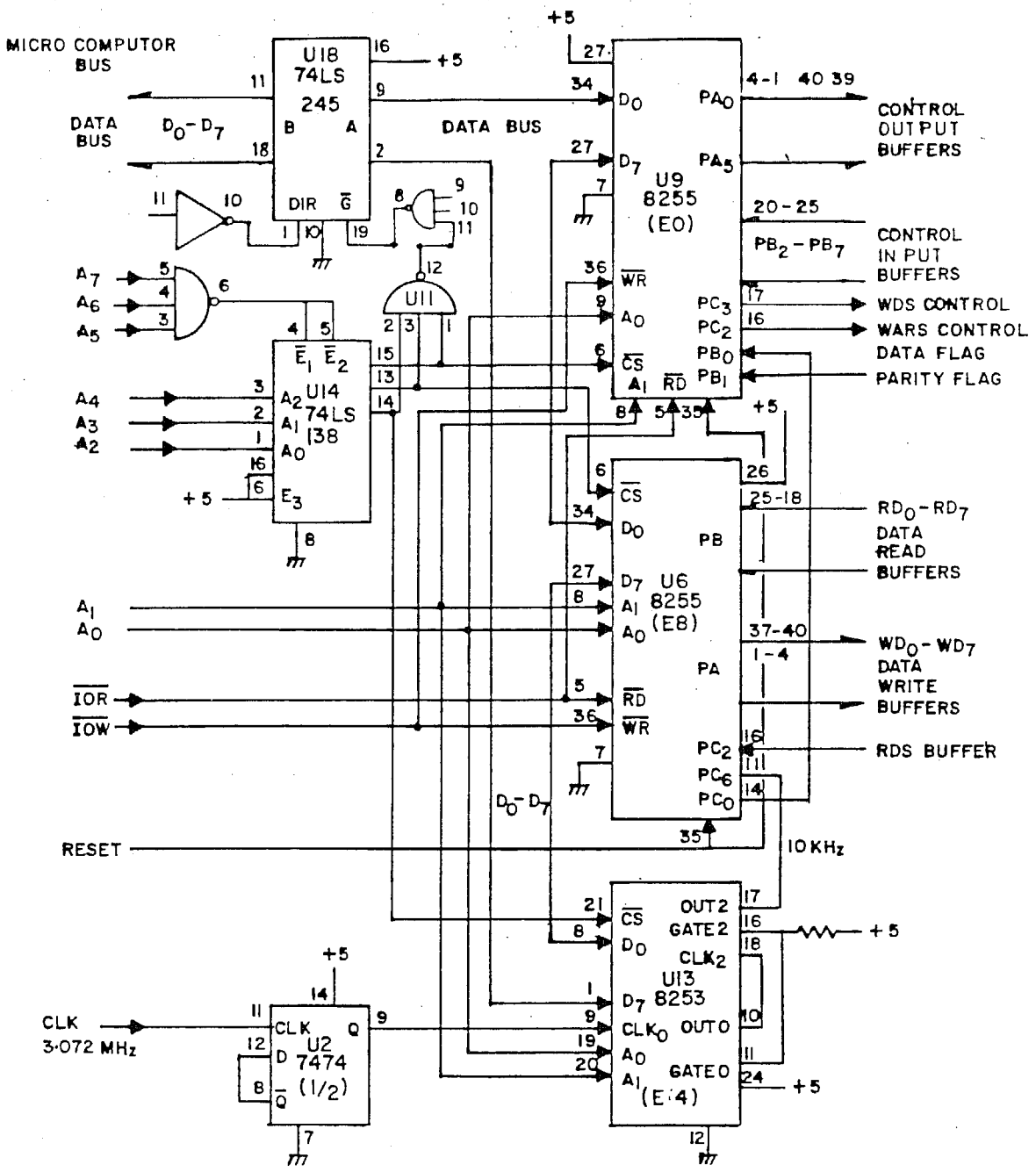


FIG. 2 CIRCUIT DIAGRAM OF CONTROLLER PORTS AND TIMER

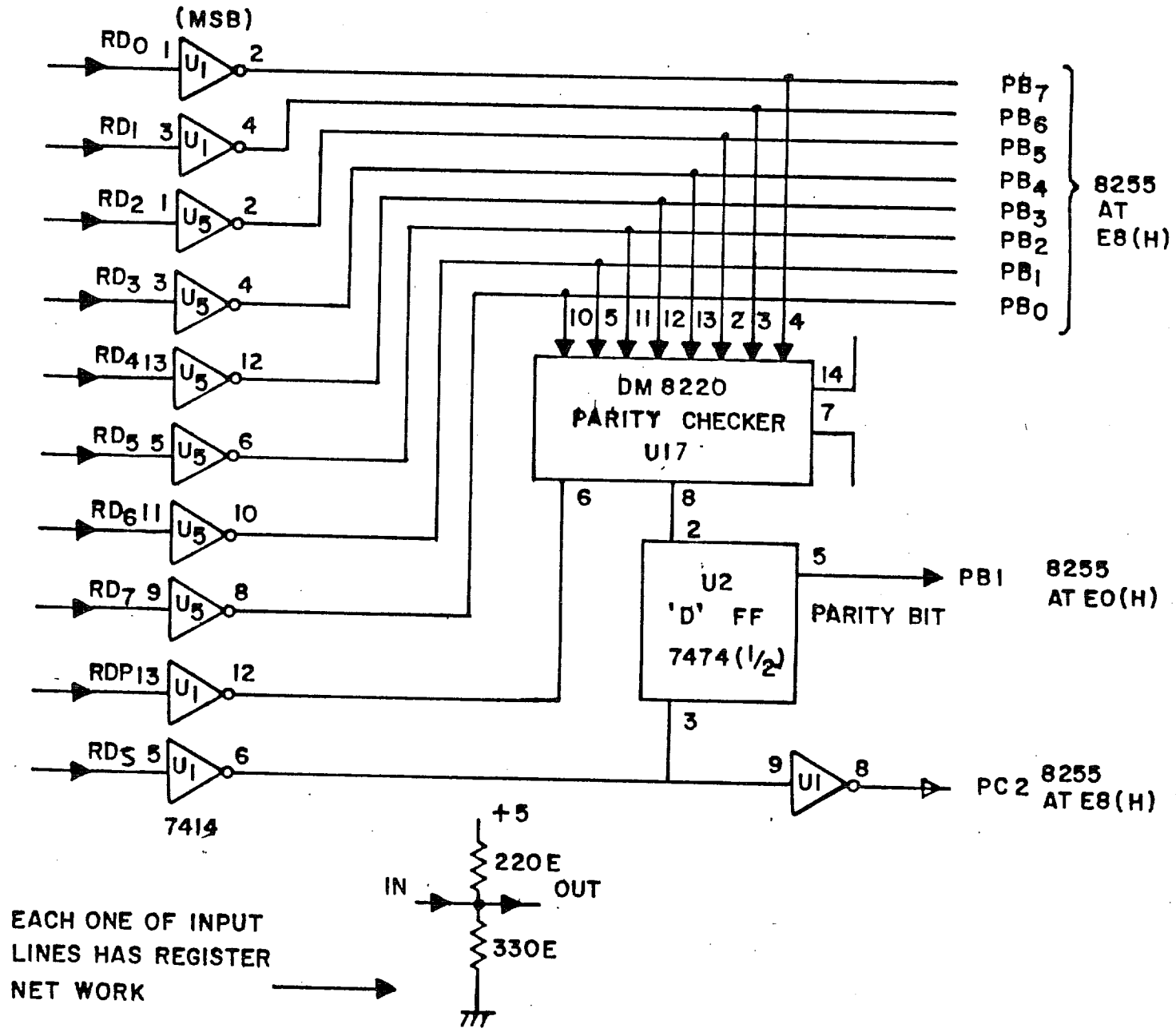


FIG. 3 DATA READ BUFFER & PARITY LOGIC

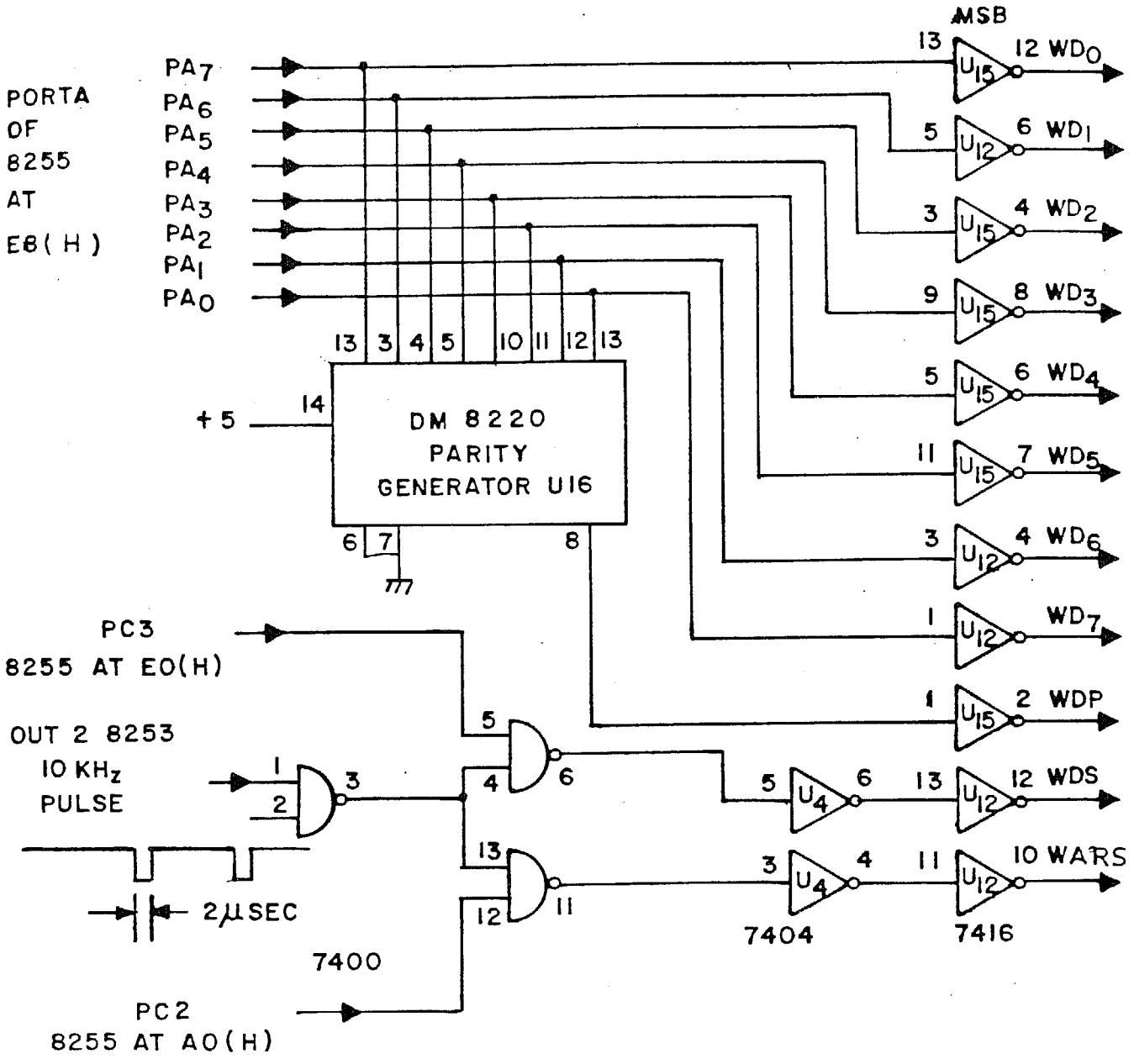


FIG. 4. WRITE BUFFERS, PARITY AND WDS, WARS STROBE LOGIC

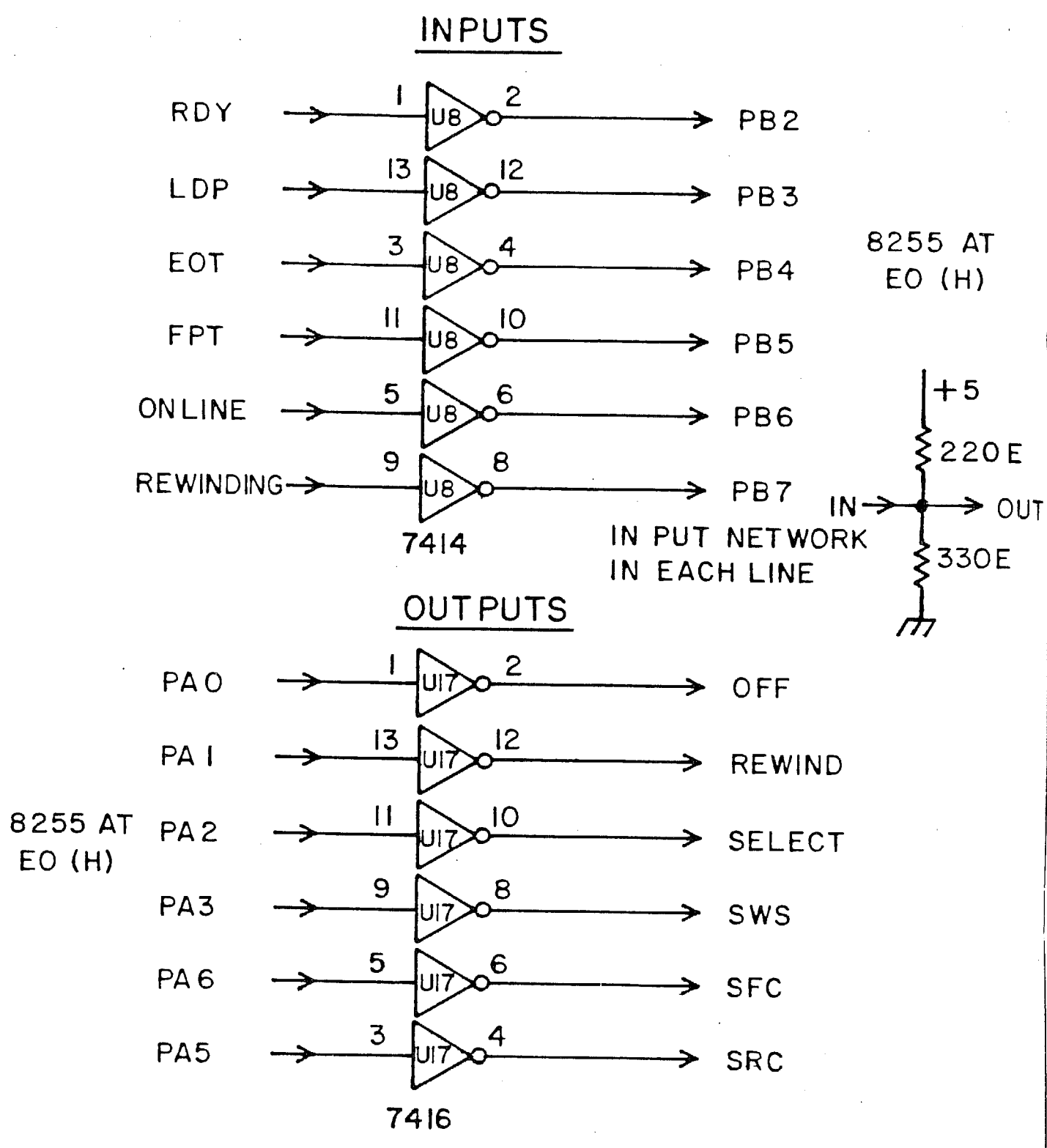


Fig. 5 CONTROL AND STATUS BUFFERS

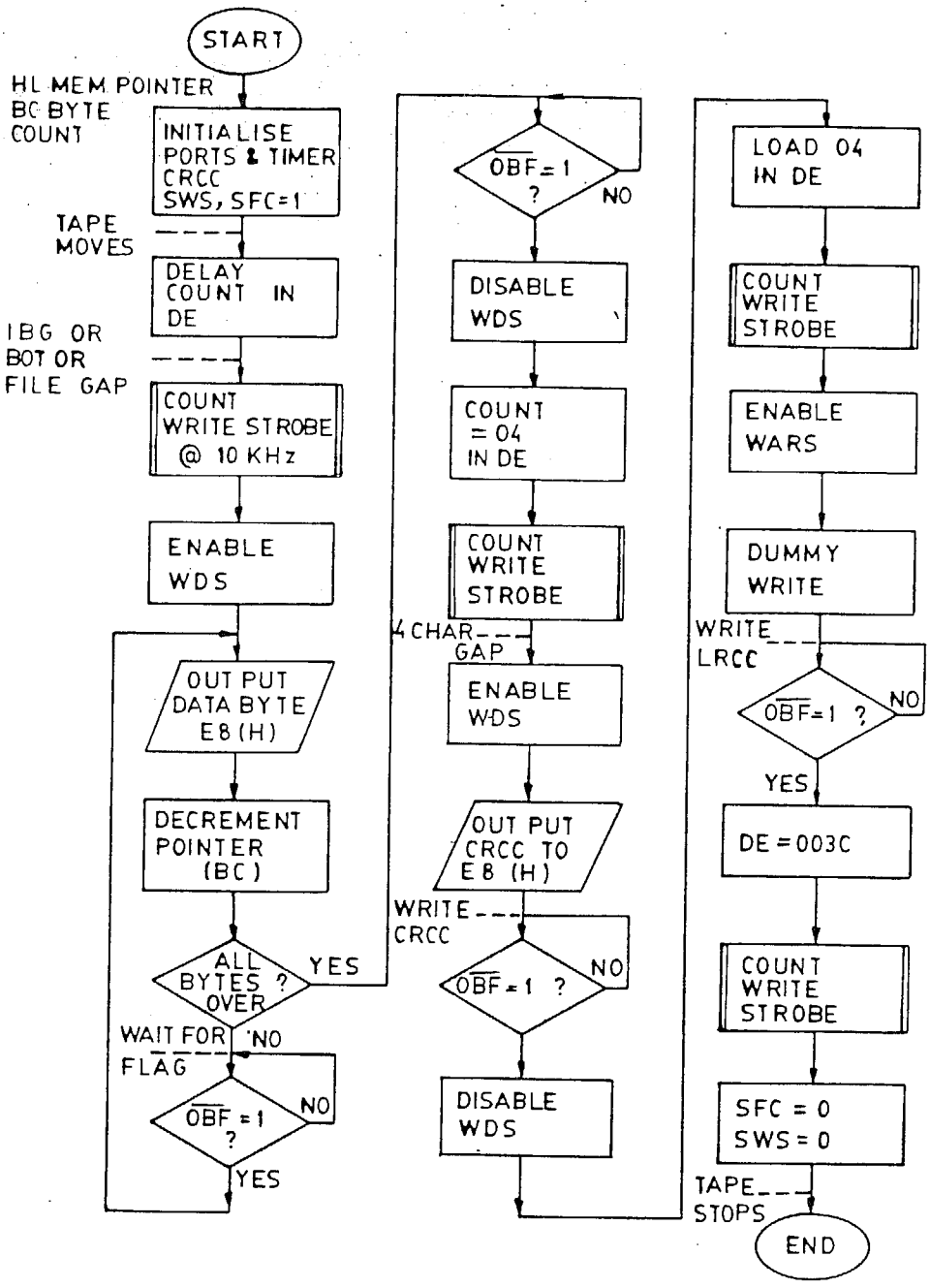


FIG-6 FLOW CHART OF BLOCK WRITE

'BLOCK READ'

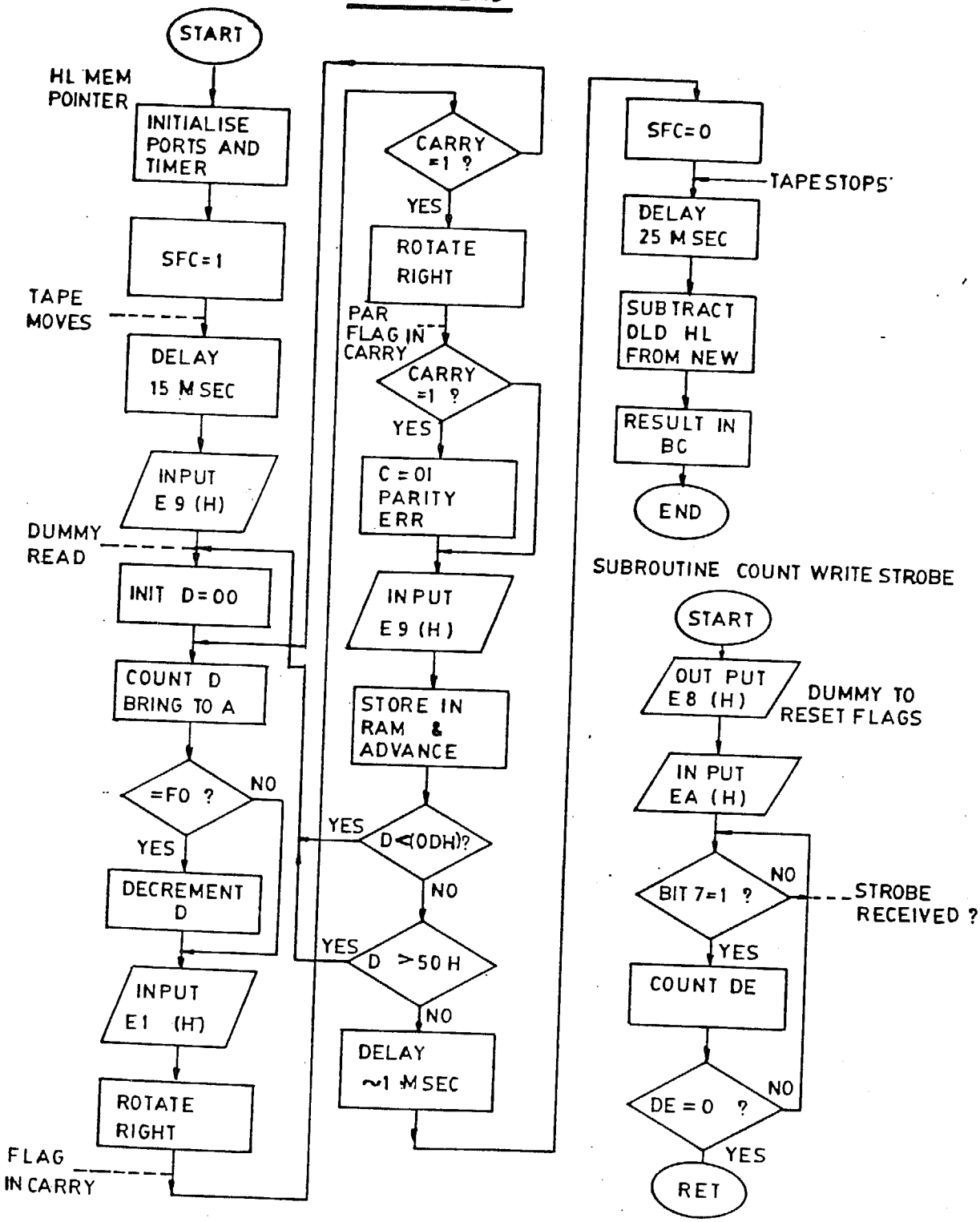


FIG.- 7

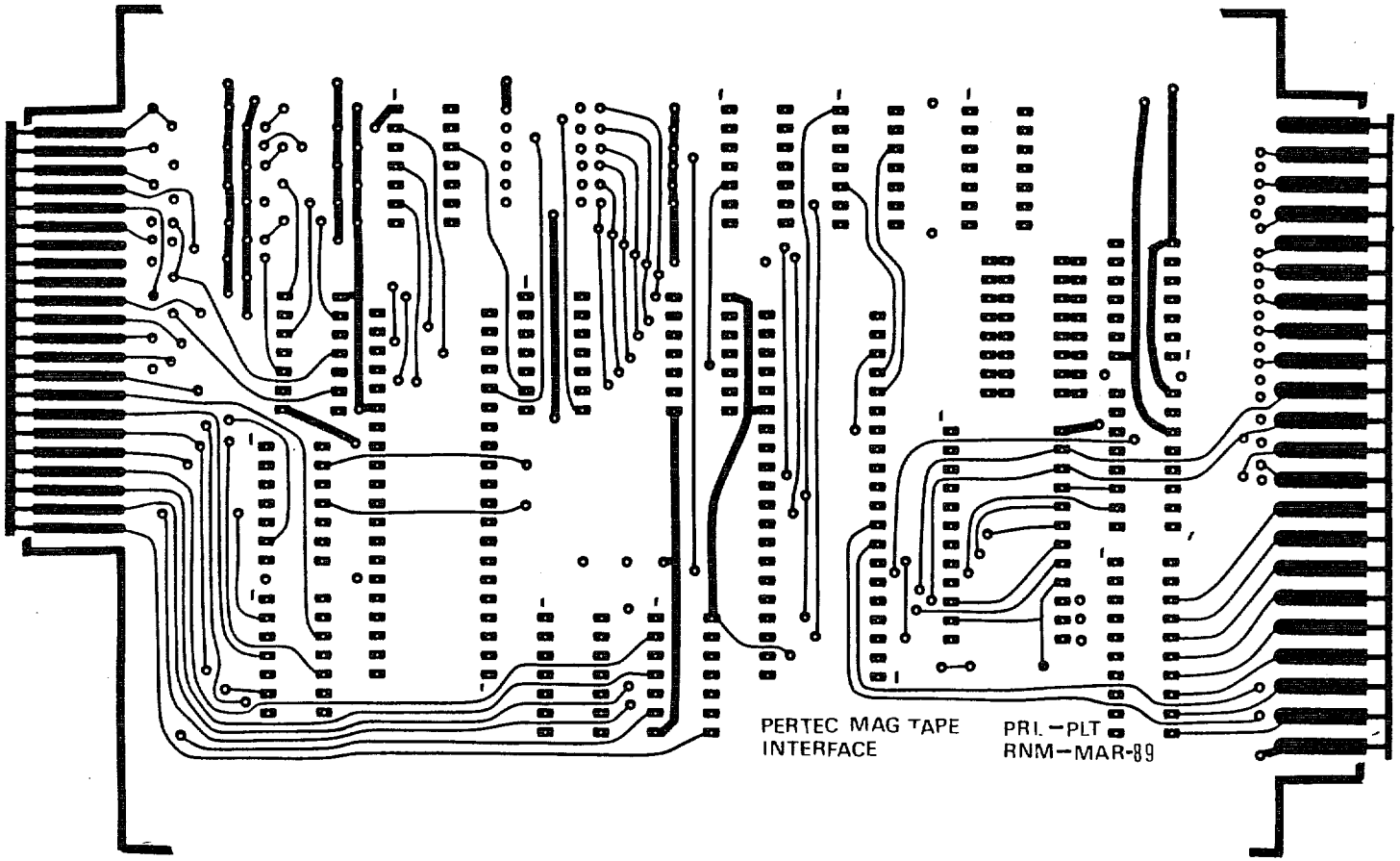
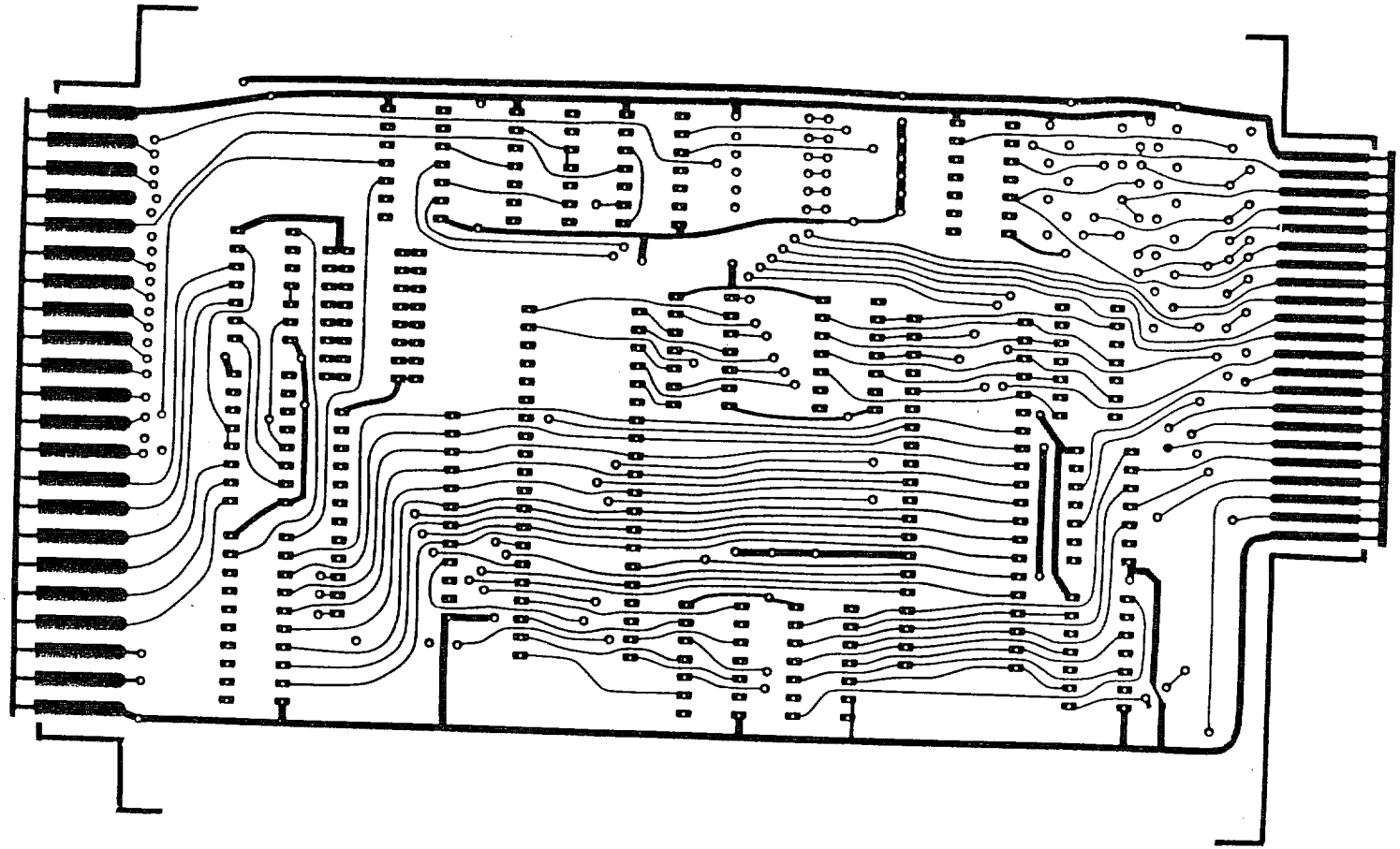
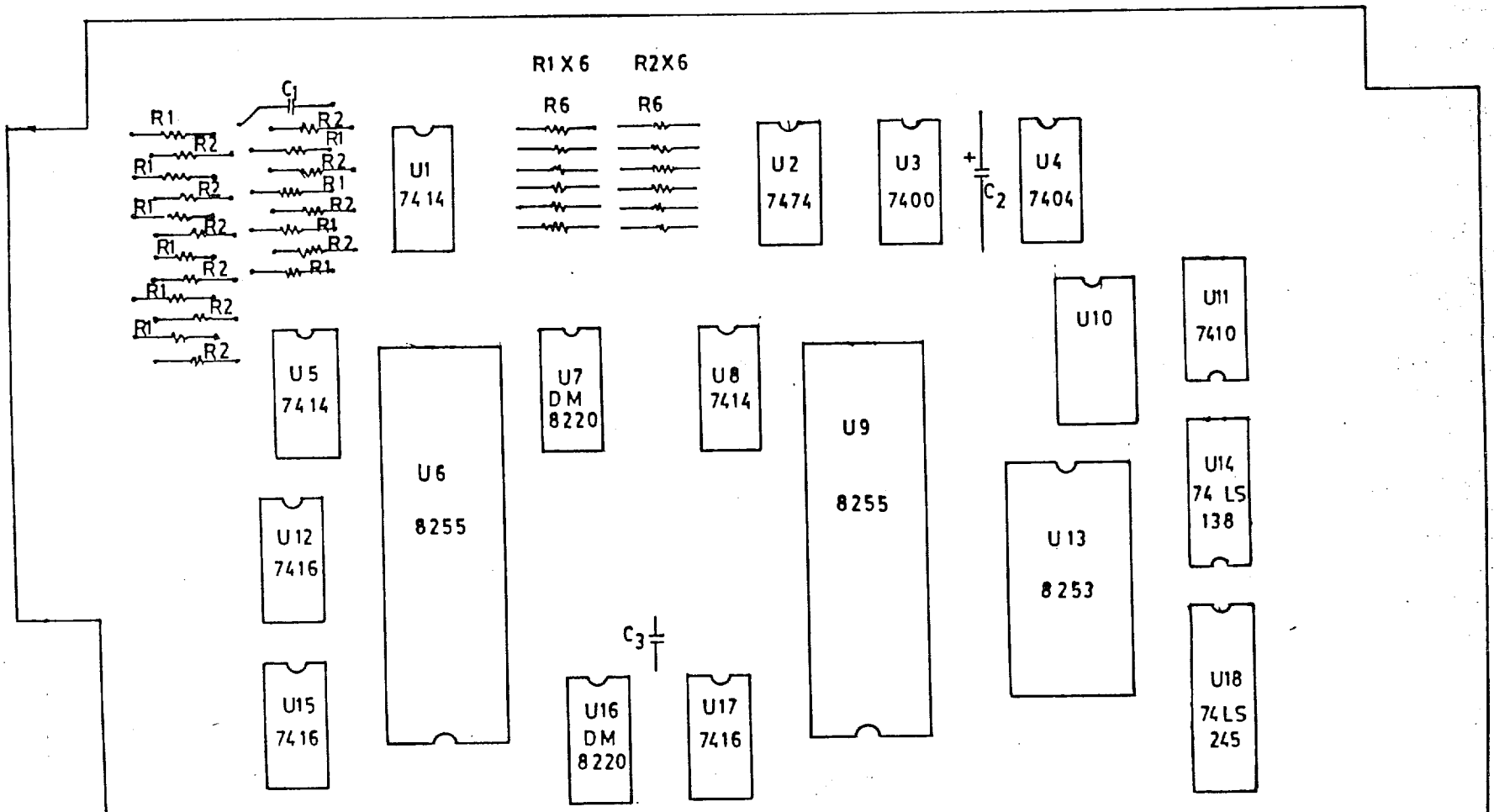


FIGURE 8 COMPONENT SIDE



SOLDER SIDE



R2 220E R1 330 E C1 , C3 0·1μ C2-10 μ

FIG.-9. PLACEMENT OF PARTS