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MICROPROCESSOR-BASED DIGITAL DATA ACQUISITION SYSTEM FOR THREE SITE IPS EXPERIMENT

By

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MICROPROCESSOR-BASED DIGITAL DATA ACQUISITION SYSTEM FOR THREE SITE IPS EXPERIMENT

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Abstract:

Under the automation programme of three site Interplanetary Scintillation experiment, the microprocessor/microcomputer based digital data acquisition system each for Thaltej, Surat and Rajkot has been developed and described here. The system hardware consists of microprocessor based dedicated front end system and an IBM XT compatible microcomputer for data and program storage. Menu based system operation is made extremely simple and data file for each radio source observed is created. The addition of modems will enhance the capability of remote job entry and real time data transportation.

1.0 Introduction:

Digital data acquisition system based on discrete technology has been operational at all three radio telescope sites of inter-planetary scintillation experiment for quite some time now. The present system under discussion has been developed to update the technology keeping in view the following considerations:

1. System reliability
2. Operational simplicity

3. System flexibility

4. Future requirement of observing more sources simultaneously

The use of PC/XT microcomputer provides necessary system reliability as this technology has withstood the test of time. The operational simplicity comes from the fact that the operation is menu-driven and observations can be programmed in advance for several sources. The sampling frequency at present is kept at 20 Hz but can be varied through software and hence provides flexibility. The system can be extended to monitor more receivers and hence extensible.

2.0 System Description:

The data acquisition system in its most elementary form is shown in Figure 1. It has an IBM XT compatible microcomputer and a separate microprocessor-based dual channel Analog to Digital Converter (ADC) system. The IBM XT computer with its 640 Kbyte RAM was the obvious choice as it provided very good environment for hardware and software development. It communicates with the ADC system through the serial I/O port. The microprocessor-based ADC system has a Z-80 processor, its associated memory, peripheral chips, 12-bit A/D, timer/counters, multiplexer, sample and hold, etc.

2.1 Microprocessor-based ADC:

Figure 2 shows the block diagram of microprocessor-based ADC system. This consists of a Z-80 microprocessor running

at 2 MHz. It has 16 Kbyte of EPROM and 16 Kbyte of RAM. Two Intel's 8251 ICs provide 2 serial channels for communication. Two programmable timer/counter ICs namely Intel's 8253 provide 6 timer/counters each having 16-bit count register. The output of the two counters are used as clocks to the serial channels. Therefore the baud rate of these channels can be changed by programming the corresponding counters. Two other timers are cascaded to derive 1 Hz from 50 kHz. The 1 Hz output is used as non maskable interrupt (NMI) to the CPU. A fifth timer is used to generate the required sampling frequency. This output is connected to the interrupt (INT) of CPU so that the sequence of operation such as sample, convert, read, store etc. can be carried out under software control. A 12 bit analog to digital converter is used to digitise the two outputs of correlation receiver using sample and hold and an analog multiplexer. A parallel I/O IC 8255 reads the data from A/D as well as provides the control signals for S/H, multiplexer and A/D. Another 8255 is used for outputting 8 bit code for the selection of appropriate antenna beam by beam selector unit.

2.2 Circuit Detail:

This section describes the circuit of the microprocessor-based analog to digital converter and explains the function in detail. The circuit is fabricated on a single PCB of 12" x 8". All connections to the external components are taken through 44 pin edge connector. The PCB along with its power supply is housed in 19" chassis with a flip cover and is suitable for

rack mounting. The circuit is powered by a custom built power supply of following rating:

1.	Input	:	230V AC
2.	Outputs	:	+ 5V @ 1.5 amps
		:	+15V @ 0.25 amps
		:	-15V @ 0.25 amps

The +15V and -15V supplies are required for A/D module. The +12V and -12V required for RS-232 C interface are obtained using onboard regulators.

2.2.1 Microprocessor and memory circuit:

The microprocessor circuit is designed around a Z-80 microprocessor operating on a single power supply and external clock. The instruction set is a superset of Intel's 8080 or 8085 microprocessor with the exception of three RST and RIM, SIM instructions. Figure 3 shows the circuit diagram of microprocessor and its connections with memory. The 74LS373 ICs are used for buffering 16 address lines and a 74LS245 IC for buffering 8 data lines. The read, write, memory request and I/O request signals are buffered by the gates of 74LS32. A 74LS138 decodes the most significant three address lines along with memory request to provide 8 chip select signals for each 8 Kbyte memory device. The memory consists of 16 Kbyte EPROM using two 2764 ICs and 16 Kbyte RAM using two HM6264 ICs. The EPROM occupies address space from 0000 to 3FFF hex and

the RAM occupies the address space from 4000 to 7FFF hex. Figure 5a shows an 8 MHz oscillator made using three inverters of 74LS06. This frequency is further divided by a 4 bit counter 74LS93 to get 2 MHz and 1 MHz clocks for CPU and timer/counters respectively. The reset signals RST and RST are generated for various circuits and are activated by a push button on the front panel.

2.2.2 Counter/Timers and serial interface:

Figure 4 shows the devices for counter/timers and serial I/O interfaces. A 74LS138 decodes the address line A3 through A7 along with I/O request to select the I/O devices. Two 8253 ICs provide 6, 16 bit counters for generating various timing signals. The input to the first timer comes from either 1 MHz clock generated onboard or 50 kHz output of an external IST clock. This timer is programmed to divide this clock and generate 1 kHz output. The second counter further divides this clock to generate 1 Hz pulses. This 1 Hz pulse is given to the non maskable Interrupt of the CPU. The service routine for this interrupt is a software driven clock. For IPS observations it is very important to synchronise this software clock with the IST clock as the observations are to be carried out simultaneously at three stations separated by approximately 200 kms. The identical IST clocks at all the three stations are synchronised with the ATA timing signals within ±5 msec accuracy. The software clock synchronised with the IST clock

will also provide relatively same accuracy at all the stations. The synchronisation with IST clock is achieved using 1 minute pulse output of IST clock. The minute pulse output is logic "high" during the odd minute and logic "low" during the even minute intervals. As shown in Figure 5b the leading and the trailing edge of this pulse is used to generate narrow pulses at every transition of a minute. This pulse is used to set the flipflop 74LS107 whose output controls the gates of timers. Prior to synchronisation the flipflop is cleared using one of the output lines of 8255 (parallel I/O) forcing the gate inputs low thereby inhibiting the timers. Subsequent minute transition pulse enables the counters.

The 1 kHz output of the first timer is also fed to the fourth timer and is appropriately divided to generate the required sampling frequency. In the present case the sampling interval is 48 msec ($\sim$20 Hz) to keep it identical with the old data acquisition system. The output of this timer is connected with the interrupt of the CPU. The service routine then carries out sequence of operations to digitise the two channels and loads the data in register or memory.

The circuit also has two serial communication interfaces using Intel's two Universal Asynchronous/synchronous Receiver-Transmitter ICs 8251. The timers five and six generate the required baud rate clocks from 1 MHz clock so that the baud rate of the two channels can be set independently. MC1488 line driver ICs are used for generating RS 232-C signal levels from TTL outputs of 8251. Similarly the receiver ICs MC1489 convert the input signal levels to TTL level.

2.2.3 Dual Channel A/D Converter and Parallel Interface:

Figure 6 shows A/D converter and parallel I/O interface for digitising and transferring data to CPU/memory. The analog signals known as "SIN" and "COS" are received from the correlation receiver. The analog signals pass through separate unity gain amplifiers made of operational amplifier LM324. The outputs of these amplifiers are given to the Sample and hold (S/H) circuit ICs 0023 of National Semiconductors as both the channels are to be sampled simultaneously. The offset trimmers are used to set zero output for zero input. The sampled signal of both the channels go to a 2 to 1 analog multiplexer IC 0014 of National Semiconductors. The output of the multiplexer is connected to the input of a 12 bit A/D converter module EH12B of Datel. Thus two channels are digitised alternately. The A/D is used in a bipolar mode for analog input in the range +5 to -5 volts. The offset and gain adjustment are provided to achieve linearity in the output.

The parallel interface consists of two programmable parallel I/O chips 8255 of Intel. The port A (8 bits) and Port b (4 msbits) of first 8255 are connected to the outputs of A/D. The lower half of the port C is used as various control lines to S/H, multiplexer, A/D and synchronisation circuit described in section 2.2.2. The upper half of the port C is used as input to get status of A/D. The second 8255 is only partially used, the port A is used for outputting the beamcode which will be used by beam selector unit to select appropriate antenna beam to point to the radio source under observation.

2.3 The Microcomputer:

The IBM PC/XT microcomputer technology is synonymous with versatility and reliability. The open ended architecture has led to large-scale manufacturing of clones and add-ons. But the better advantage is in the availability of software and software tools. Therefore the IBM XT compatible computer is selected to support the function of data acquisition, processing and transportation of data. The system configuration is given in Appendix A. The computer communicates with the ADC system through the asynchronous communication interface.

3. Software:

The software is discussed in two parts, first the software for the microprocessor-based ADC. The EPROM resident software in this system consists of a monitor and several other routines to support data acquisition. The monitor provides some simple commands to examine memory, alter memory, execute programmes etc. It also provides some common routines to help manipulate data.

3.1.0 NMI Service Routine:

As described in section 2.2.1 the CPU receives a non-maskable interrupt every second. This interrupt is serviced by CLOCK routine. This routine updates the memory-based counters for hours, minutes and seconds. It also compares the time set for source observation and if it is equal sets an acquisition flag.

3.1.1 Interrupt Service Routine:

The interrupt to CPU occurs at the sampling frequency decided by the timer, in the present case the sampling interval is 48 msecs. If the data acquisition flag is set then in this routine the analog signals are latched into S/H circuits. These are multiplexed and the 12-bit digital data are read by CPU into its registers, converted into a string of six hex characters and output to the serial port at 4800 bits/sec. At a sampling frequency of 20 Hz the interrupt routine utilizes about 30% of the CPU time.

3.2 Main Programme:

The main software programme for acquiring and storing the data is developed in Turbo Pascal ver 4.0. The main functions of this programme are to download necessary parameters to the ADC system such as time of synchronisation, starting time of observation, duration of observation, beamcode for the source to be observed etc. The programme is menu-driven and offers various choices to carry out observations, view data or monitor the system. This programme uses a datafile containing names of the sources and the beam number required to point the antenna to the respective source. The data received from the ADC system are stored in the arrays. On completion of the duration of observation data are automatically saved on the disk along with necessary house keeping information.

The name of the data file is the name of the radio source itself with a file extension consisting of three characters representing the julian day of the observation. The data are then available for quick look graphics display. Several radio sources can be observed in a sequence without any manual operation. Each source can be observed for a maximum of 50 minutes i.e. 62,500 data samples (with present sampling rate) which is 250 Kbyte of data. The data files are stored on 20 Mbyte winchester disk. These data files must be periodically removed to other storage devices. The floppy disks provide a convenient mode of data transportation. The listing of various programmes appear in a separate report. Further details are discussed in the following section on system operation. Besides this main programme other utility programmes are developed to help data transportation.

4.0 System Operation:

The system operation is entirely through the computer keyboard and monitor except for a reset switch on the ADC unit. It is made interactive and menu-driven so that even non-programmers can operate the system. The executable code of the programme named IPSAUTO is placed in AUTOEXEC batch file so that it is executed automatically at power on or booting the computer system. It is essential to enter the DATE correctly as it is used to calculate julian day which goes as a part of the file name and helps in identifying the data file. On execution of the programme it comes up with a menu of nine functions

which are described in detail here.

4.1.0 Clock Synchronisation:

This function allows to synchronise the software driven real-time clock in ADC system with the IST clock. Upon entering this function the readiness of ADC system must be checked by pressing "ENTER" key, the ADC should respond with "." prompt. If there is no response the ADC system can be reinitialised by the reset switch. After the prompt is seen press the "ESC" key, the computer then requests to enter the time for synchronisation. The time should be entered in the format specified i.e. two digits each for hours, minutes and seconds. The time to be entered is obtained from the display of the IST clock. The time entered must be the time of the next completing minute. The "ENTER" key must be immediately pressed, if real time passes the time entered before the "ENTER" key is pressed then the synchronisation will not be proper. At this stage the display will show a stationary clock and it will start ticking at the minute transition. Keep the space bar pressed to see the displayed clock updating. Having satisfied that the clock is in synchronism with the IST clock, "ESC" key is used to return to the menu.

4.1.1 Terminal:

This function provides the capability to debug the ADC system by using the microcomputer as terminal to the system.

4.1.2 Observations:

This function is used to take the observation for a single source, selecting this function the computer prompts the user to enter name of the source, starting time of the observation and duration of the observation etc. and then waits till the scheduled observations are taken. It displays the number of data points acquired while it is doing so. At completion of the period of observation the data are stored in a file with the file name as described in section 3.2.

4.1.3 Programmed Observation:

In this function number of sources to be observed in a sequence are programmed. The system requests to enter necessary parameters as above for all the sources to be observed. The input query is terminated by typing "END" for a source name. The information entered is displayed in a tabular form for verification. If there are any errors the user has the option to reenter the data. If the acknowledgement is positive computer lists all the sources, programmed to be observed and proceeds to acquire the data. As the data acquisition proceeds it shows the status of each source. The programme goes back to the main menu when all the sources are observed.

4.1.4 Display:

This function gives the graphical display of the data of the currently recorded source or previously recorded source. The data can be viewed for different time intervals beginning

with 0.5 minute to complete duration of observation. The display on the screen can be copied on a paper by a dotmatrix printer. Two such print outs on different time scales are shown in Figures 7 and 8.

4.1.5 Loading previously recorded source:

This function is provided to load memory with previously recorded datafile for viewing.

4.1.6 Automatic Observations:

Once the observation schedule file is prepared as described in 4.1.3 which is transparent to the user, this function carries out the task of data acquisition for all the sources listed in this file. This file can also be created/edited by any text editor utility.

4.1.7 Clock Display:

This function displays the real-time clock in the ADC system to help ascertain that the clock is in synchronism with the IST.

4.2 File Transfer Utility:

The data files are ultimately to be transferred to DEC-10 or Micro-VAX computer for processing and archival storage on magnetic tapes. The detafiles on the winchester or floppy disks are in the binary format which is the most compressed

way to store the data. However this format is not suitable for transmission over an asynchronous line such as a time-shared terminal. In absence of a direct connection of the micro-computer engaged in data acquisition with DEC-10 the data file is transported to the IBM PC/XT system having such a link. Then a utility programme IPSTRAN converts the binary file into a compressed ASCII file. In this ASCII file a combination of two non-control ASCII characters are used to represent a single 12-bit binary value. The data samples are divided into records of 256 samples each for "SIN" and "COS" channels. The record also holds the information about time of the first sample in the record.

This file is then transmitted to DEC-10 under terminal emulation programme running on IBM PC/XT. Another utility programme in DEC-10 converts this compressed ASCII file into understandable format. This format is compatible with the existing disk file format used by IPS data processing programmes.

5.0 Conclusions:

Three identical systems have been fabricated one each for Thaltej, Rajkot and Surat. The system at Thaltej has been operational for more than a year. The other two systems also have been operational at Thaltej site for several months. Continuous and vigorous testing of all three systems in single as well as in parallel mode of operation has duly confirmed the system reliability. The correlation test between the three

systems when the same source was recorded showed a correlation factor close to 0.999. This correlation factor between three systems is shown in Appendix B, C & D. These three DAS systems are therefore suitable for observations of solar wind velocity using the interplanetary scintillations from three sites.

Acknowledgements:

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7. Intel Microprocessor and Peripheral Handbook, 1983.

8. Personal Computer XT Technical Reference Manual, 1983.

9. Version 4.0 Turbo Pascal Reference Manual by Borland International, 1987.

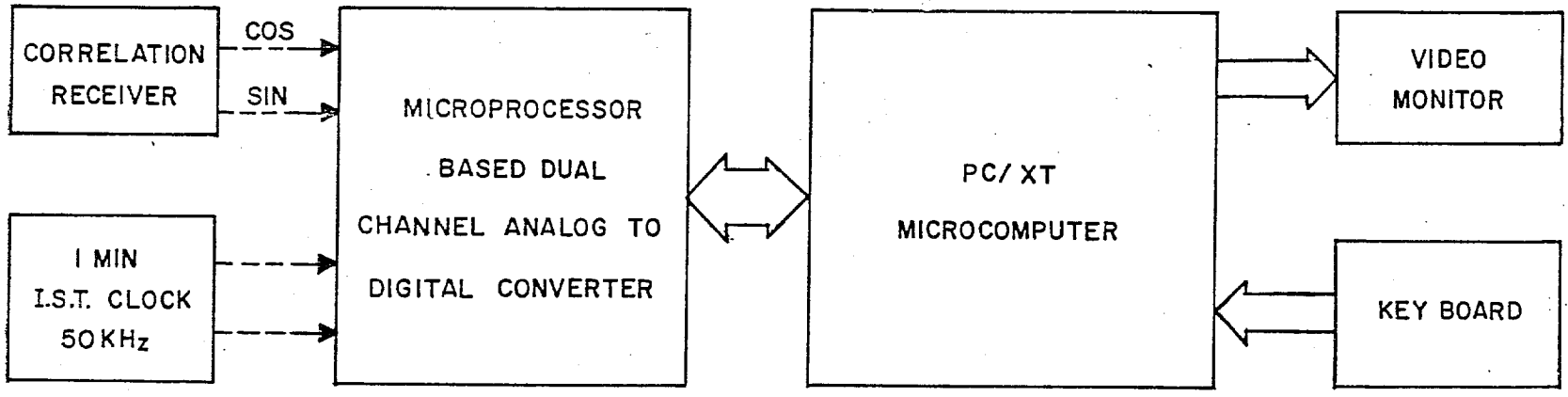

FIG. 1. DIGITAL DATA ACQUISITION SYSTEM BLOCK DIAGRAM

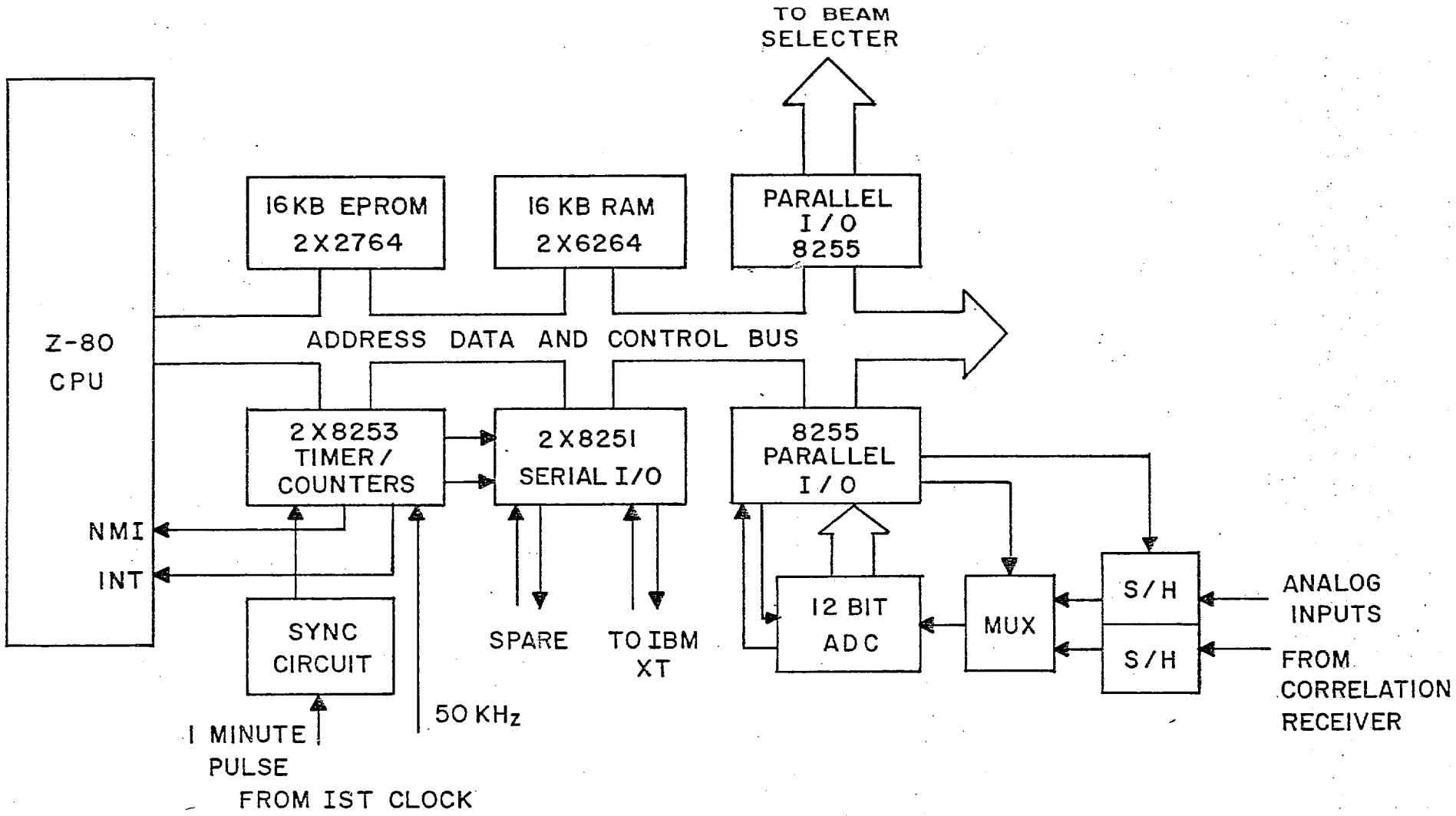

FIG. 2 MICROPROCESSOR BASED ANALOG TO DIGITAL CONVERTER

(BLOCK DIAGRAM)

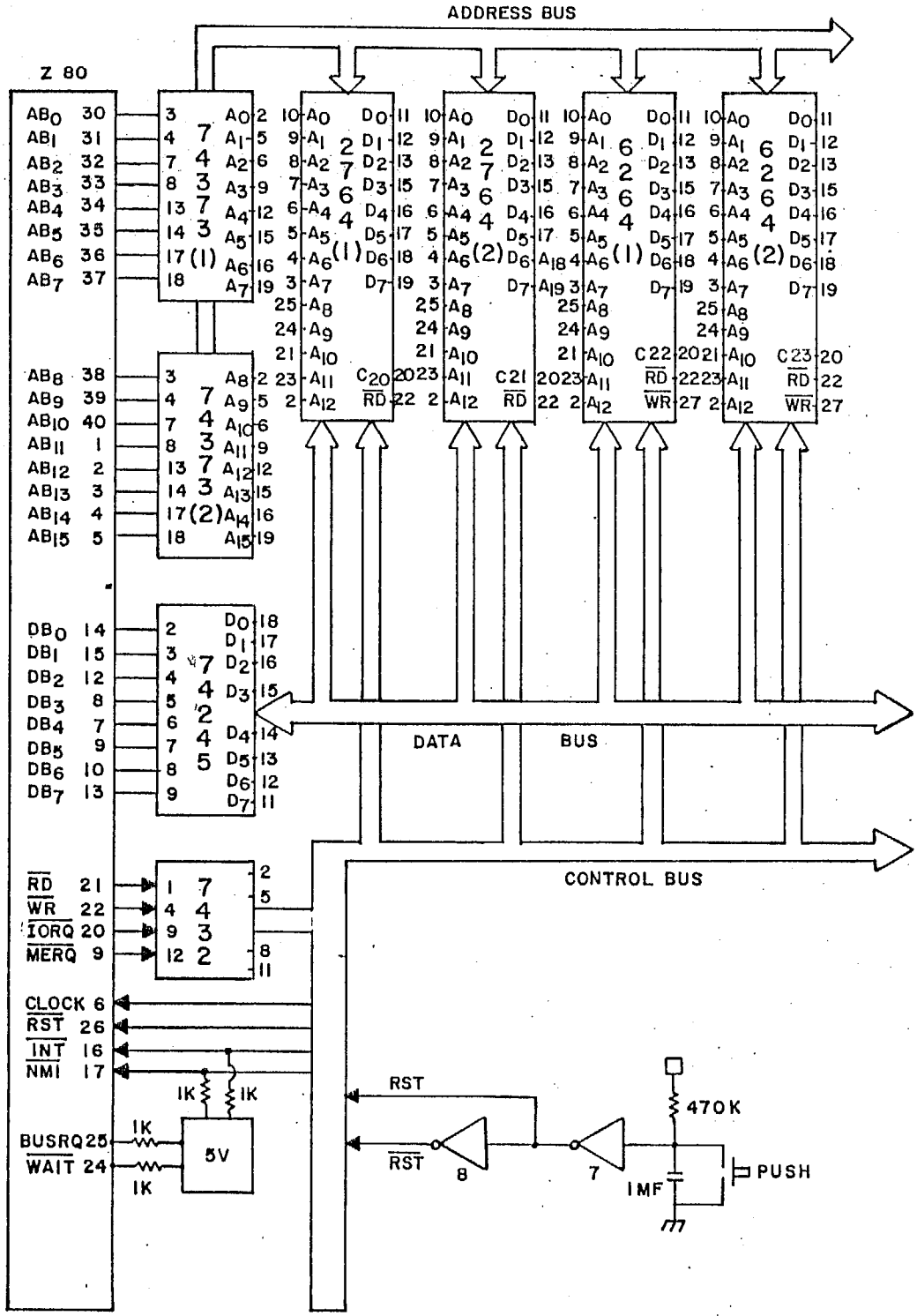

FIG. 3. MICROPROCESSOR AND MEMORY CIRCUIT

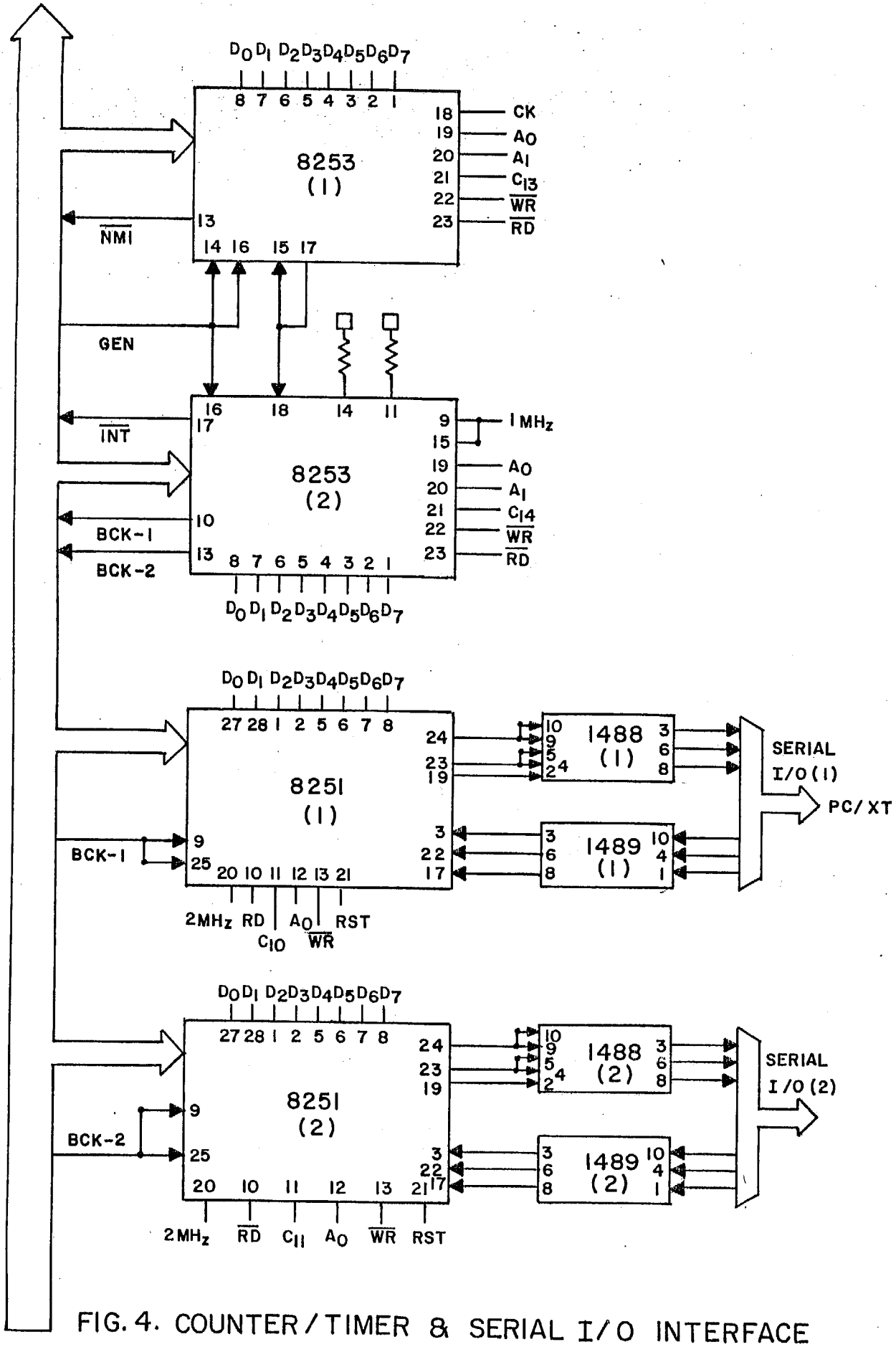

FIG. 4. COUNTER/TIMER & SERIAL I/O INTERFACE

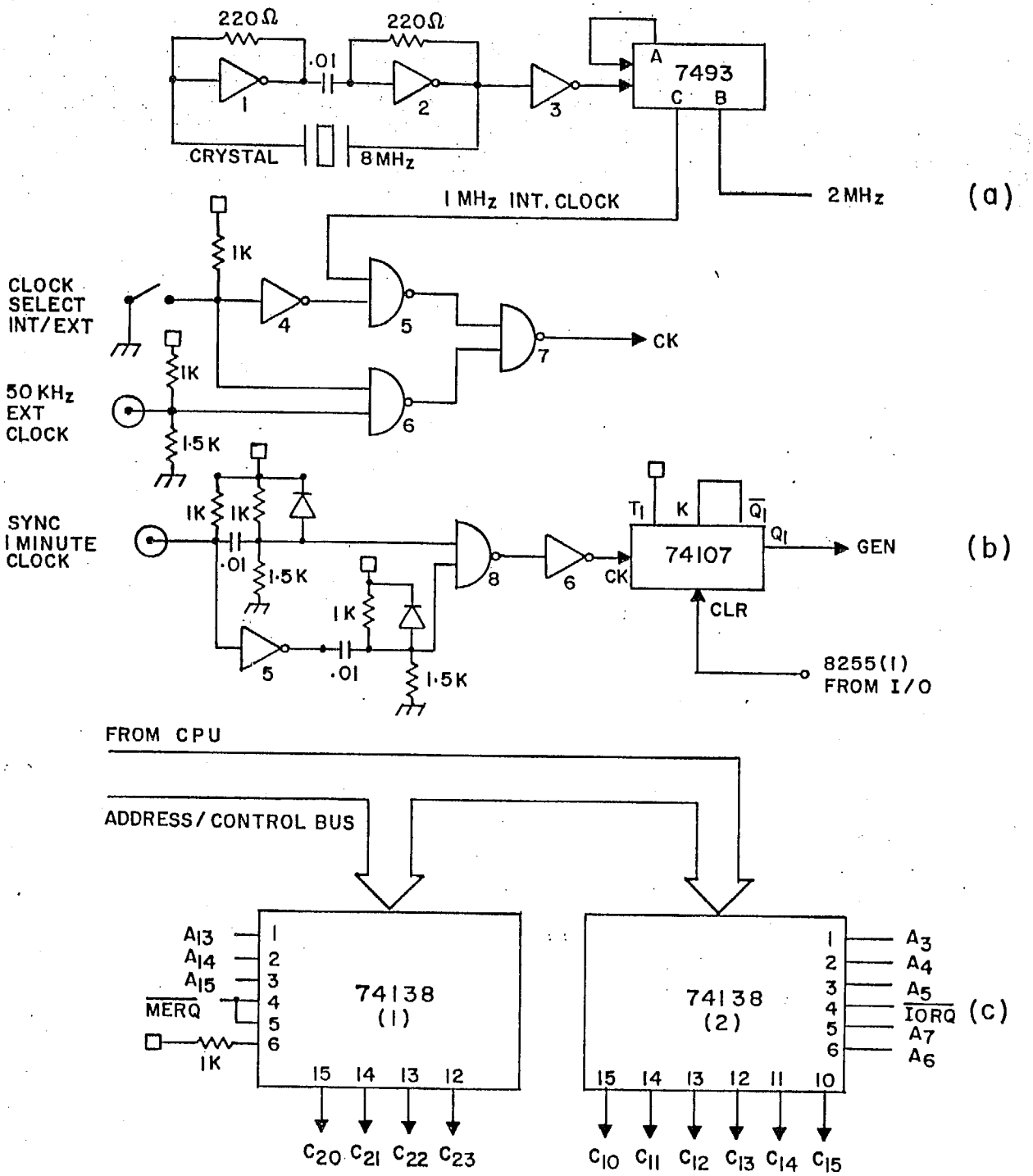

FIG. 5. CLOCK, SYNC. & CHIP SELECT BUFFERS

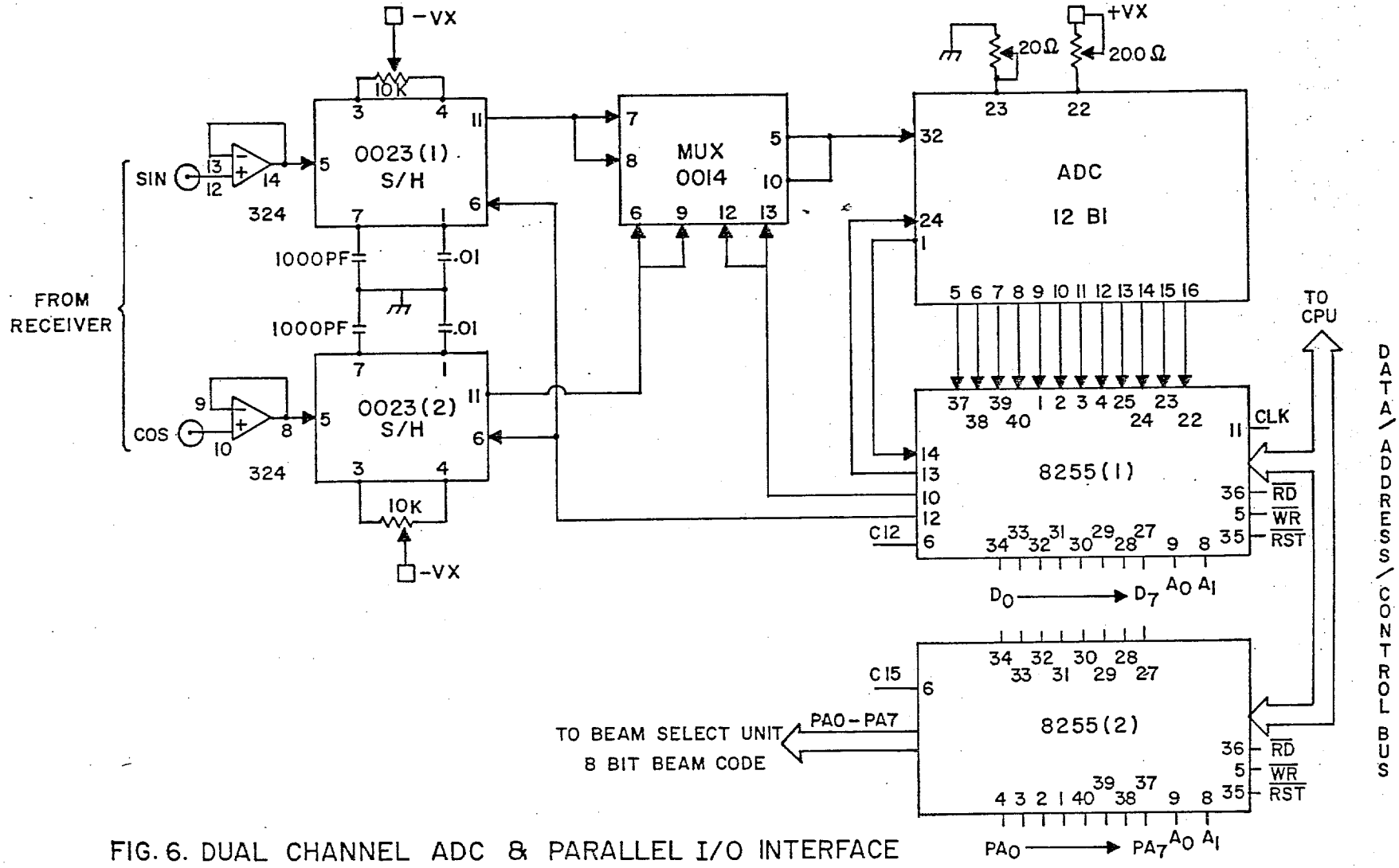

FIG. 6. DUAL CHANNEL ADC & PARALLEL I/O INTERFACE

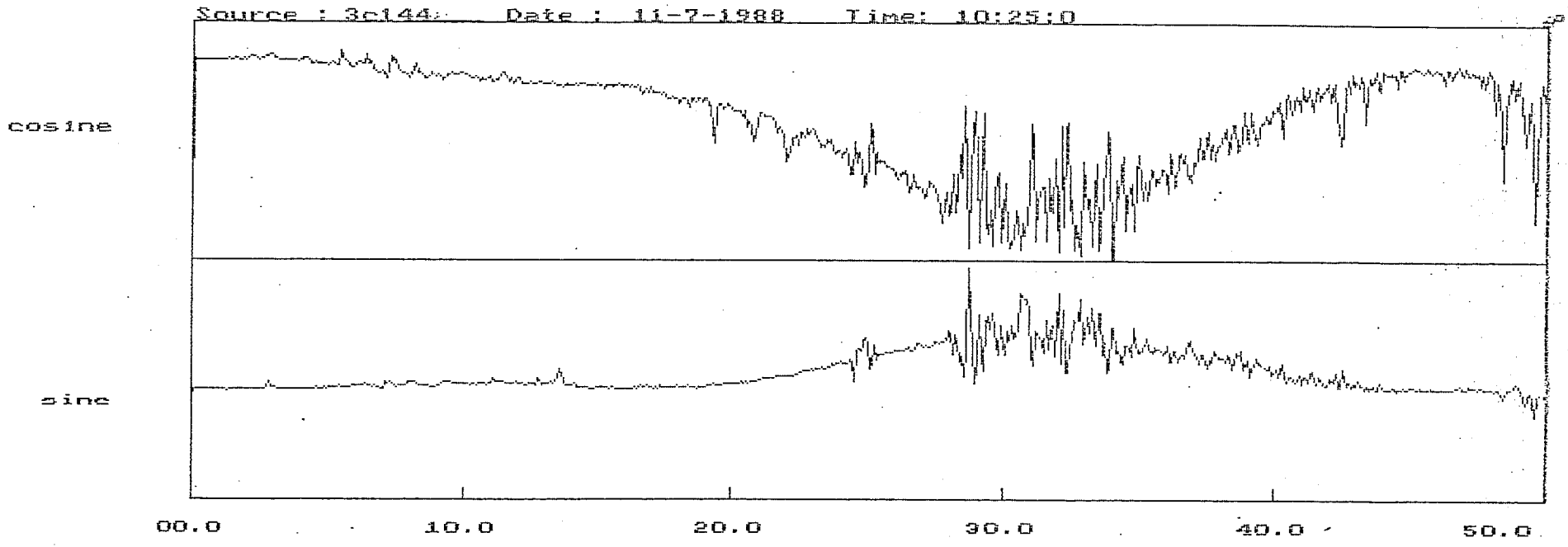
Source : 3c144
Date : 11-7-1988
Time: 10:25:0
cosine
sine
00.0
10.0
20.0
30.0
40.0
50.0

Fig. 7.

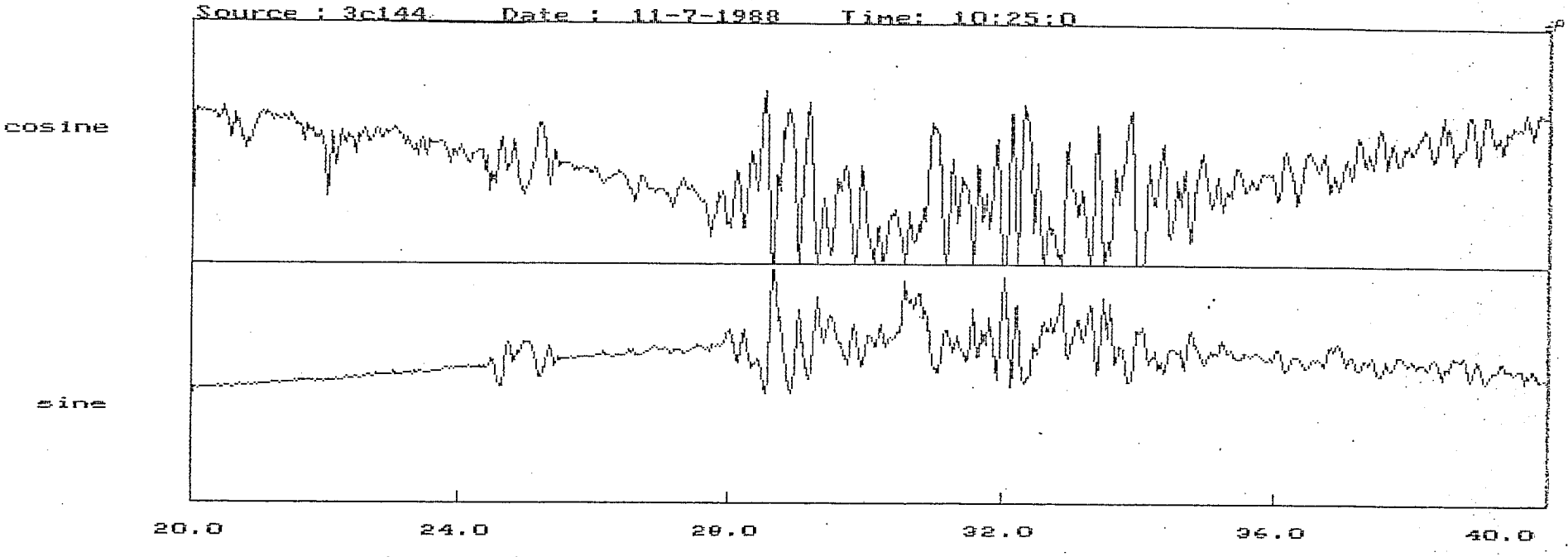
Source : 3c144
Date : 11-7-1988
Time: 10:25:0
cosine
sine
20.0
24.0
28.0
32.0
36.0
40.0

Fig. 8.

Appendix A

System Configuration

1. CPU - 8088 operating at 8/4.77 MHz

2. Memory - 640 Kbyte

3. Display - Hercules Graphics Adapter with Monochrome Monitor

4. Keyboard - IBM AT/XT compatible keyboard

5. Ports - Two serial and one parallel port

6. Operating system - MS DOS ver 3.2

Appendix B

CROSS CORRELATION FACTOR

Unit A	Unit B	Date	Time	COS	SIN
3c144a	3c144b	11/7/1988	10 25 0 48	0.99631	0.89618
3c144a	3c144b	11/7/1988	10 25 12 336	0.99660	1.00000
3c144a	3c144b	11/7/1988	10 25 24 624	0.99542	0.99983
3c144a	3c144b	11/7/1988	10 25 36 912	0.99683	0.99978
3c144a	3c144b	11/7/1988	10 25 49 200	0.99764	0.99963
3c144a	3c144b	11/7/1988	10 26 1 488	0.99584	0.99970
3c144a	3c144b	11/7/1988	10 26 13 776	0.99529	0.99963
3c144a	3c144b	11/7/1988	10 26 26 64	0.99789	0.99972
3c144a	3c144b	11/7/1988	10 26 38 352	0.99816	0.99950
3c144a	3c144b	11/7/1988	10 26 50 640	0.99726	0.99932
3c144a	3c144b	11/7/1988	10 27 2 928	0.99721	0.99951
3c144a	3c144b	11/7/1988	10 27 15 216	0.99754	0.99921
3c144a	3c144b	11/7/1988	10 27 27 504	0.99636	0.99932
3c144a	3c144b	11/7/1988	10 27 39 792	0.99940	0.99985
3c144a	3c144b	11/7/1988	10 27 52 80	0.99823	0.99858
3c144a	3c144b	11/7/1988	10 28 4 368	0.99188	0.99854
3c144a	3c144b	11/7/1988	10 28 16 656	0.99707	0.99783
3c144a	3c144b	11/7/1988	10 28 28 944	0.99713	0.99825
3c144a	3c144b	11/7/1988	10 28 41 232	0.99637	0.99905
3c144a	3c144b	11/7/1988	10 28 53 520	0.99877	0.99892
3c144a	3c144b	11/7/1988	10 29 5 808	0.99708	0.99880
3c144a	3c144b	11/7/1988	10 29 18 96	0.99575	0.99864
3c144a	3c144b	11/7/1988	10 29 30 384	0.99616	0.99667
3c144a	3c144b	11/7/1988	10 29 42 672	0.99374	0.99739
3c144a	3c144b	11/7/1988	10 29 54 960	0.99517	0.99766
3c144a	3c144b	11/7/1988	10 30 7 248	0.99167	0.99542
3c144a	3c144b	11/7/1988	10 30 19 536	0.99982	0.99802
3c144a	3c144b	11/7/1988	10 30 31 824	0.99803	0.99682
3c144a	3c144b	11/7/1988	10 30 44 112	0.99491	0.99548
3c144a	3c144b	11/7/1988	10 30 56 400	0.99720	0.99722
3c144a	3c144b	11/7/1988	10 31 8 688	0.99116	0.99365
3c144a	3c144b	11/7/1988	10 31 20 976	0.99930	0.99624
3c144a	3c144b	11/7/1988	10 31 33 264	0.99850	0.99401
3c144a	3c144b	11/7/1988	10 31 45 552	0.99291	0.99760
3c144a	3c144b	11/7/1988	10 31 57 840	0.99829	0.99809
3c144a	3c144b	11/7/1988	10 32 10 128	0.99976	0.99714
3c144a	3c144b	11/7/1988	10 32 22 416	0.99939	0.99527
3c144a	3c144b	11/7/1988	10 32 34 704	0.99231	0.99106
3c144a	3c144b	11/7/1988	10 32 46 992	0.99478	0.99700
3c144a	3c144b	11/7/1988	10 32 59 280	0.99965	0.99477
3c144a	3c144b	11/7/1988	10 33 11 568	0.99590	0.99524
3c144a	3c144b	11/7/1988	10 33 23 856	0.99733	0.99292
3c144a	3c144b	11/7/1988	10 33 36 144	0.99203	0.99008
3c144a	3c144b	11/7/1988	10 33 48 432	0.99373	0.99361

Appendix C

CROSS CORRELATION FACTOR

Unit B	Unit C	Date	Time	COS	SIN
3c144b	3c144c	11/7/1988	10 25 0 40	0.99640	0.87792
3c144b	3c144c	11/7/1988	10 25 12 336	0.99553	0.99925
3c144b	3c144c	11/7/1988	10 25 24 624	0.99445	0.99911
3c144b	3c144c	11/7/1988	10 25 36 912	0.99434	0.99916
3c144b	3c144c	11/7/1988	10 25 49 200	0.99622	0.99933
3c144b	3c144c	11/7/1988	10 26 1 488	0.99679	0.99896
3c144b	3c144c	11/7/1988	10 26 13 776	0.99614	0.99931
3c144b	3c144c	11/7/1988	10 26 26 64	0.99637	0.99894
3c144b	3c144c	11/7/1988	10 26 38 352	0.99661	0.99937
3c144b	3c144c	11/7/1988	10 26 50 640	0.99706	0.99921
3c144b	3c144c	11/7/1988	10 27 2 928	0.99757	0.99901
3c144b	3c144c	11/7/1988	10 27 15 216	0.99740	0.99949
3c144b	3c144c	11/7/1988	10 27 27 504	0.99758	0.99928
3c144b	3c144c	11/7/1988	10 27 39 792	0.99883	0.99888
3c144b	3c144c	11/7/1988	10 27 52 80	0.99892	0.99937
3c144b	3c144c	11/7/1988	10 28 4 368	0.99763	0.99976
3c144b	3c144c	11/7/1988	10 28 16 656	0.99770	0.99923
3c144b	3c144c	11/7/1988	10 28 28 944	0.99723	0.99907
3c144b	3c144c	11/7/1988	10 28 41 232	0.99767	0.99944
3c144b	3c144c	11/7/1988	10 28 53 520	0.99896	0.99938
3c144b	3c144c	11/7/1988	10 29 5 808	0.99777	0.99923
3c144b	3c144c	11/7/1988	10 29 18 96	0.99722	0.99912
3c144b	3c144c	11/7/1988	10 29 30 384	0.99638	0.99916
3c144b	3c144c	11/7/1988	10 29 42 672	0.99478	0.99922
3c144b	3c144c	11/7/1988	10 29 54 960	0.99678	0.99912
3c144b	3c144c	11/7/1988	10 30 7 248	0.99732	0.99919
3c144b	3c144c	11/7/1988	10 30 19 536	0.99992	0.99943
3c144b	3c144c	11/7/1988	10 30 31 824	0.99898	0.99917
3c144b	3c144c	11/7/1988	10 30 44 112	0.99827	0.99932
3c144b	3c144c	11/7/1988	10 30 56 400	0.99867	0.99949
3c144b	3c144c	11/7/1988	10 31 8 688	0.99704	0.99928
3c144b	3c144c	11/7/1988	10 31 20 976	0.99976	0.99938
3c144b	3c144c	11/7/1988	10 31 33 264	0.99959	0.99928
3c144b	3c144c	11/7/1988	10 31 45 552	0.99532	0.99952
3c144b	3c144c	11/7/1988	10 31 57 840	0.99959	0.99985
3c144b	3c144c	11/7/1988	10 32 10 128	0.99990	0.99953
3c144b	3c144c	11/7/1988	10 32 22 416	0.99974	0.99951
3c144b	3c144c	11/7/1988	10 32 34 704	0.99887	0.99936
3c144b	3c144c	11/7/1988	10 32 46 992	0.99822	0.99959
3c144b	3c144c	11/7/1988	10 32 59 280	0.99980	0.99933
3c144b	3c144c	11/7/1988	10 33 11 568	0.99869	0.99947
3c144b	3c144c	11/7/1988	10 33 23 856	0.99952	0.99937
3c144b	3c144c	11/7/1988	10 33 36 144	0.99873	0.99936
3c144b	3c144c	11/7/1988	10 33 48 432	0.99855	0.99953

Appendix D

CROSS CORRELATION FACTOR

Unit A	Unit C	Date	Time	COS	SIN
3c144a	3c144c	11/7/1988	10 25 0 48	0.99832	0.99903
3c144a	3c144c	11/7/1988	10 25 12 336	0.99480	0.99951
3c144a	3c144c	11/7/1988	10 25 24 624	0.99666	0.99958
3c144a	3c144c	11/7/1988	10 25 36 912	0.99748	0.99977
3c144a	3c144c	11/7/1988	10 25 49 200	0.99606	0.99950
3c144a	3c144c	11/7/1988	10 26 1 488	0.99621	0.99936
3c144a	3c144c	11/7/1988	10 26 13 776	0.99404	0.99949
3c144a	3c144c	11/7/1988	10 26 26 64	0.99672	0.99911
3c144a	3c144c	11/7/1988	10 26 38 352	0.99655	0.99918
3c144a	3c144c	11/7/1988	10 26 50 640	0.99539	0.99940
3c144a	3c144c	11/7/1988	10 27 2 928	0.99771	0.99909
3c144a	3c144c	11/7/1988	10 27 15 216	0.99642	0.99935
3c144a	3c144c	11/7/1988	10 27 27 504	0.99657	0.99902
3c144a	3c144c	11/7/1988	10 27 39 792	0.99830	0.99979
3c144a	3c144c	11/7/1988	10 27 52 80	0.99864	0.99934
3c144a	3c144c	11/7/1988	10 28 4 368	0.99278	0.99835
3c144a	3c144c	11/7/1988	10 28 16 656	0.99612	0.99785
3c144a	3c144c	11/7/1988	10 28 28 944	0.99762	0.99787
3c144a	3c144c	11/7/1988	10 28 41 232	0.99728	0.99853
3c144a	3c144c	11/7/1988	10 28 53 520	0.99040	0.99846
3c144a	3c144c	11/7/1988	10 29 5 808	0.99784	0.99812
3c144a	3c144c	11/7/1988	10 29 18 96	0.99485	0.99774
3c144a	3c144c	11/7/1988	10 29 30 384	0.99402	0.99595
3c144a	3c144c	11/7/1988	10 29 42 672	0.99279	0.99738
3c144a	3c144c	11/7/1988	10 29 54 960	0.99544	0.99679
3c144a	3c144c	11/7/1988	10 30 7 248	0.99216	0.99483
3c144a	3c144c	11/7/1988	10 30 19 536	0.99978	0.99795
3c144a	3c144c	11/7/1988	10 30 31 824	0.99763	0.99625
3c144a	3c144c	11/7/1988	10 30 44 112	0.99422	0.99537
3c144a	3c144c	11/7/1988	10 30 56 400	0.99711	0.99704
3c144a	3c144c	11/7/1988	10 31 8 688	0.99140	0.99358
3c144a	3c144c	11/7/1988	10 31 20 976	0.99933	0.99609
3c144a	3c144c	11/7/1988	10 31 33 264	0.99867	0.99331
3c144a	3c144c	11/7/1988	10 31 45 552	0.99242	0.99737
3c144a	3c144c	11/7/1988	10 31 57 840	0.99832	0.99799
3c144a	3c144c	11/7/1988	10 32 10 128	0.99974	0.99676
3c144a	3c144c	11/7/1988	10 32 22 416	0.99920	0.99507
3c144a	3c144c	11/7/1988	10 32 34 704	0.99258	0.99094
3c144a	3c144c	11/7/1988	10 32 46 992	0.99550	0.99662
3c144a	3c144c	11/7/1988	10 32 59 280	0.99960	0.99427
3c144a	3c144c	11/7/1988	10 33 11 568	0.99628	0.99496
3c144a	3c144c	11/7/1988	10 33 23 856	0.99683	0.99283
3c144a	3c144c	11/7/1988	10 33 36 144	0.99180	0.98959
			10 33 48 432	0.99330	0.99294