PRL

Technical Note

PRL-TN-86-57

DIGITAL DATA ACQUISITION SYSTEM FOR 3-SITE INTERPLANETARY SCINTILLATION PROJECT

By

A.D.Bobra, C.K.Viswanathan Achari and H.T.Ali

1986

Physical Research Laboratory
Ahmedabad-380009

DOCUMENT CONTROL AND DATA SHEET

1. Report No.	:	PRL-TN-86-57
2. Title and Subtitle : ' DIGITAL DATA ACQUISITION SYSTEM FOR 3-SITE INTERPLANETARY SCINTILLATION PROJECT '	3. Report Date	: Dec. 1986
	4. Type of Report	: Technical Report
	5. Pages	: 39
	6. Price	: Unpriced
	7. No. of References	: 7
8. Author(s)	:	A.D.Bobra, C.K.Viswanathan Achari & H.T.Ali
9. A. Purpose	:	Data Acquisition
B. Useful for	:	3-Site Interplanetary Scintillation (IPS) data acquisition
10. Originating Unit/ Division and Address	:	Radio Astronomy Group of Solar & Plasma Astrophysics Area Physical Research Laboratory Navrangpura, Ahmedabad-380009
11. Sponsoring Agency	:	DOS/DST
12. Abstract :	:	Details of the digital data acquisition system developed and installed at each of the three-field sites (viz.Thaltej, Rajkot and Surat) of the Interplanetary Scintillation (IPS) project.
13. Key-words	:	1. Data Acquisition 2. IPS Instrumentation
14. Distribution statement	:	Distribution unlimited
15. Security Classification	:	Unclassified

DIGITAL DATA ACQUISITION SYSTEM FOR 3-SITE INTERPLANETARY SCINTILLATION PROJECT

A.D. Bobra, C.K. Viswanathan Achari & H.T. Ali
Physical Research Laboratory
Ahmedabad-380009

ABSTRACT

We present here details of the digital data acquisition system[1,2] developed and installed at each of the three-field sites (viz. Thaltej, Rajkot and Surat) of the Interplanetary Scintillation (IPS) project. The 'SIN' and 'COS' outputs of the correlation receiver together with the scintillometer output are recorded on a strip chart for estimating scintillation index and also for monitoring purpose. The same data are converted into digital form and simultaneously recorded on a digital magnetic tape along with Indian Standard Time (IST) and system status information for facilitating further processing and analysis.

Introduction:

First a simple data acquisition system (DAS) capable of recording only a single receiver output, either 'COS' OR 'SIN'[1,2] was developed. This system was redesigned, keeping in mind that the system should be simple in operation. The two field stations viz.

Rajkot and Surat are situated within the respective University complexes. From the 2 to 3 years of operation of the DAS system at Thaltej, we concluded that: (i) maximum of about 250 sources might be of interest; (ii) the sampling frequency need not be kept variable and could be fixed at 20 Hz; and (iii) the A/D converter should be of high resolution (12 bit). These points were the basis of the modified DAS design.

The Digital data Acquisition system:

The block diagram of the modified DAS is shown in Fig. 1. The system is divided into the following subsystems:

(i) Hex encoder
(ii) Memory Register
(iii) Mux controller
(iv) A/D converter
(v) Data multiplexer
(vi) Pertec controller & Interface, and
(vii) Clocks

Various input and output signals in these subsystems are shown in Fig. 2.

HEX ENCODER

This sub-system shown in Fig. 3, provides the necessary decoded data from the HEX key board to the memory circuit for storing the information in the RAM - in the MANUAL/WRITE/NOT MODIFY/NOT RUN mode (WRITE MODE). In AUTO/READ/NOT MODIFY/RUN mode (RUN MODE) the HEX encoder provides data for scanning the RAM address at the rate of 100 Hz.

In the WRITE mode the 8 bit address of RAM is selected using a HEX Encoder, 4 bits at a time. For this purpose, the data select inputs of 16-input multiplexer 74150, are connected to the 4-bit output of a Binary Counter 74193. The clock to the Binary counter is disabled when the HEX-key (which is pressed) is selected by the multiplexer. The 4-bit output of the Binary counter is then latched in 4-bit latch 7475. When the next key is pressed, the second latch is activated. Thus, the 8-bit address is selected. These 8 bits are then loaded on to the outputs of two Binary counters 74193 using parallel load facility. This is done by pressing a LOAD switch on the front panel. These are then decoded and displayed on the front panel. These addresses are connected to the memory through open collector buffer 7417.

In the RUN mode the binary counter input is 100 Hz IST. This input is present only when the front panel switches are in accordance with the RUN mode. This enables the memory address to change at the rate of 100 Hz.

MEMORY REGISTER

This sub-system shown in Fig. 4, stores the 40-bit source information for maximum of 256 radio sources. The source information includes SDT ON time, SDT OFF time, BEAM CODE (Table-1), LOW FREQUENCY ATTENUATION (LF ATT.) and ON BIT. Radio sources are given codes from 00_H to FF_H. These are nothing but the memory addresses. The information for each source is stored in 10 numbers of 256 x 4 bit STATIC RAM. All the outputs of the RAMS are connected to displays (HP 5082-7391 and HP 5082-7395) on the front panel to display the stored information. The flexibility in selecting SDT ON time and SDT OFF time helps in observing sources having very close transit times. The ON-BIT selection provides flexibility, to the observer, to select the program on daily, weekly or monthly basis.

This sub-system also converts the serial SDT clock data to parallel data using 8-bit serial to parallel converter 74164. The parallel data are then latched to

4-bit shift register 7495 using parallel-in, parallel-out mode. The hours and minutes output of this latch (16 bits) are connected to 2 sets of B inputs of 4 x 4 bit magnitude comparators 7485, one for the ON time comparison and another for the OFF time comparison.

In RUN MODE the RAM is scanned at the rate of 100 Hz. This means the output of the RAM is available for comparison and display to the circuit for 10 milliseconds. The SDT ON time of hours & minutes (16 bits) are connected to the input A of the ON time nagnitude comparator.

When the actual SDT time is equal to the stored SDT ON time the scanning of RAM is disabled and the data are displayed. This comparator output is fed to the present input of D-Flip flop (D F/F) 7474 via a 2-input OR gate 7432. The other input of the OR gate is connected to a microswitch for manual start through a debouncing circuit. The D F/F output is ON output and is connected to a 2-input NAND gate 7400, the other input being from the ON-BIT. Thus, the system ON and $\overline{\text{ON}}$ outputs are available only and only when the ON-BIT is logical ONE. The ON and $\overline{\text{ON}}$ control the system operation. A similar circuit is used for OFF time comparison and control.

Once the data are entered in the WRITE mode the ON bit can be modified using a MODIFY MODE. In this mode the control switches should be in MAN / WRITE / MOD / NOT RUN position. This enables only the ON BIT to change keeping the other information intact.

MUX CONTROLLER

This sub-system generates all the control pulses required for analog signal processing and digital data recording. Fig. 5 shows the system diagram and Fig. 6 shows the various control pulses generated.

The 1 kHz IST clock is connected to a monoshot 74121 D6 to stretch the pulse, and used as a clock to serial shift registers 74164. These 74164 are enabled by the ON signal received from the D F/F 7475 D4. The input to this F/F is derived from IST 1-minute pulse, and the ON signal from memory register subsystem. The 20 Hz signal derived from IST is available and used as a clock to Dual JK F/F 7473. The output of this F/F along with 1 kHz signal obtained from AND gate 7408 is connected to another AND gate whose output is used as a clock to the next JK F/F 7473. This circuit enables only one pulse of 1 kHz to pass through during one cycle of 20 Hz. This

output is again connected to a monoshot C1 74121.

The output of this monoshot is connected as an input to a serial shift register. This pulse is then shifted serially at 1 kHz rate and various outputs such as RESET, SAMPLE AND HOLD (S & H), ANALOG MULTIPLEXER (MUX A/MUX B), SELECT BYTES of SIN AND COS, etc. are generated.

The Byte selection outputs are also connected to a NAND gate 7440 after inversion using 7404. This is then ANDED with the FEN input available from Pertec Controller. This is the ANS STROBE for the Pertec controller.

The count input received from the Pertec controller is connected to the input of the Binary counters 7493 connected in cascade. The 7-bit output is the address of a system status multiplexer (SYS-MUX) and connected to the data multiplexer subsystem. The time-up-date for recording the system status is modified only at the falling edge of the most significant bit of the SYS-MUX address. This is achieved using one JK F/F B6 7473 and an AND gate 7408.

A/D CONVERTER

As said earlier, we need to record the SIN and COS outputs of the receiver within the range of ± 5 volts. It is important that these signals should be sampled simultaneously at a sampling rate of 20 Hz. As described earlier the various control signals are generated on the MUX-CONTROLLER sub-system.

The analog signals from the receiver are connected to two S & H circuits 0023C after a unity gain buffer using operational amplifier (Op.Amp.) 741, as shown in Fig.7. These signals are sampled by the S & H control pulse after it is stretched by the monoshot B6 74123. The outputs of the 0023C are connected to an analog multiplexer (ANA-MUX) 0014CD. The MUX A and MUX B control pulses are ORed in 7432. The output is connected to the clock input of a JK F/F wired in a toggle mode. The Q output of this F/F is connected to the select input of the ANA-MUX. The output of the ANA-MUX is connected to the input of an A/D converter (A/D C) EH12B1, through a unity gain buffer using an Op.Amp. 741. The MUX-A, MUX-B ORed output is also connected to the start conversion input of A/D C, after stretching by using monoshots 74123. The 12-bit outputs

of the A/D C are connected to a tri state logic (TSL) circuit 8197. The six outputs of each TSL are connected together. This enables to get only a 6-bit output at a time. The control gate input to TSL 8197 is derived from the COS I, COS II, SIN I, SIN II inputs after they are ORed and connected to the clock input of JK F/F wired in the toggle mode. The outputs Q and $\overline{Q}$ of this F/F are connected to the control gate of TSL. The sequence in which the TSL outputs available is:

Most significant 6 bits of COS
Least significant 6 bits of COS
Most significant 6 bits of SIN
Least significant 6 bits of SIN

These are then connected to the PERTEC Controller.

DATA MULTIPLEXER

This sub-system converts the parallel system status information (SSI) viz. IST time upto millisecond, Station code, source code, L.F. Attn., Beam code, SDT ON time and synchronization word (Sync. Word), into one-bit serial output. This one-bit (Status information bit-SIB) is the least significant bit (LSB) in the 8-bit byte data

being recorded onto a magnetic tape. The SSI is 128 bits long and, therefore, with every 128 bytes recorded on tape, we get complete SSI. Thus, in a record length of 1024 bytes SSI is repeated 8 times. This enables to cross-check the SSI, in case of problems, while decoding in the computer.

The IST serial data are first converted to parallel using serial-to-parallel converter 74164 at the clock rate of 50 kHz as shown in Fig. 8. The parallel outputs are connected to the input of a shift register 7495 used in parallel-in-parallel-out mode. This is enabled by the modify-time pulse which is available only when one complete cycle of SSI is recorded.

The heart of this subsystem is the 16-input data multiplexer 74150. The 128 inputs of the SSI are connected to the inputs of 8 data multiplexers in a particular sequence. The IST time (6 bytes) inputs are derived from the shift registers 7495. The station code (1 byte) is wired permanently for a specific field station (Thaltej $D2_H$, Rajkot CD_H, Surat $C9_H$). The source code (1 byte) is derived from the address of the memory register sub-system. The LF Attn. and Beam Code (each of 1 byte) inputs are derived from the Front panel. For LF Attn. only 4 LSB and for beam code only 6 LSB are used.

Remaining bits are connected to Logic Zero permanently. The SDT-ON time (2 bytes) inputs are derived from the memory register sub-system. These are the memory outputs. The Sync-Word is 4 bytes long and permanently wired as $OOFFOFOF_H$. The Sync-Word is used to identify the position of various informations while decoding the SSI in the computer.

The 8-bit output of these multiplexers is connected to an 8-input multiplexer 74151. The 7-bit address (4 bit for 74150 and 3 bit for 74151) is derived from the mux controller sub-system. The one-bit serial output of SSI is available and connected to the Pertec controller for merging with A/D C data output to form bytes.

PERTEC CONTROLLER

The subsystem, shown in Fig. 9, generates commands viz. FEN, WFM, GO etc. necessary to initiate the operation of the PERTEC Buffered Magnetic Tape Transport (BMTT). On receipt of ON command from the mux controller, the Q output of D F/F 7474 becomes high and connected to the 4-input NAND 7440. The other inputs are from 1 kHz IST, AUTO/MAN and the $\overline{Q}$ of D F/F 7474. This output is then connected to a decade counter 7490 connected in cascade

to operate for divide by 50. Thus, a 20 Hz output is derived and is used for controlling the mux controller as shown in Fig. 6. JK F/F 7473 (B6, B4) are used to derive the serial input of serial-to-parallel converter 74164. The clock for this is derived from the output of NAND 7440 (A5) and NAND 7400 (B5). Using outputs of the serial-to-parallel converter FEN and WFM, control outputs are derived by D F/F 7474 (B2), monoshot 74121 and NAND 7400 (A3, C4).

One of the outputs of 74164 is the GO command. Internal reset is also generated.

These PERTEC control signals are generated on receipt of ON and OFF commands from the memory register and mux controller subsystems.

The final control signal generator shown in Fig. 10, which caters to the manual control as well as to the automatic control generated, is described below. A 5-bit shift register with clear and preset facility is used to control the manual operation. The signal generated by the Pertec controller subsystem is ORed with these outputs, and are connected as final control to the BMTT system. The ANSWER STROBE (ANS-STB) and GO are delayed using monoshot 74123 and OR gates 7432.

The GO and buffer A-OVERFLOW (A-OVF), buffer B-OVER FLOW (B-OVF) signals are ORed, stretched using 74123 and are connected to input of binary counter 7493 connected in cascade to count the number of records recorded on the BMTT. The output of these counters are connected to a Display (HP 5082-7395) on the front panel for monitoring.

The 6-bit data received from the A/D C are connected as 6 MSB and the one-bit serial (Fig. 11) SIB is connected as LSB, the other bit being permanently connected to logical zero. Thus, these bits form a byte. These 8 data lines are connected to open collector inverter 7416 and its outputs are connected to BMTT system. These outputs are also connected to the input of a NAND 7400 the other input being from the READ/WRITE (R/W) control on the front panel. These are called WRITE DATA for display. The 8 READ data lines and one parity line are terminated using 220/330 Ω resistances and connected to a NAND 7400. The other input to the NAND is again R/W control. These are called READ DATA for display. These READ and WRITE DATA lines are connected to the NAND as shown and are connected to an LED display on the front panel.

The BMTT status information signals received are first terminated, and connected to an AND 7408 (Fig. 12). The outputs are connected to an LED for display on the front panel after appropriate stretching using 74123 as required.

DIGITAL CLOCK

For the success of the 3-Site IPS experiment, it is of utmost importance to keep the digital clocks at these sites in synchronism with each other within, say about $\pm$ 5 msec. This is achieved by using a highly accurate and stable frequency source for digital clocks and synchronizing them with the national time signals ATA, transmitted from Kalkaji near New Delhi at frequencies of 5, 10 and 15 MHz[4].

The basic frequency standard is an oven-controlled Crystal Oscillator at a frequency of 10 MHz as shown in Fig. 14. The crystal used has frequency stability of $\pm 5 \times 10^{-10}$ per day under stable operating conditions. The output signal is sinusoidal and about 200 mv rms in amplitude. This is amplified using video amplifiers (LM733) and converted to TTL compatible signals using a high speed differential comparator (LM361) and a schmitt

trigger 7413. This is then connected to a Fine retard (R/F) and Coarse retard (R/C) circuit consisting of mono-shots and NAND gates. This circuit disables the clock for a fixed time interval. The R/F control disables the clock for about 1 msec and the R/C control disables it for about 20 msec. The 10 MHz output is then connected to a decade counter 7490 providing outputs of 1 MHz and 100 kHz. These outputs are then connected to a Fine advance (A/F) and a Coarse advance (A/C) circuit. Under normal operation, the 100 kHz clock is connected to another decade counter 7490, but when A/F or A/C control is operated, additional 1 MHz pulses are supplied to the decade counter, thus advancing the clock by a pre-determined interval, depending on the monoshot time constant. All these four controls are provided on the front panel. The two decade counters 7490, connected in cascade, now provide 50 kHz and 1 kHz outputs. Further counting is done using synchronous up/down counters 74192 connected in cascade with appropriate reset for days, hours, minutes, seconds and milliseconds. A set of 7 thumb-wheel switches (TWS) are used to load days, hours, minutes (preset time). When the time is loaded all the other counters are reset to zero. The output of 1 Hz and the 'A' output of

the minute counter (units) are available separately. The 1 Hz pulse is used for synchronizing the clock with the ATA using an oscilloscope. The minute pulse is used to start the DAS. The counter outputs from millisecond to days (parallel) are connected to a parallel-to-serial converter 74165. These are 48 bits long and are shifted by 50 kHz clock, thus we get a 48-bit serial output. The fresh information to these 74165 is loaded by a load pulse (PRF 960 /usec) derived from the display circuit. This ensures the serial clock information update every millisecond (msec). The 50 kHz serial data load pulse and 1 Hz pulse are also connected to a Buffer for display as well as for DAS.

The display circuit (Fig. 15), designed using multiplex technique, consists of a 4-bit serial-to-parallel shift register 7495, where the serial time data are first converted to 4-bit parallel data by the 50 kHz clock. The 50 kHz clock is also divided by 4 using JK F/F 7473. This output is used to latch the 4-bit parallel clock data to 7475. These latched outputs are then decoded using 7446 a seven-segment decoder driver. The 7 lines of decoded outputs are then connected to display-inputs, 'a' thro' 'g' of all the displays through an

appropriate resistance to limit the current. The divide-by-4 output is also connected to a binary counter 7493 and is used as divide by 12. This gives the load pulse of 960 μsec (PRF). The 4-bit output of this counter is then decoded using 7442 decimal decoder. Each output of the decoder is then connected to a buffer and a driver to drive the display. The display is thus selected one at a time. Only 9 outputs of the decoder are used to drive the display (DAYS-HOURS-MIN-SEC.).

The Sidereal Clock is identical to the IST clock described above except for the basic crystal oscillator. For this, a BEL crystal with a frequency of 10.026 MHz is used. This clock is used only to control the DAS "ON time" and "OFF time" and hence need not be highly accurate and stable.

OPERATING PROCEDURE

The System Library has to be loaded only once after the instrument power supply is switched 'ON'. The systems at all the three stations are run by an uninterrupted power supply (UPS) system. The UPS system has a capacity to run the entire system for about 5 hours, when batteries are fully charged. The entire operational

procedure is divided into 3 modes.

(i) LOAD OR WRITE MODE :- In this mode radio source parameters for all the sources planned to observe are stored in the memory register (called SOURCE LIBRARY). The control switches on the front panel are selected for this mode as follows:

AUTO/MANUAL	SWITCH	ON	MANUAL
READ/WRITE	"	"	WRITE
NOT MODIFY/MODIFY	"	"	NOT MODIFY
RUN/NOT RUN	"	"	NOT RUN

Now the source code is selected by HEX-ENCODER key board and by pressing the LOAD Switch. By a set of the TWS the SDT ON-TIME and SDT OFF-TIME are selected. By toggle switches the beam code is selected. The ON-BIT toggle is kept on low and the information written by pressing WRITE. For example to load for the source 3C48 (Source Code 37), SDT ON time 0504 and SDT OFF time 0604 (for 1 hour observation around transit time), beam 5R (beam code 14), ON BIT toggle to low, the display will read as: 37 0504 14 0604.

(ii) MODIFY MODE:- In this mode, only the ON-BIT of the source to be recorded is made High. The control switches are kept as follows:-

AUTO/MANUAL	SWITCH	ON	MANUAL
READ/WRITE	"	"	WRITE
NOT MODIFY/MODIFY	"	"	MODIFY
RUN/NOT RUN	"	"	NOT RUN

The source code is selected using the HEX-Key. The ON-BIT toggle is kept to HIGH and the WRITE-Key is pressed. The ON-BIT will display High.

(iii) RUN MODE:- This mode is used when the actual observations are taken. The controls are as follows:-

AUTO/MANUAL	SWITCH	ON	AUTO
READ/WRITE	"	"	READ
NOT MODIFY/MODIFY	"	"	NOT MODIFY
RUN/NOT RUN	"	"	RUN

The memory addresses are scanned at a rate of 100 Hz. The SDT time of the clock is checked with the stored SDT ON time output from the memory. Each output is available for about 10 msec for comparison and action. Once the time is matched, the sequence starts as described in the earlier

sections.

At the end of the SDT OFF time, a file-mark is recorded on the magnetic tape. After this, the ON BIT of this source is changed to Low and next source ON BIT to High by the modify mode.

SYNCHRONISATION OF THE IST CLOCK

For proper operations of the DAS at all the three IPS stations all the three IST clocks have to be accurate within $\pm$ 5 msec with one another. This is achieved by synchronising the clocks with ATA transmitted from New Delhi at 5, 10 and 15 MHz frequencies. ATA signal contains modulation of 5 pulses, 1 msec each in every second. The synchronisation is done with the help of a dual trace oscilloscope. Channel Y_1 and the external trigger inputs are simultaneously fed with 1 Hz output from the clock and the channel Y_2 is fed with the ATA signal from the RACAL receiver, as shown in Fig.13. If the rising edge of 1 Hz is not in synchronism with the first pulse of the ATA, the clock is made faster or slower as the case may be with the help of controls provided on the front panel. The controls are adjusted till the rising edge of 1 Hz is synchronised with the first pulse of ATA. Thus

the clock is exactly synchronised with the ATA. The accuracy of $\pm$ 5 msec is tolerated. Every 15 minutes, there is an announcement of time from the ATA.

Acknowledgements

The authors wish to express their gratitude to Prof. S.P. Pandya and Prof. R.K. Varma for their keen interest and support. We are thankful to Prof. R.V. Bhonsle and Prof. S.K. Alurkar for their valuable suggestions, guidance and enduring encouragements. Thanks are due to M/s. D.V. Subhedar, N.S. Jog and R.C. Shah for useful discussions. We are grateful to all the members of the IPS group for their timely help and co-operation. Thanks are given to the staff of the Workshop and PRL Computer Centre for extending their co-operation which enabled us to get the work done in time. Wiring of chips and other components of PCB and their assembly into a standard enclosure done by M/s. S.L. Kayastha, N.V. Dalal, D.R. Vinchhi and Arati Joshi is greatly appreciated. We are also thankful to Mr. A.H. Desai who helped in the preparation of the Circuit diagrams. We are very grateful to Mr. D. Stephen and Mrs. M.V. Vijayalakshmi for their neat typing of this document. The financial support to this project came from

the Department of Space and Department of Science and Technology, Govt. of India.

References

1. Progress report "Solar Activity & Interplanetary medium-Interplanetary Scintillation (IPS)" by S.K. Alurkar and R.V. Bhonsle.

2. A Correlation Interferometer for Interplanetary Scintillations Observations by S.K. Alurkar et al. JIETE, 28, 577, 1982.

3. A General purpose interface for Computer Compatible tape recorders by A.D. Bobra et al. PRL Technical Note TN-78-02.

4. Time Synchronization for a 3-site Interplanetary Scintillation (IPS) experiment using ATA time signal transmission by A.D. Bobra et al. JIETE, 27, 569, 1981.

5. Radio Astronomy by John D. Kraus, McGraw-Hill Book Company, 1966.

6. National Semiconductor TTL Data Book, 1980.

7. National Semiconductor Linear Integrated Circuit Data Book, 1982.

Figure Captions

Fig. 1: Block Diagram of Data Acquisition System (DAS)

Fig. 2: Diagram showing I/O signals of DAS

Fig. 3: Hex Encoder

Fig. 4: Memory Register

Fig. 5: Mux-Controller

Fig. 6: Timing Diagram

Fig. 7: A/D Converter

Fig. 8: Data Multiplexer

Fig. 9: Pertec Controller

Fig. 10: Control Signal Generator (Pertec)

Fig. 11: Write/Read Data Display (Pertec)

Fig. 12: Status Display (Pertec)

Fig. 13: Time Synchronization

Fig. 14: Digital Clock

Fig. 15: Clock Display

Table - 1

BEAM CODE

BEAM	CODE HEX	BEAM	CODE HEX
16L	00	1R	10
15L	01	2R	11
14L	02	3R	12
13L	03	4R	13
12L	04	5R	14
11L	05	6R	15
10L	06	7R	16
9L	07	8R	17
8L	08	9R	18
7L	09	10R	19
6L	OA	11R	1A
5L	OB	12R	1B
4L	OC	13R	1C
3L	OD	14R	1D
2L	OE	15R	1E
1L	OF	16R	1F

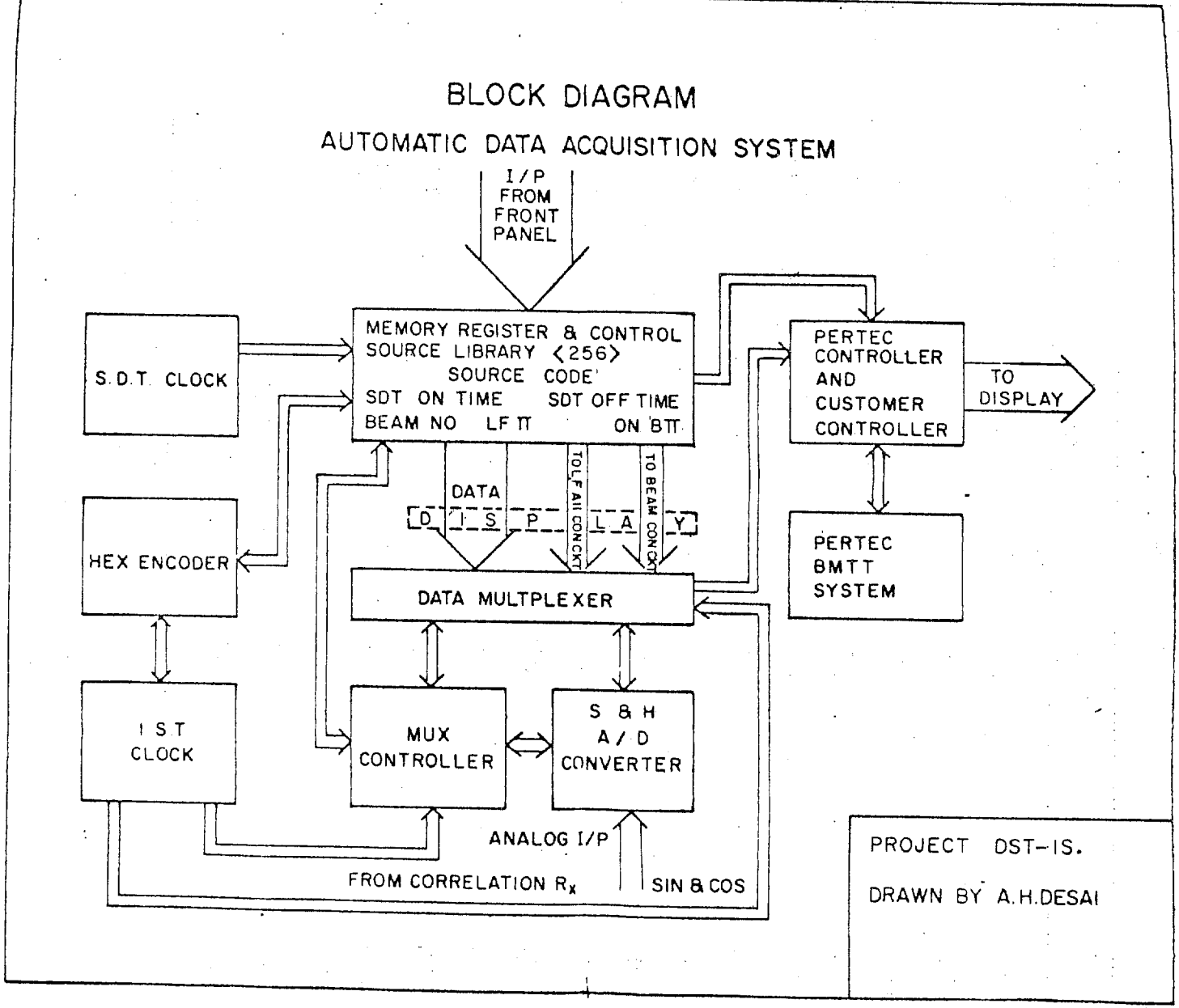

BLOCK DIAGRAM
AUTOMATIC DATA ACQUISITION SYSTEM
I/P FROM FRONT PANEL
S.D.T. CLOCK
MEMORY REGISTER & CONTROL
SOURCE LIBRARY <256>
SOURCE CODE
SDT ON TIME
SDT OFF TIME
BEAM NO
LF TT
ON BTT
PERTEC CONTROLLER AND CUSTOMER CONTROLLER
TO DISPLAY
DATA
D I S P L A Y
TO L.F. ALL CONCKT
TO BEAM CONCKT
HEX ENCODER
PERTEC BMTT SYSTEM
DATA MULTPLEXER
I S T CLOCK
MUX CONTROLLER
S & H A/D CONVERTER
ANALOG I/P
FROM CORRELATION R_x
SIN & COS
PROJECT DST-IS.
DRAWN BY A.H.DESAI

Fig.1

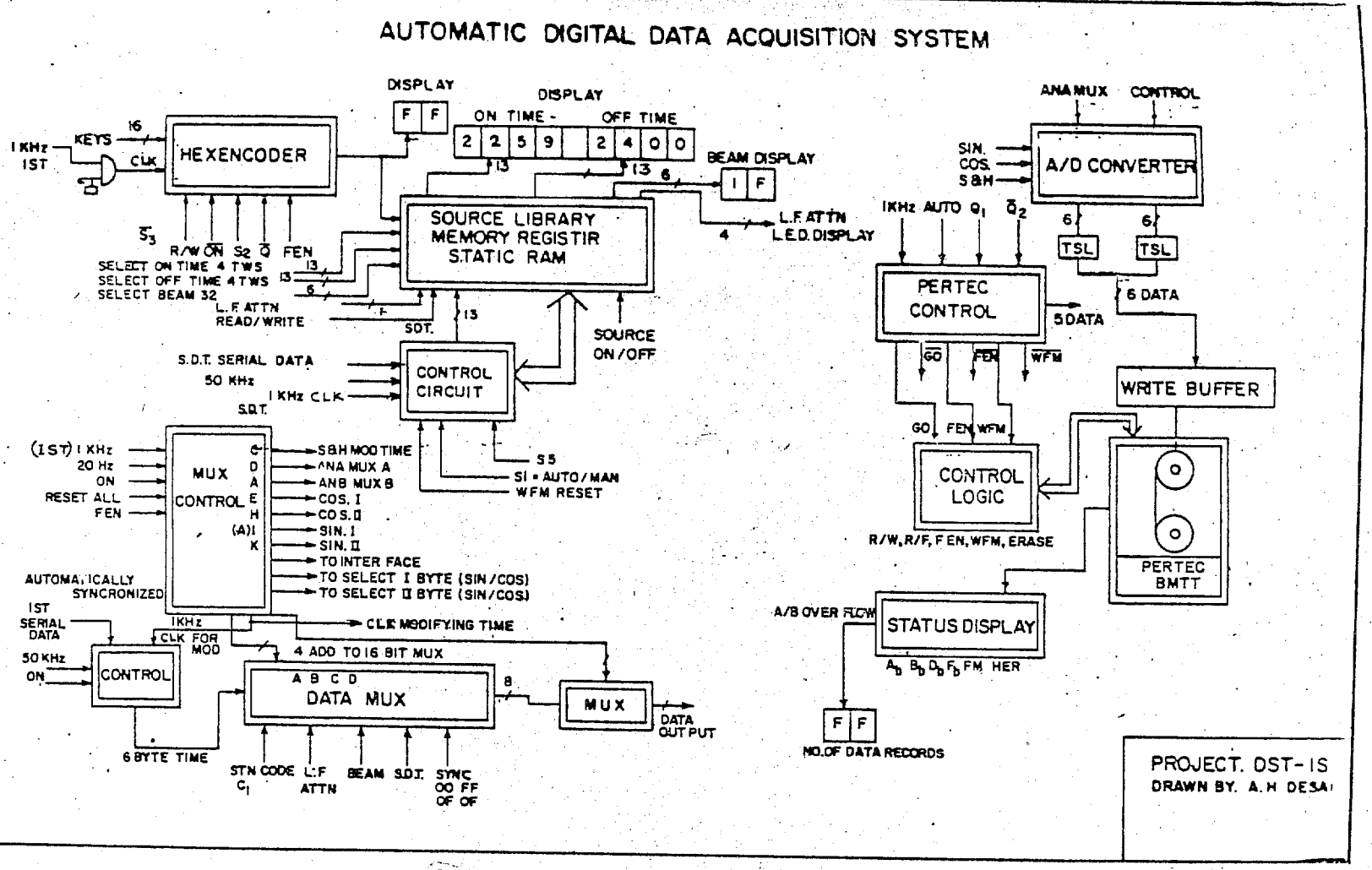

AUTOMATIC DIGITAL DATA ACQUISITION SYSTEM
DISPLAY
F F
DISPLAY
ON TIME - OFF TIME
2 2 5 9 2 4 0 0
BEAM DISPLAY
I F
1KHz
1ST
KEYS
16
CLK
HEXENCODER
SOURCE LIBRARY
MEMORY REGISTIR
STATIC RAM
L.F ATTN
L.E.D. DISPLAY
R/W ON S2 FEN
SELECT ON TIME 4 TWS
SELECT OFF TIME 4 TWS
SELECT BEAM 32
L.F ATTN
READ/WRITE
SDT.
S.D.T. SERIAL DATA
50 KHz
1 KHz CLK
S.R.T.
CONTROL
CIRCUIT
SOURCE
ON/OFF
(IST) 1 KHz
20 Hz
ON
RESET ALL
FEN
MUX
CONTROL
S&H MOD TIME
ANA MUX A
ANB MUX B
COS. I
COS. II
SIN. I
SIN. II
TO INTER FACE
TO SELECT I BYTE (SIN/COS)
TO SELECT II BYTE (SIN/COS)
S5
SI = AUTO/MAN
WFM RESET
AUTOMATICALLY
SYNCRONIZED
1ST
SERIAL
DATA
50 KHz
ON
CONTROL
1KHz
CLK FOR
MOD
CLK MODIFYING TIME
4 ADD TO 16 BIT MUX
A B C D
DATA MUX
MUX
DATA
OUT PUT
6 BYTE TIME
STN CODE
L.F
ATTN
BEAM
S.D.I.
SYNC
00 FF
OF OF
ANA MUX CONTROL
SIN.
COS.
S&H
A/D CONVERTER
1KHz AUTO
TSL
TSL
PERTEC
CONTROL
5 DATA
6 DATA
GO
FEN
WFM
WRITE BUFFER
CONTROL
LOGIC
R/W, R/F, F EN, WFM, ERASE
PERTEC
BMTT
A/B OVER FLOW
STATUS DISPLAY
FM HER
F F
NO. OF DATA RECORDS
PROJECT. DST-IS
DRAWN BY. A.H DESAI

FIG. 2

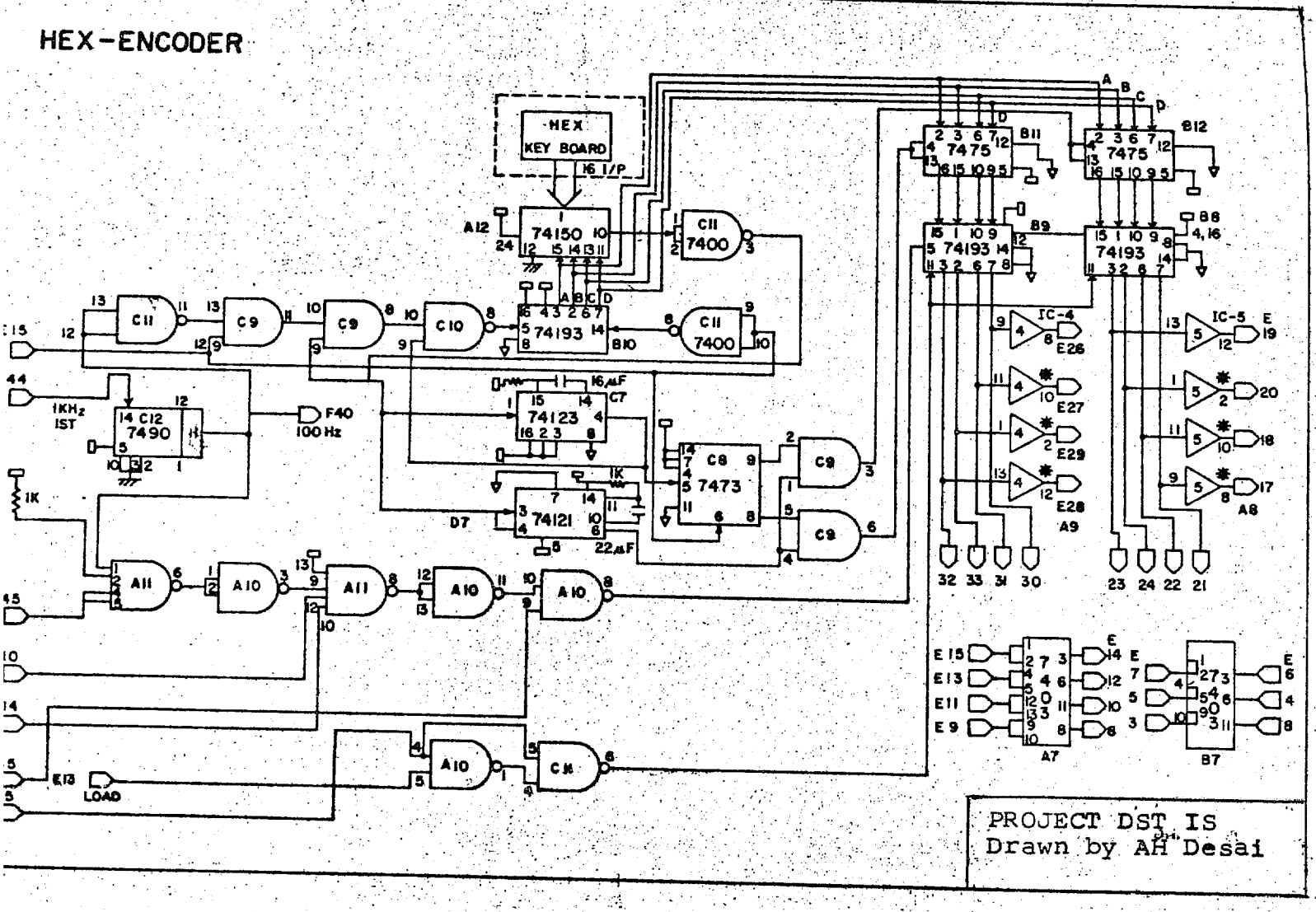

HEX-ENCODER
HEX KEY BOARD
16 I/P
74150
74193
74123
74121
7490
7475
7473
7400
1KHz IST
F40 100 Hz
1K
16 µF
22 µF
LOAD
PROJECT DST IS
Drawn by AH Desai

FIG. 3

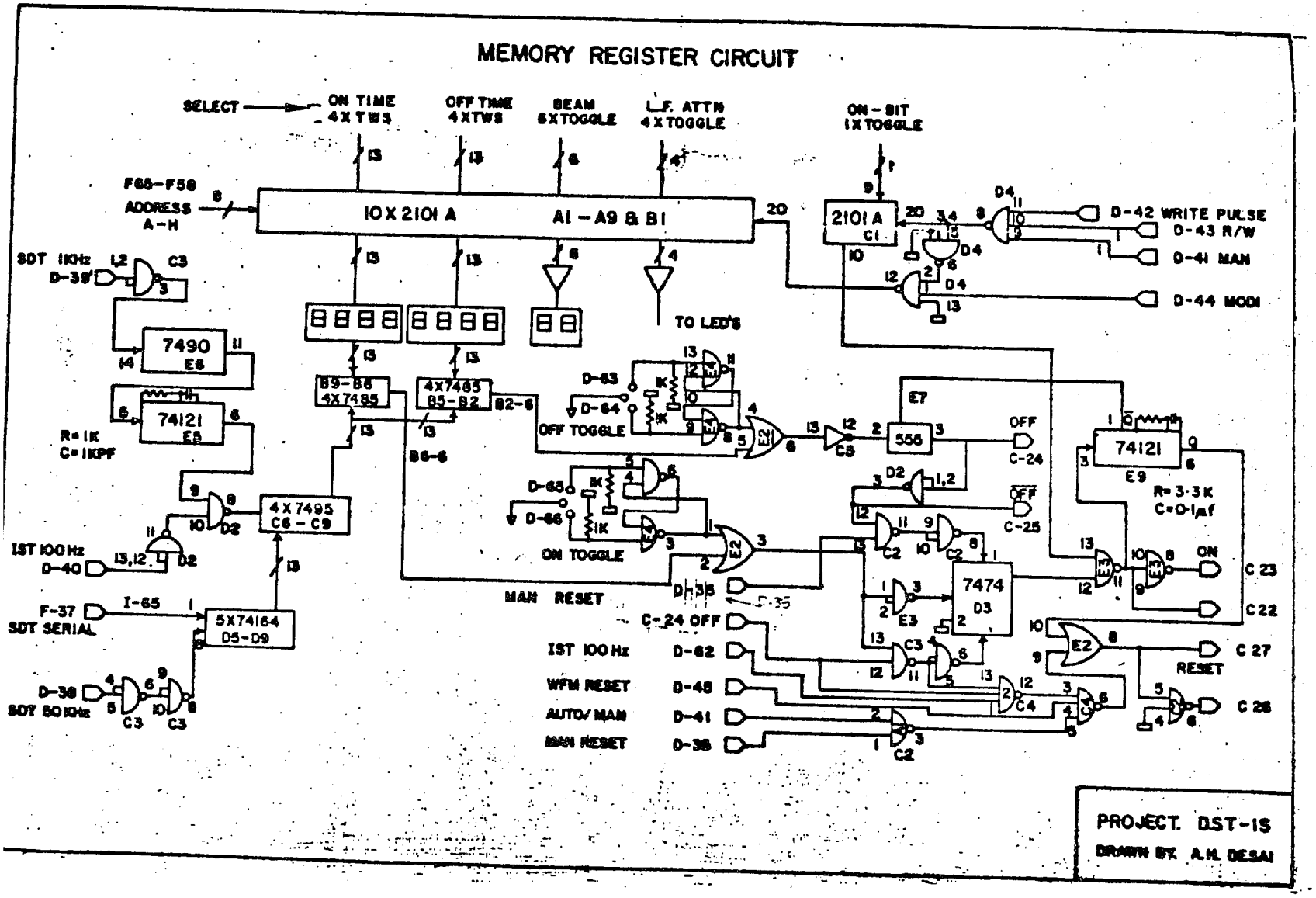

MEMORY REGISTER CIRCUIT
SELECT
ON TIME 4XTWS
OFF TIME 4XTWS
BEAM 6XTOGGLE
L.F. ATTN 4XTOGGLE
ON-BIT 1XTOGGLE
F68-F58 ADDRESS A-H
10X2101A
A1-A9 & B1
2101A C1
D-42 WRITE PULSE
D-43 R/W
D-41 MAN
D-44 MODI
TO LED'S
SDT 1KHz D-39
7490 E6
74121 E8
R=1K C=1KPF
B9-B6 4X7485
4X7485 B5-B2
B2-B
B6-B
D-63
D-64
OFF TOGGLE
D-65
D-66
ON TOGGLE
MAN RESET
D-35
E7
556
OFF
C-24
OFF
C-25
74121 E9
R=3.3K C=0.1μf
ON
C 23
C 22
7474 D3
RESET
C 27
C 26
4X7495 C6-C9
1ST 100Hz D-40
F-37 SDT SERIAL
I-65
5X74164 D5-D9
D-38 SDT 50KHz
C-24 OFF
1ST 100Hz D-62
WFM RESET D-48
AUTO/MAN D-41
MAN RESET D-36
PROJECT. DST-IS
DRAWN BY. A.H. DESAI

FIG. 4

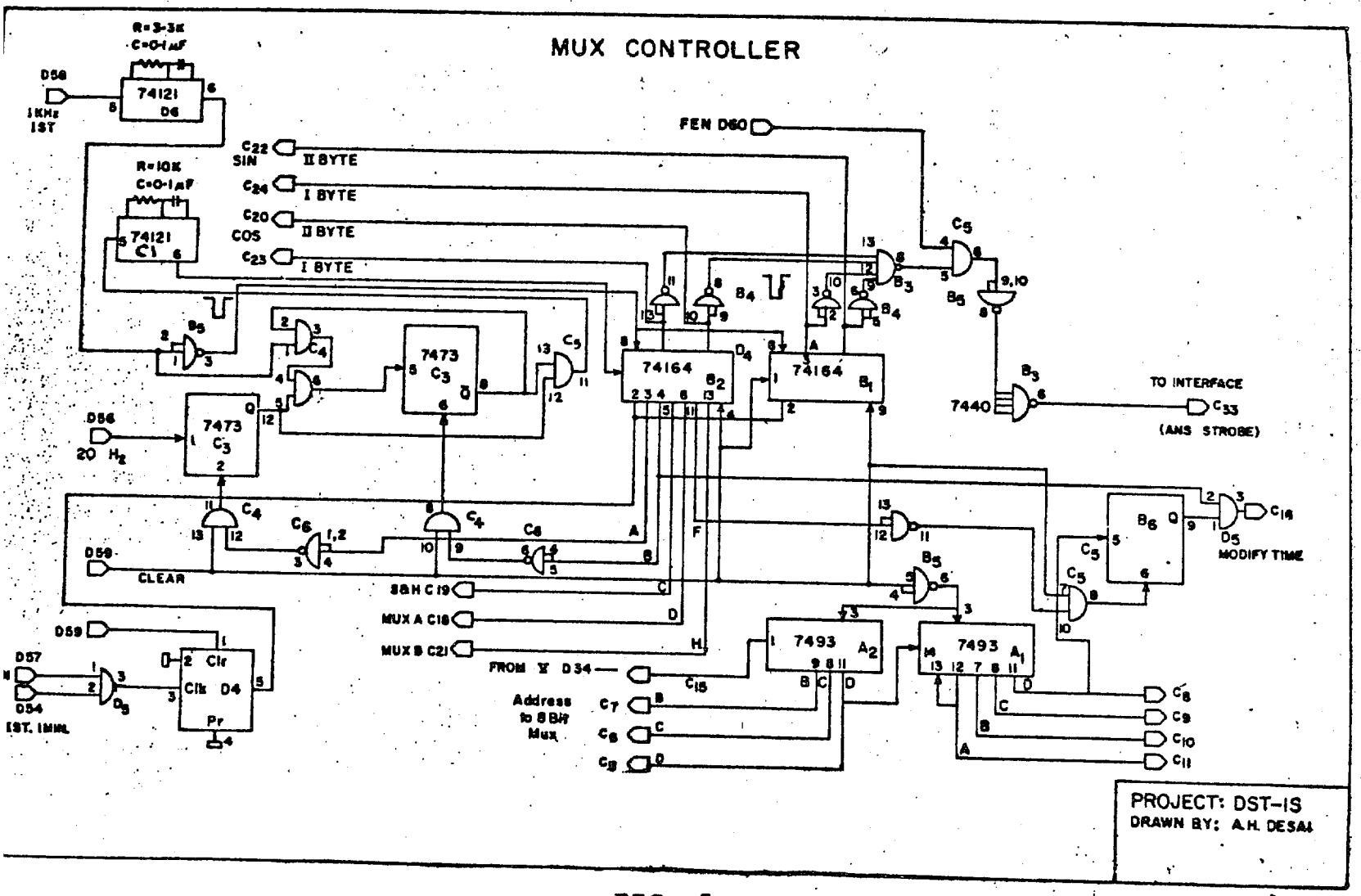

MUX CONTROLLER
R=3.3K
C=0.1μF
74121
D6
D58
1KHz
1ST
R=10K
C=0.1μF
74121
C1
FEN D60
C22
SIN
II BYTE
C24
I BYTE
C20
COS
II BYTE
C23
I BYTE
74164
B2
74164
B1
7473
C3
7473
C3
D56
20 Hz
D59
CLEAR
7440
TO INTERFACE
C33
(ANS STROBE)
B6
D5
MODIFY TIME
C14
S&H C19
MUX A C18
MUX B C21
FROM Y D34
C15
7493
A2
7493
A1
Address
to 8 Bit
Mux
C7
C8
C9
D57
D54
EST. IMM.
D59
C8
C9
C10
C11
PROJECT: DST-IS
DRAWN BY: A.H. DESAI

FIG. 5.

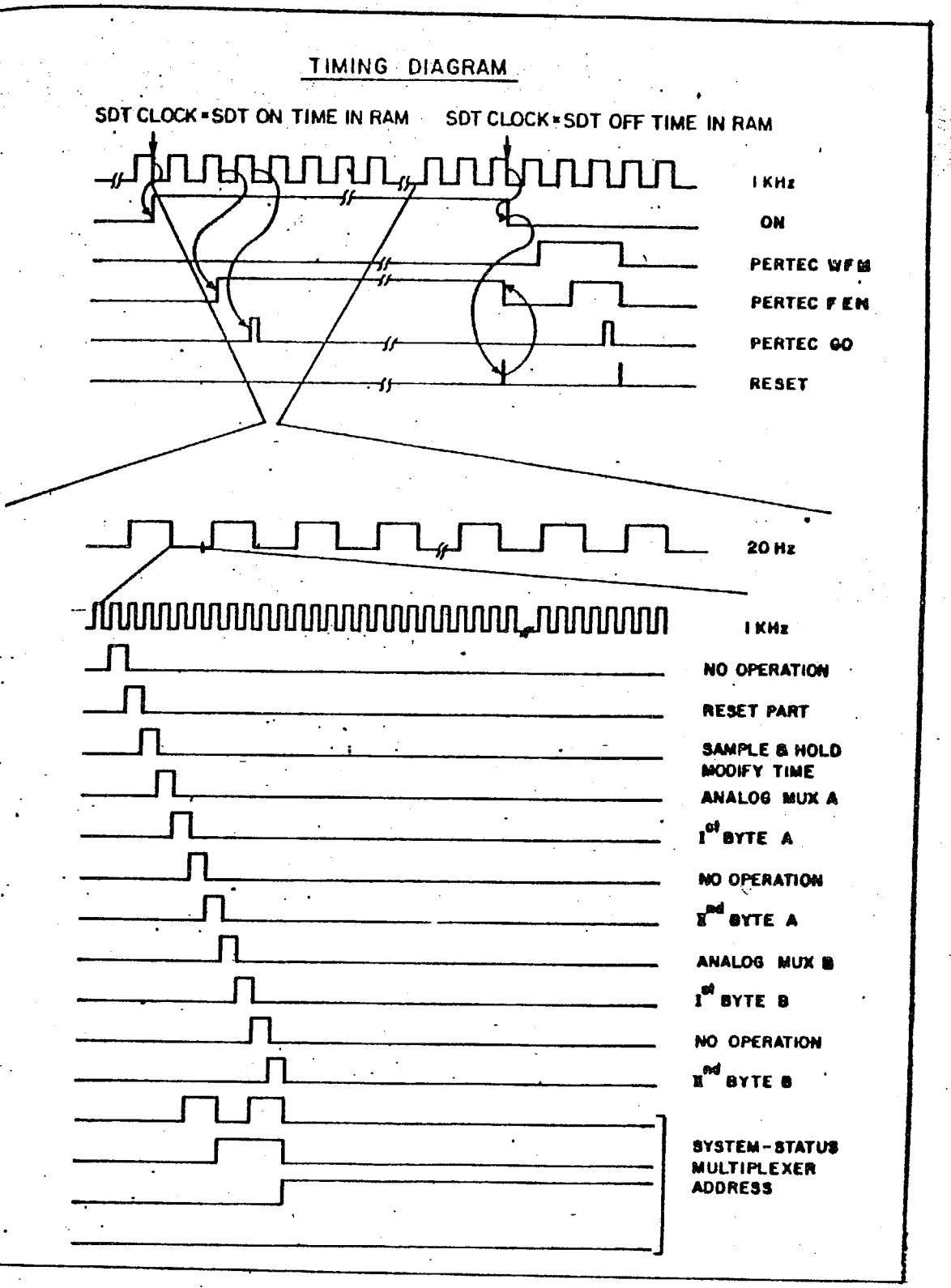

TIMING DIAGRAM
SDT CLOCK = SDT ON TIME IN RAM
SDT CLOCK = SDT OFF TIME IN RAM
1 KHz
ON
PERTEC WFM
PERTEC F EN
PERTEC GO
RESET
20 Hz
1 KHz
NO OPERATION
RESET PART
SAMPLE & HOLD MODIFY TIME
ANALOG MUX A
I st BYTE A
NO OPERATION
II nd BYTE A
ANALOG MUX B
I st BYTE B
NO OPERATION
II nd BYTE B
SYSTEM-STATUS MULTIPLEXER ADDRESS

Fig. 6

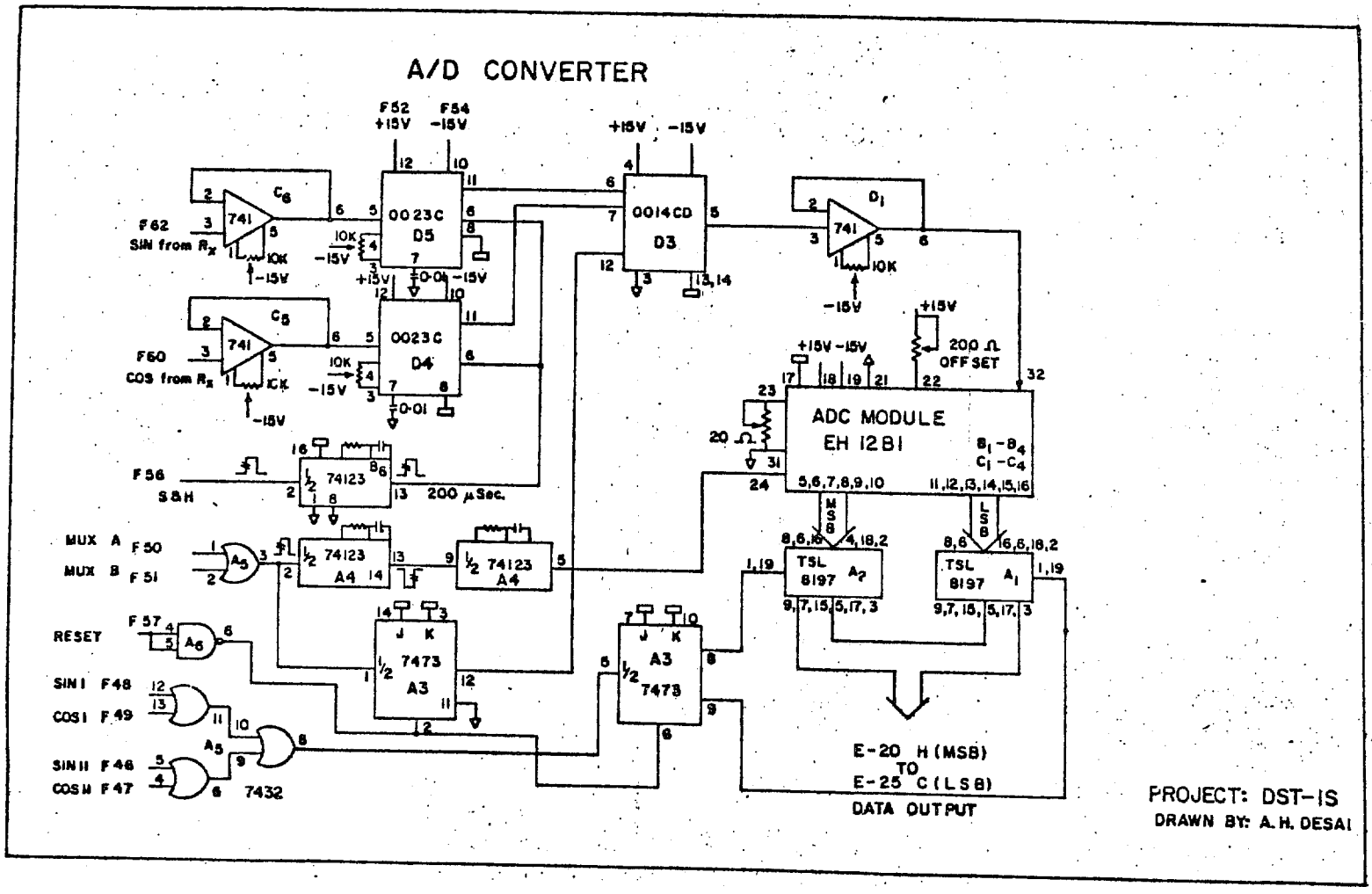

A/D CONVERTER
F52 +15V
F54 -15V
+15V
-15V
C6
741
F62
SIN from Rx
10K
-15V
0023C
D5
0014CD
D3
D1
C5
F60
COS from Rx
D4
0.01
200 Ω OFFSET
ADC MODULE
EH 12B1
20 Ω
F56
S&H
74123
B6
200 μSec.
MUX A F50
MUX B F51
A5
A4
RESET
F57
A6
7473
A3
SIN I F48
COS I F49
SIN II F46
COS II F47
7432
TSL 8197 A2
TSL 8197 A1
MSB
LSB
E-20 H (MSB)
TO
E-25 C (LSB)
DATA OUTPUT
PROJECT: DST-IS
DRAWN BY: A. H. DESAI

FIG. 7

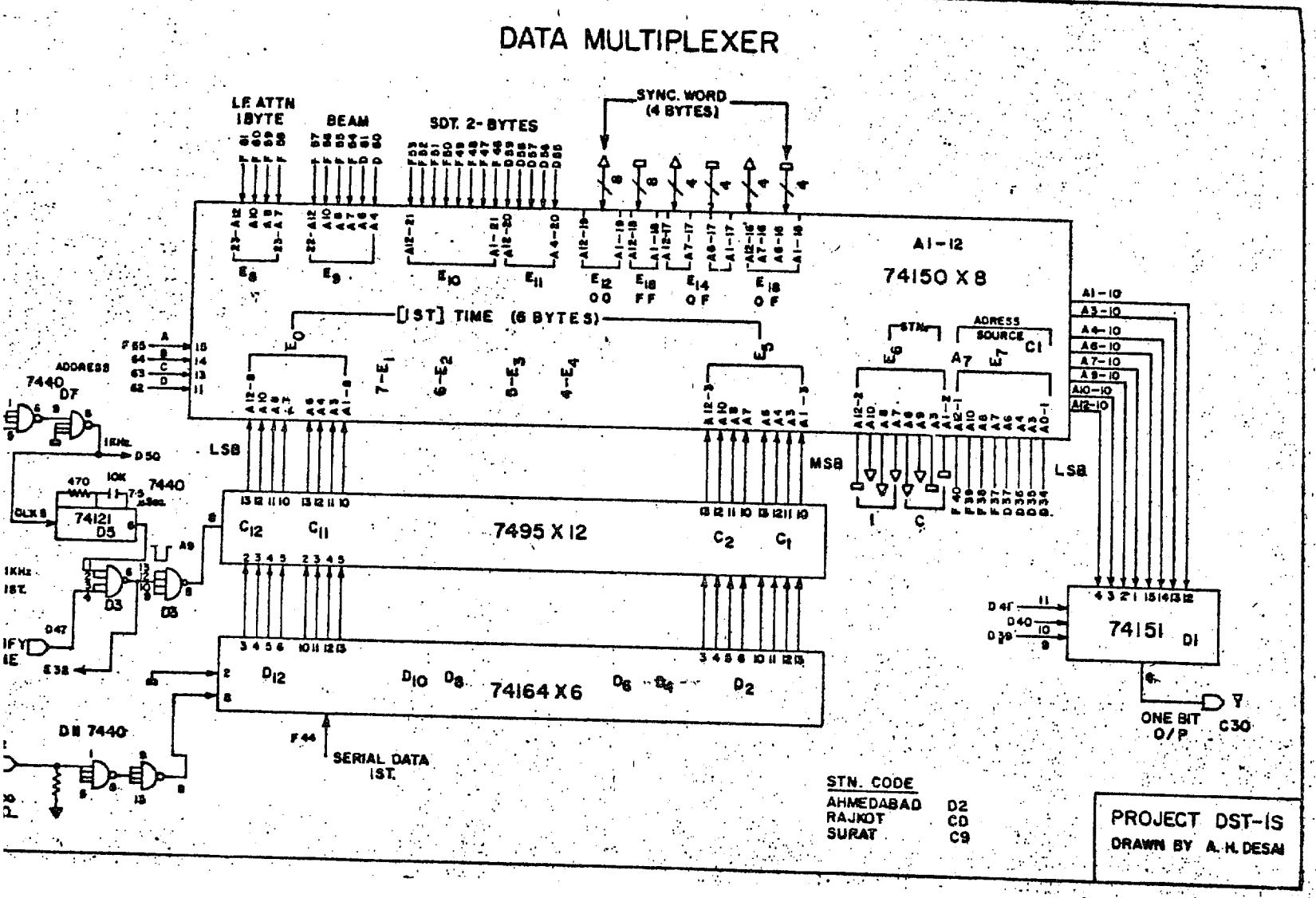

DATA MULTIPLEXER
LF ATTN 1BYTE
BEAM
SDT. 2-BYTES
SYNC. WORD (4 BYTES)
A1-12
74150 X 8
[IST] TIME (6 BYTES)
ADDRESS
7440 D7
LSB
MSB
7495 X 12
74164 X 6
74121 D5
7440
D3
D5
D8 7440
74151 D1
ONE BIT O/P
C30
SERIAL DATA IST.
STN. CODE
AHMEDABAD D2
RAJKOT C0
SURAT C9
PROJECT DST-IS
DRAWN BY A. H. DESAI

FIG. 8

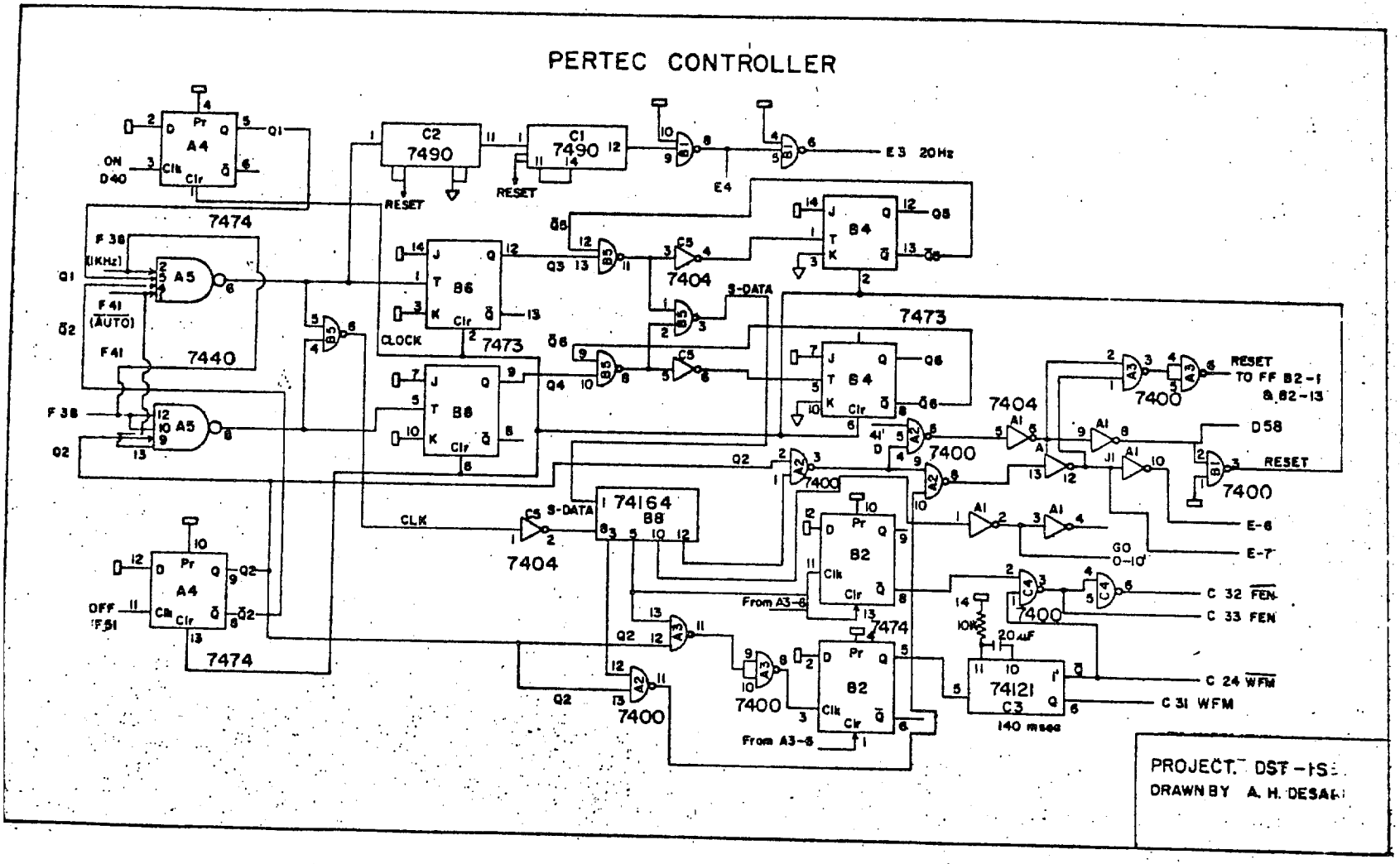

PERTEC CONTROLLER
A4
7474
ON
D40
F 38
(1KHz)
F 41
(AUTO)
F41
A5
7440
Q1
Q2
C2
7490
C1
7490
RESET
E3 20Hz
E4
B6
B4
B8
7473
Q3
Q4
Q5
Q6
7404
S-DATA
CLOCK
74164
B8
CLK
7400
RESET
TO FF B2-1
& B2-13
D58
RESET
E-6
E-7
GO
0-10
B2
From A3-6
C 32 FEN
C 33 FEN
10K
20 uF
74121
C3
140 msec
C 24 WFM
C 31 WFM
OFF
(F51)
PROJECT: DST-1S
DRAWN BY A. H. DESAI

FIG. 9

CONTROL SIG. GEN.
(PERTEC)

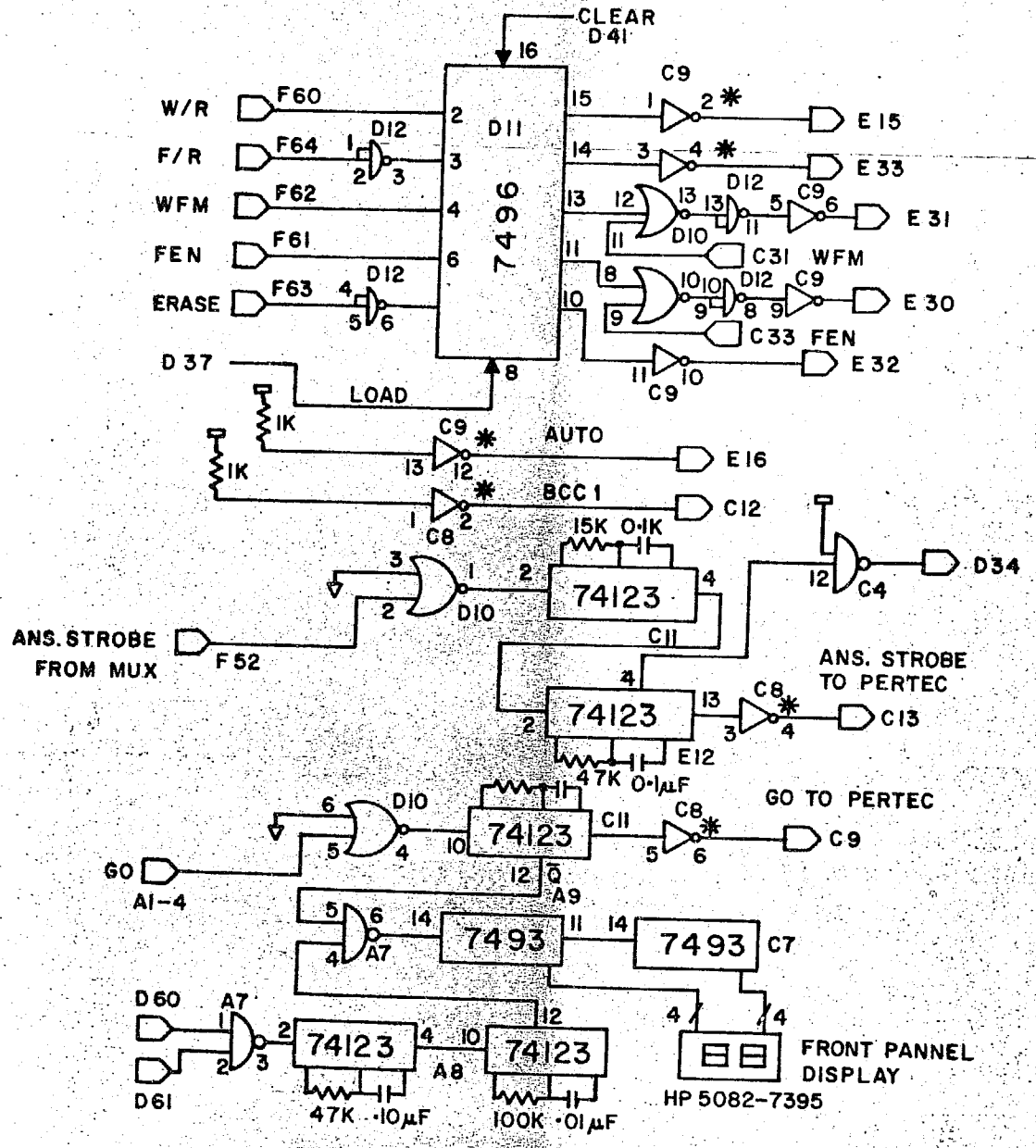


Fig. 10.

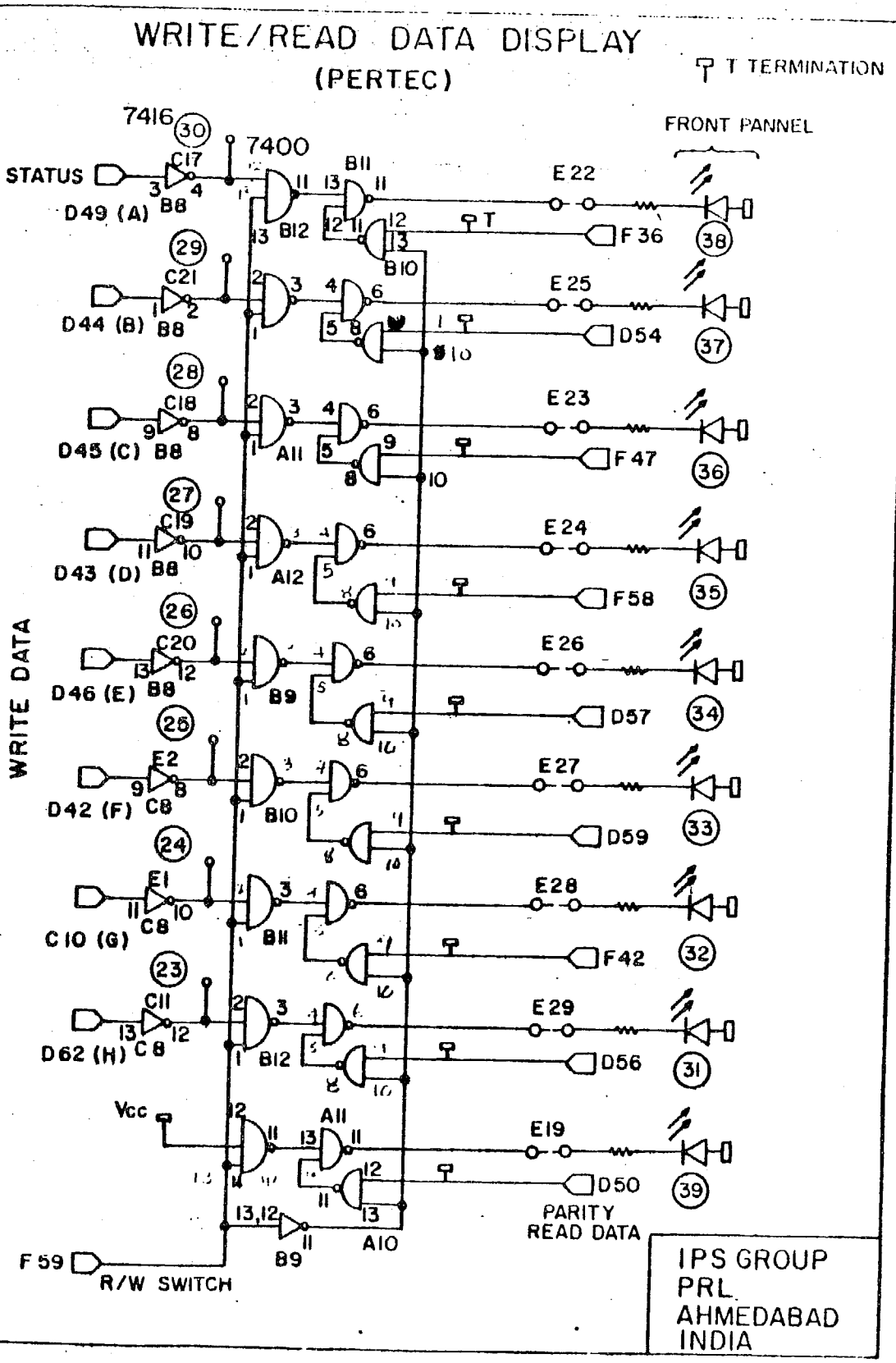
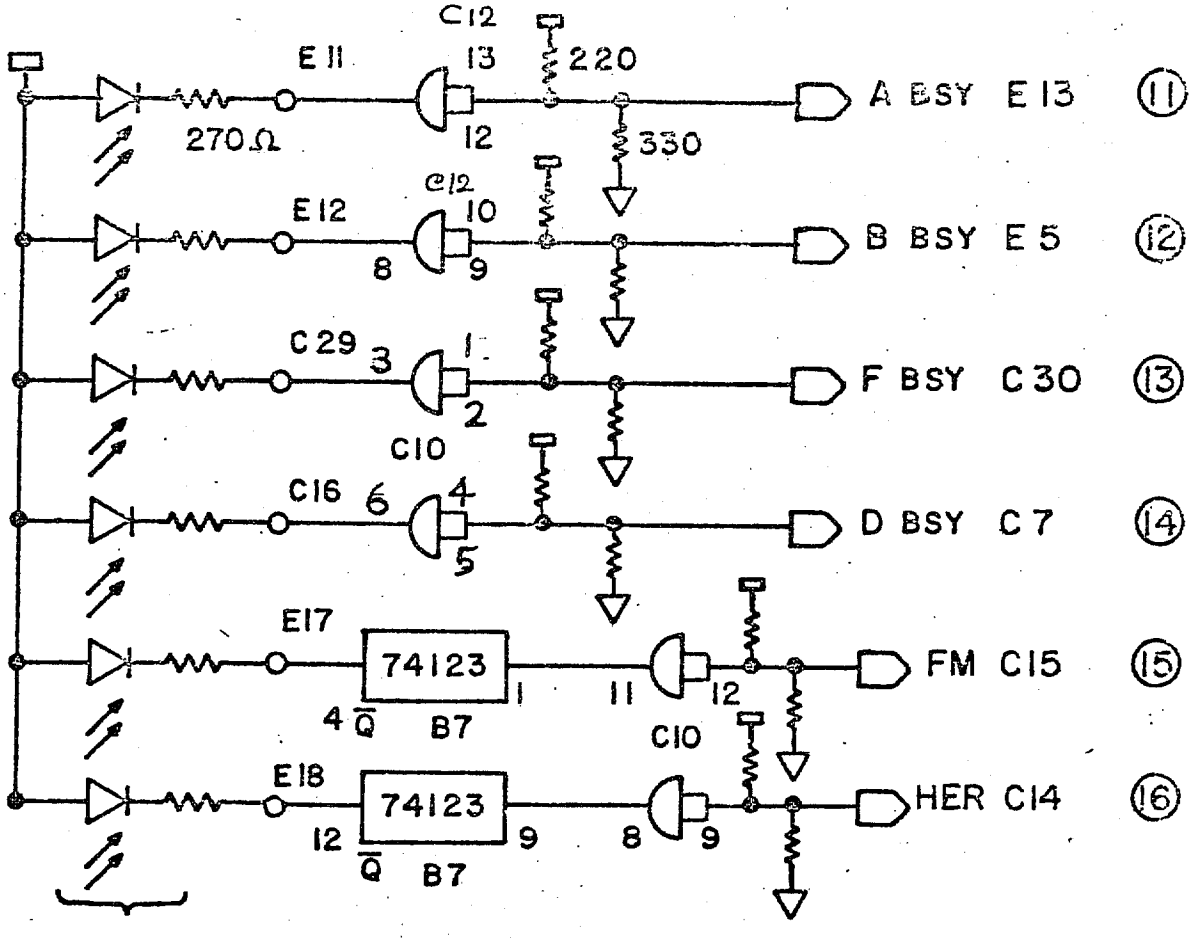

WRITE/READ DATA DISPLAY
(PERTEC)
T TERMINATION
FRONT PANNEL
7416
7400
STATUS
D49 (A) B8
D44 (B) B8
D45 (C) B8
D43 (D) B8
D46 (E) B8
D42 (F) C8
C10 (G)
D62 (H) C8
Vcc
F59
R/W SWITCH
WRITE DATA
PARITY
READ DATA
E22
E25
E23
E24
E26
E27
E28
E29
E19
F36
D54
F47
F58
D57
D59
F42
D56
D50
IPS GROUP
PRL
AHMEDABAD
INDIA

FIG. 11

STATUS DISPLAY (PERTEC)



Note: ◯ Stands for 50-Pin Connector

FIG. 12

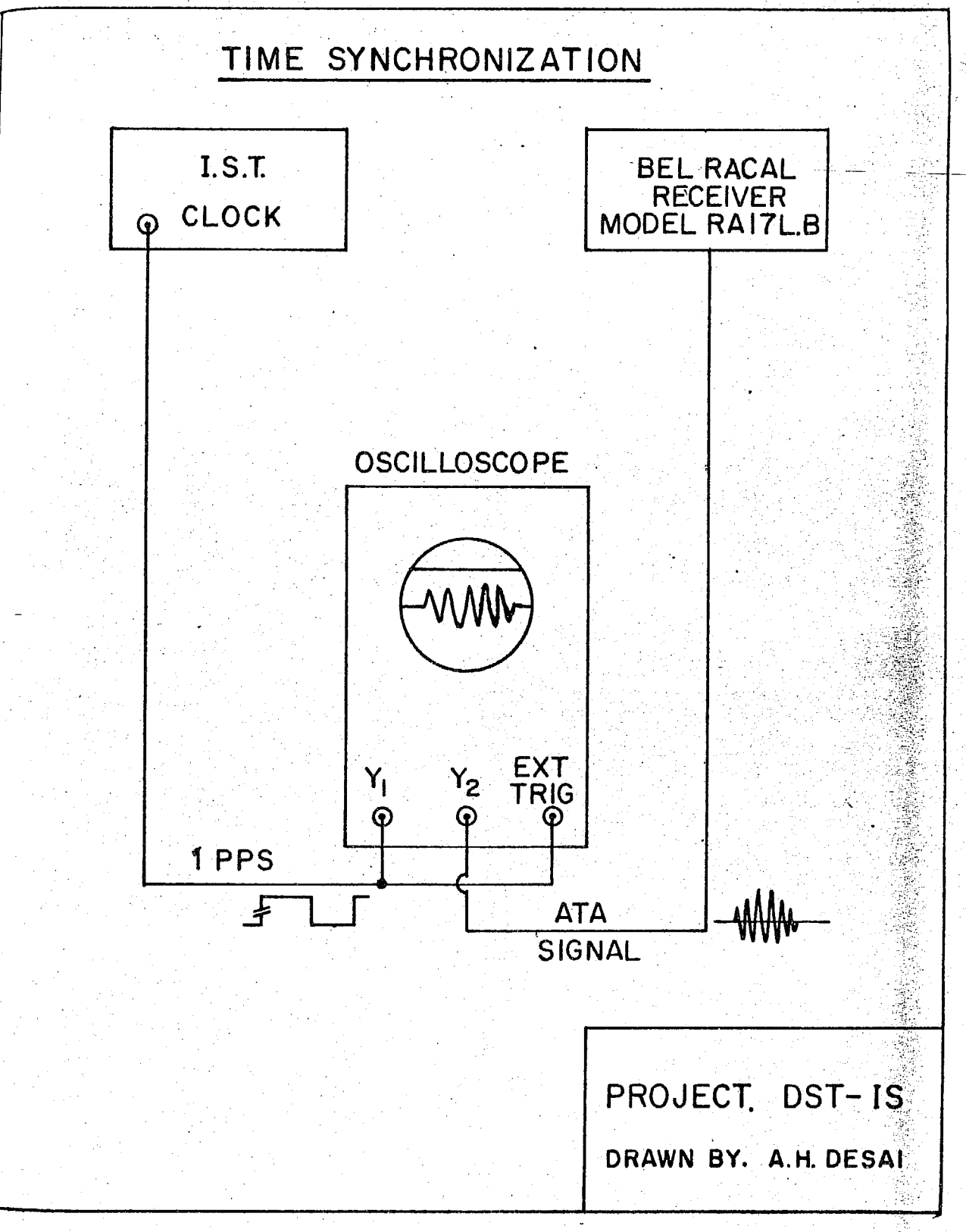

TIME SYNCHRONIZATION
I.S.T.
CLOCK
BEL RACAL
RECEIVER
MODEL RA17L.B
OSCILLOSCOPE
Y1
Y2
EXT
TRIG
1 PPS
ATA
SIGNAL
PROJECT. DST-IS
DRAWN BY. A.H. DESAI

FIG. 13

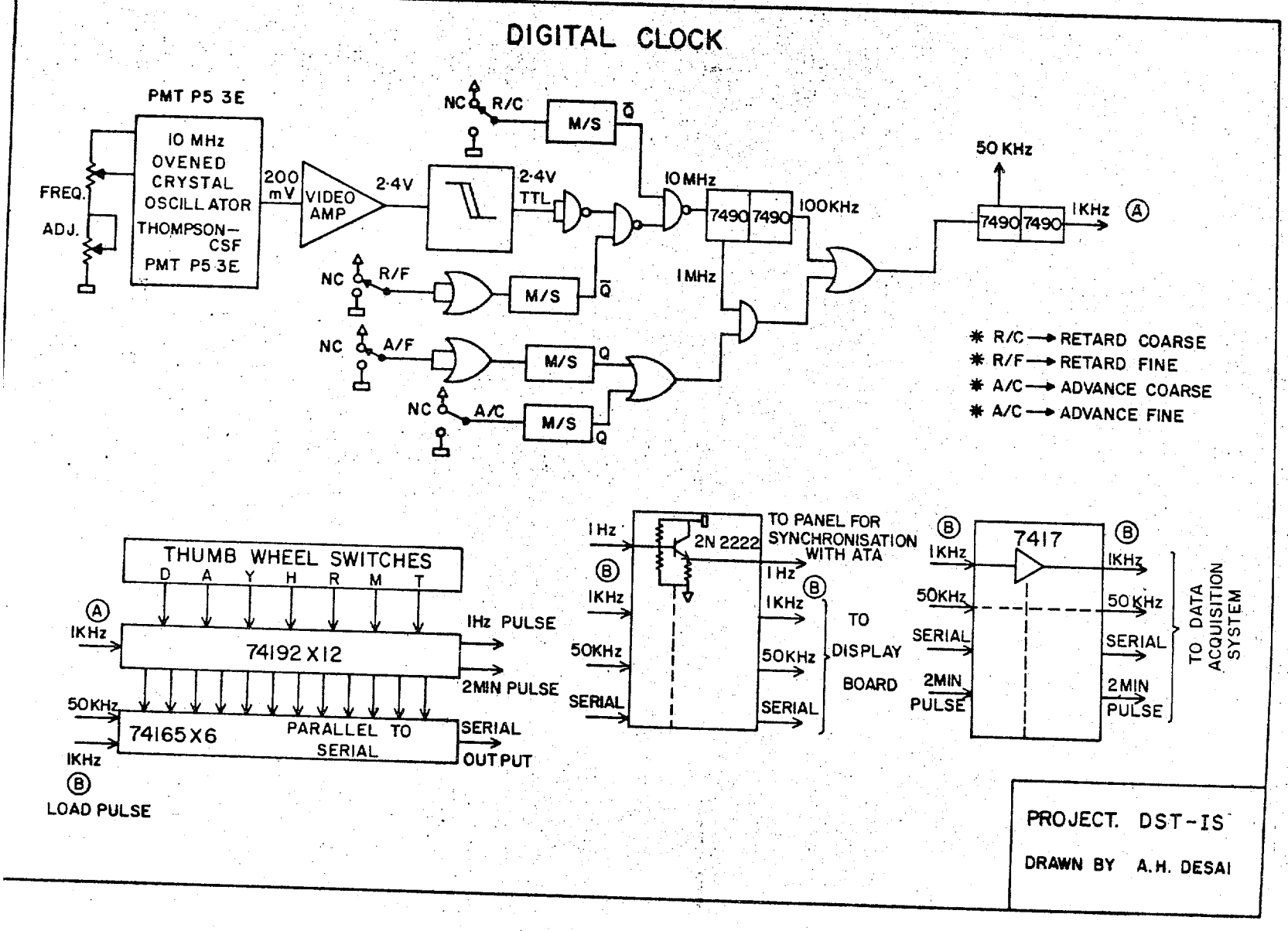

DIGITAL CLOCK
PMT P5 3E
10 MHz OVENED CRYSTAL OSCILLATOR THOMPSON–CSF PMT P5 3E
FREQ. ADJ.
200 mV
VIDEO AMP
2·4V
2·4V TTL
NC R/C
M/S
NC R/F
M/S
NC A/F
M/S
NC A/C
M/S
10 MHz
1 MHz
7490 7490
100 KHz
50 KHz
1 KHz
* R/C → RETARD COARSE
* R/F → RETARD FINE
* A/C → ADVANCE COARSE
* A/C → ADVANCE FINE
THUMB WHEEL SWITCHES
D A Y H R M T
74192 X12
74165 X6
PARALLEL TO SERIAL
1Hz PULSE
2MIN PULSE
SERIAL OUTPUT
LOAD PULSE
1Hz
2N 2222
TO PANEL FOR SYNCHRONISATION WITH ATA
TO DISPLAY BOARD
7417
TO DATA ACQUISITION SYSTEM
PROJECT. DST-IS
DRAWN BY A.H. DESAI

FIG. 14

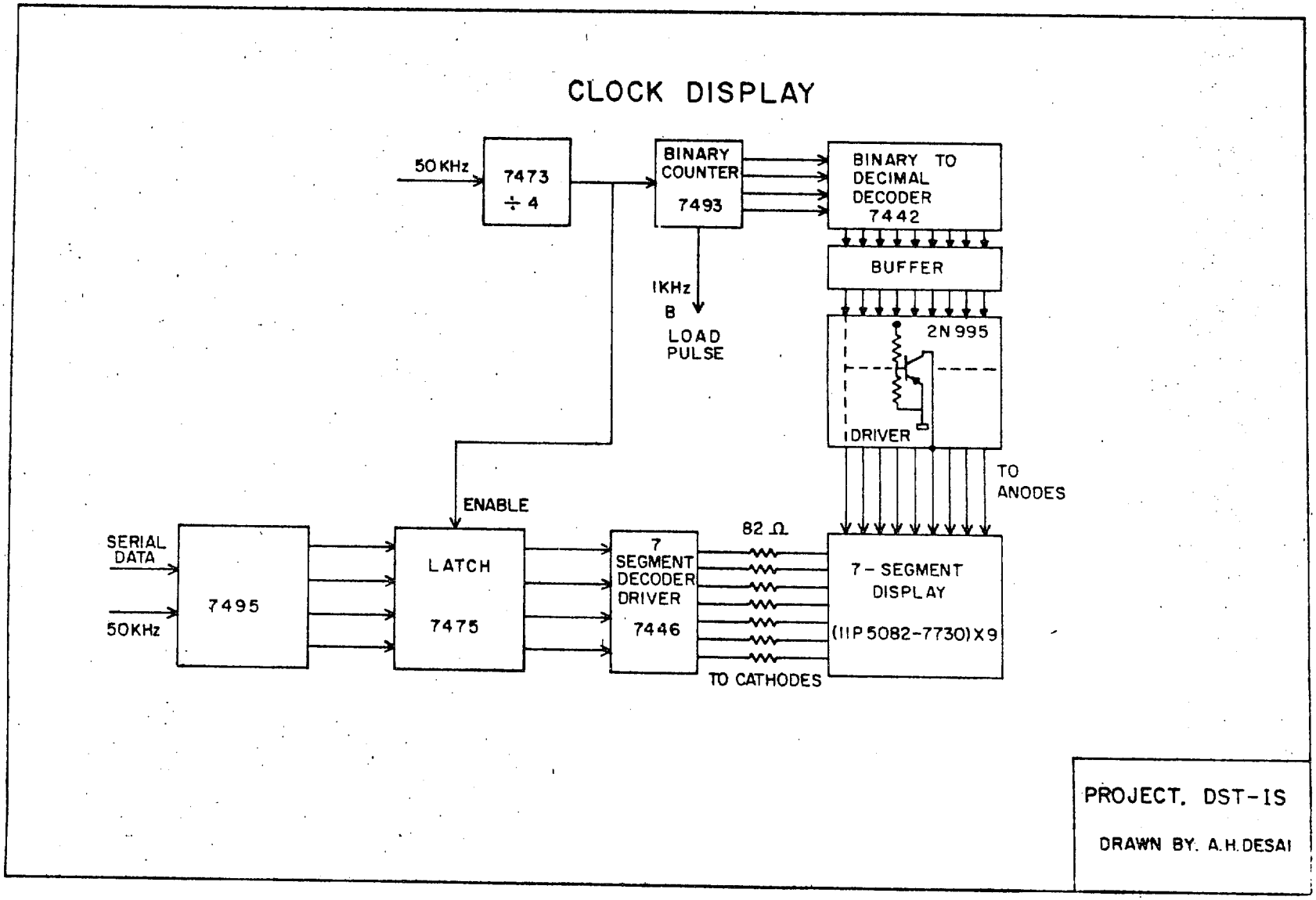

CLOCK DISPLAY
50 KHz
7473
÷ 4
BINARY
COUNTER
7493
BINARY TO
DECIMAL
DECODER
7442
BUFFER
1KHz
B
LOAD
PULSE
2N995
DRIVER
TO
ANODES
ENABLE
SERIAL
DATA
50KHz
7495
LATCH
7475
7
SEGMENT
DECODER
DRIVER
7446
82 Ω
7 - SEGMENT
DISPLAY
(IIP5082-7730)X9
TO CATHODES
PROJECT. DST-IS
DRAWN BY. A.H.DESAI

FIG. 15