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A LOW COST TOUCH KEYBOARD CRT TERMINAL

by

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12. Abstract	:	Design and fabrication details of a touch keyboard CRT Terminal have been described. It uses an 12"/14" domestic TV receiver as display device and has mains and printer ports with RS-232C interface. It can be used in LOCAL, ON LINE and intelligent modes. In the letter mode it can be used for development of programme for 8085A micro-processor.
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A LOW COST TOUCH KEYBOARD CRT TERMINAL

Abstract

A CRT terminal has become the most important computer peripheral. Being totally electronic, this instrument has a lower failure rate as compared to the printing terminals like teleprinter and saves on stationery. The microcomputer has taken a central place in all types of instrumentation where it serves the need for all types of controls and data acquisition. The CRT terminal is utilized for the purpose of data/program entry and data presentation. The modern LSI's have made realisation of advanced features in the CRT terminals a simple affair. The cost of these terminals has also gone down in the recent past. However, the price of a CRT terminal is still quite high in the Indian market. The need for a large number of CRT terminals has inspired the authors to design a functional CRT terminal at a low cost. A CRT terminal based on the components easily available in the local market, and that uses an ordinary TV receiver as the display device, has been described in this document. It has been an endeavour of the authors that this document should serve as the base material for the basic understanding of the CRT terminals, as well as, have sufficient details to enable an average reader to fabricate his own.

Introduction

Invention of microprocessors has revolutionalized the field of computers and electronics. Small computers have been available to the average user at a cost of as low as Rs.1,000/-. These used an average TV receiven as the display device and could display 40 characters of 24 lines. Some of them had the facility of being used as CRT terminal. Now this product is on the decline in the west and manufacturers have shifted their attention to costlier products. Indian scene is very bleak even now and a few personal computers which are available in the Indian market cost anywhere above Rs. 5,000/-.

The CRT terminals are not very different in internal circuitry from personal computers and their cost should therefore be just the sum of the cost of a TV and a personal computer barring the ones with advanced features. However, a low cost functional CRT terminal is not available in the Indian market and an average product costs between Rs.20,000/- to Rs. 35,000/-.

There are many applications where a functional CRT terminal of average performance would be acceptable. Keeping this area in mind a cost effective CRT terminal has been designed and which is described in the following pages.

2. Design

The block diagram of the touch switch terminal has been given in Fig.1. The CRT terminal consists of three major parts;

1. Keyboard,
2. Display
3. Control

The keyboard should have about 60 keys for alpha-numeric and control characters and is, due to the mechanical nature of key-switches, to the most failure prone section. A new touch switch type keyboard has been designed which relies on the skin resistance of the operators fingers for the contact closure and thus does not have any moving part at all. The design of the keyboard has been described adequately elsewhere[1].

The Display: Ordinary 12" TV receiver is the most cost effective display device available today and, if the video signal is connected directly to the video amplifier, it can display 64 to 80 characters per line. Quite a few types of video display generator ICs are available in the market, but they are still very costly, costing around Rs.200/-. A design published earlier[2] has been chosen for the display controller which has the advantage of using readily available medium scale integrated circuits. However, it limits the programmability of the present design to 40 x 24 or 80 x 24 format of alpha-numeric characters.

Control: A 8085A based microcomputer has been used for this control function. Keyboard and band rate selection switches are connected to ports and the video display board is connected to the microprocessor bus.

3. Video Display Generator

The popular format for alpha-numeric displays is of 24 rows of 40 or 80 columns. Here it is worth noticing that the coverage text on Quartorsize paper (regular sunlit bond paper) consists of about 24 - 26 rows of 60-64 characters. The terminal described here can display 24 rows of 40 or 80 columns.

The video display generator has been designed to interface to TV receivers conforming to CCIR-B standard. Salient features of the system relevant to the design have been given below:

Horizontal scan frequency	15625 Hz
Frame Rate	50 Hz
No. of lines per field	625
Active line period	52 μ sec
Horizontal sync pulse width	4 μ sec

It may be noted that the above standard utilizes interlaced scanning and therefore each frame consists of only 312.5 lines. However, the video display interface has been

designed for noninterlaced operation and each frame consists of 320 lines. The number chosen here is very close to that used in TV broadcasting and any slight deviation in vertical scan frequency will be taken care of by synchronization circuits in the TV receivers.

During the vertical retrace quite a few horizontal lines are blanked and the average TV receiver has some overscan to take care of component mismatch in production and, or degradation with time. Therefore the actual number of lines scan on the TV could only be about 500-550. In case of non-interlaced display the number of lines is accordingly about 250. Similarly some margin has to be left on both the sides and therefore active horizontal scan period is less than 48 μ sec. Here a figure of 40 matches very well to our proposed formats of 40/80 column display. And in such a case each character would occupy 1 or 0.5 μ sec. respectively.

A 5 x 7 matrix is adequate to display all the printable ASCII characters and hence it has been chosen for our display. Each character occupies 6 x 10 pixed space on the screen, out of which one pixel gap is utilized for inter character gap and 3 lines are blanked out between each character to improve readability of text. Total 240 scan lines are used for the display and 40 lines are blanked out before and after the

vertical sync to take care of overscan. The display structure has been shown in Fig.2. In some TVs even this much margin may not be sufficient resulting in first or the last line of characters going out of screen. In that case the vertical scan current can be reduced a little. This is usually a preset pot in TV's and can be accassed after opening the back.

As each character is formed by six horizontal elements, the basic dot clock frequency is 6 MHz for 40 column display and 12 MHz for 80 column display. This would generate a video signal of 3 and 6 MHz bandwidth respectively. Video bandwidth of an average TV receiver is about 3-4 MHz and 40 column display would pose no problem. However, video signal would have to be fed to the grid of the picture tube through separate amplifier for 80 column display. If we use 48 μ seconds of the horizontal scan a dot clock of 8 MHz would provide a display format of 64 x 24 which is quite OK for most of word processor applications for the reason stated earlier. 80 column option can be implemented by following the instructions given in Apprndix A.

The circuit of the video display generator is slightly complex and therefore it has been split into the following two functional parts :

A. Sync and Address generator.

B. Display RAM, character generator and microcomputer bus interface.

A. Sync and Address Generator

The circuit diagram of this part has been given in Fig.5. Dot clock frequency of 6 MHz has been generated with the popular NAND gate oscillator. This clock is fed to a divide by 6 counter, realised by a part of 7492. The three outputs of this counter are fed to a 3 input NAND gets to generate the load pulse for the parallel to serial converter. This pulse train is the character clock (1MHz) and it is in turn fed to a 6 bit binnary counter consisting of 3 bit parts of two 7493 ICs. The outputs of this counter chain are fed to a decoder circuit realised by NAND gates and inverters to generate the horizontal sync and horizontal blanking signals. The final output of this chain is at the horizontal scan rate (15, 625 KHz) and it is divided by 320 with the help of one decade and one 5 bit binary counter to generate the frame rate of about 50 Hz at the output. The outputs of the binary counter in the vertical count down chain are decoded to generate the vertical blanking and vertical sync signals. The various wave forms of the circuit have been given in Fig.3 & 4. An interesting possibility is the use of 6.144 MHz dot clock, in which case the frame rate becomes exactly 50 Hz and the resulting display is almost flicker free. The horizontal and vertical sync pulses are fed to an exclusive OR gate to generate the composite sync. The video signal

obtained at the serial output of parallel to serial converter 74165 and the composite sync signals are combined in a transistor mixer to generate a composite video signal. This signal can be connected to the video input of a domestic TV receiver.

A six bit counter chain which is also driven by character clock is enabled during the line scan period with the help of horizontal blanking signal, and generates the low order addresses A0 through A5 for the display RAM. The outputs of first 3 bits of the decade counters 7490 act as the line counter for character generator and the 'D' output is used for interline blanking. The 5 bit outputs of the binary counter in the vertical count down chain act as the high order addresses A6 through A11. It is worth noting that the various Video Display Generators available in the market do the job described above. Their advantages are the programmability of the format.

B. Display RAM, character generator and microprocessor bus interface:

The circuit diagram of this part has been given in Fig.6. The display RAM stores the data to be displayed on the screen. It is accessed by the address generator described above most of the time and by the microprocessor through the bus during the time when data is being read/written into it. The outputs of character counter and the

row counter are total 11 and therefore a display RAM of 2Kx8 is needed. Static RAM type 6116 has been used for this purpose. The address lines generated by character and row counters and the address lines A0-A11 of the microprocessor bus are multiplexed with the help of three QUAD-TWO to ONE multiplexer type 74LS157. Two data bus buffers type 8216 have been used to interface the RAM output lines to the microprocessor data bus. The RAM has been assigned a memory space starting at F000(H) and can be read/written by the microprocessor. Normally the display RAM is continuously accessed by the display generator and its outputs D0-D6 are fed to the address lines A3-A9 of the characters generator which itself is a 2716 EPROM. 7 data lines are sufficient as the total number of displayable characters are about 96 only. Address lines A0-A2 of the character generator are driven by the line counter output L0, L1 and L2. The output D0-D5 of the character generator are fed to the six inputs. A to F of 8 input parallel to serial shift register type 74165 whose serial output at pin 7 is the video signal.

A 3 to 8 decoder type 74LS138 has been used for address selection of display RAM. It is gated by MW + $\overline{MR}$ signals and its output $\overline{O_8}$ has been used to enable 8216. The same output is inverted to generate control signal for the address multiplexer type 74LS157. $\overline{O_8}$. $\overline{MW}$ signal controls the outputs of 6116 and data direction of 8216. The elaborate decoding

is needed to avoid interaction of I/O devices with display RAM. The video display generator circuit has been accommodated on a double sided printed circuit board. The artwork layout has been given in Fig.12. The list of components has been given in Appendix-B.

4. The Control Unit

A microcomputer based on the popular microprocessor 8085A has been used for the control of the terminal. The printed circuit board of this unit is also of the same size as that of Video Display Generator, about 6" x 4" and these are interconnected to each other with the help of 44 line bus. The bus signals have been given in the Appendix-C. A 0.1" pitch 44 pin connector has been utilized for I/O and hardware interrupt lines. The signals on this connector have been listed in Apprndix-D.

The microcomputer operates at a clock frequency of 6.144 MHz and has facilities of two serial I/O, two 8 bit and one six bit parallel I/O port, 4 programmable timers and 4.25K RAM and 4/8K EPROM. Multi-function circuit type 8155 has been used for parallel I/O, 14 bit timer and 256 byte RAM. Three timers and serial I/O have been implemented by 8253 and 8251 respectively. 8212 latch has been used for separating data and address lines and two 74LS138 IC's have been utilized for address decoding and generation of Separate Memory and I/O Read/Write signals

from the IO/$\overline{M}$, $\overline{WR}$ & $\overline{RD}$ signals available on 8085A (Fig.8). Ready, S0 and S1 signals are not used very often, therefore they have not been brought out on the bus. However, there are 4 uncommitted lines on the bus connector which can be utilized for such signals. Memory and I/O map of the systems has been given in the Fig.7. The circuit diagram of the microcomputer board has been given in Figs.5 & 6. There is provision for two EPROM type 2716 in the two 24 pin sockets on the left and 2SRAMS type 6116 on the remaining two sockets. This microcomputer can be utilized for any other control applications as such and EPROM type 2732 can be substituted in place of 2716 after making the modifications given in Appendix-E. The PCB artwork of the microcomputer and the list of components have been given in Fig.13 and Appendix-F respectively.

5. Interface Details

As stated earlier, the terminal can operate in one of the three modes, local, line and intelligent. In the last mode it can be used as an 8085A based small microcomputer for program development. These modes are selected by two D/P switches which are connected to C4 and C5 lines of Port-C. The baud rate for the printer can be controlled by another set of D/P switches connected to B0 & B1 lines of port-B. The keyboard is connected to port-A, and baud rate of terminal can

be controlled by separate D/P switches connected to C0-C2 lines of Port-C. The baud rate clock is generated internally in the timer of 8155. Timer 8253 has not been used in the system and it can be utilized for any other purpose. Similarly the hardware interrupt lines RST 5.5, RST 6.5, RST 7.5 and TRAP, serial input line SID and interrupt line are also free. These have been terminated on the connector by 15K to avoid any malfunction.

6. Other Miscellaneous Hardware Details

The video display generator board and the microcomputer boards have been interconnected through a back plane printed board and the whole assembly is housed in a card frame. A conventional power supply has been used for feeding the various voltages to the system. TTL /RS232C level conversion is done with the help of discrete devices. The unused interrupt lines have been terminated to ground through 15K resistors. The power supply and TTL/RS232C converter circuits have been accommodated on a separate printed board. All the hardware has been accommodated in a small enclosureof 360 x 415 x 110 m size (W x D x H). The various controls and connectors have been located on the rear panel. The keyboard which is a fibreglass printed circuit board has been mounted with a gentle slope for ease of operation. The circuit diagram of the power supply and level converters have been given in Fig.15. The enclosure dimensions and location of various parts have been shown in Fig.16.

7. Software

After each power on or reset operation the initialization of the ports and baud rate clock takes place. The program tests the mode selection switches at 003F and branches to 0050 for line mode, 00B4 for local mode and 03FA for intelligent mode. The program from 03FA to 07FF is similar to SDK-85 monitor program. The stack has been changed to 20AD and the 'CI' (Character IN) and 'CO' (Character OUT) sub-routines have been replaced by keyboard read and character display routines. Keyboard read routine provides a delay and branches to a keyboard flag test program to check for any character present. It loops on itself in the absence of characters but if character is present it returns to caller with character in A, before returning to caller it tests if CRTL 'N' or CRTL 'O' have been pressed. In case of former the contents of screen are printed through the printer port. While the latter branches back to intelligent mode. As this keyboard input subroutine is used for all the operations, CRTL 'N' and CRTL 'O' are effective in all modes of operation.

Character display routine accepts an ASCII character from C and tests for control character (00-1F) or displayable character (20 - 7F). Appropriation action is taken accordingly. The bulk of display program is located from 0100-01FF.

SOD line has been utilized for driving the printer port. The subroutine for character out is located at 00C7(H) while the printer program is located at 0087(H) which copies the display information.

The disassembled monitor program from 0004 to 03F9 and keyboard IN and character display routines located from 0590 to 05E9 have been given in appendix I. The rest of the program is similar to the monitor program of SDK-85 kit. Addresses of various subroutines has been given in Table-I.

8. Operation

After every reset operation and after power on the microprocessor scans the C4 C5 lines of port C., and selects the mode as given in appendix E. Baud rate of the RS232C interface is also set during this sequence according to DIP switch position at Port C_0, C_1 & C_2 and after each change in baud rate the terminal needs to be reset for this reason. Print of screen display can be obtained by CONTROL-N, i.e. touching 'CRTL' & 'N' together. Printer baud rate is chosen according to switch position at port B0, B1 every time CONTROL-N is touched. In any mode of operation Intelligent mode can be reached by touching 'CRTL' & '0' together. In this mode monitor takes over and displays PLT-AS-RNM-85, CR-LF and a prompt '*'. Now it takes all commands of SDK-85 monitor, provided of course that it is already in the EPROM.

DIP switches, reset switch, printer port which is also a RS232C interface and the main RS232C interface port has been located in the back plate. On-off switch is also located on this plate.

9. Acknowledgements

The microcomputer printed circuit board artwork was done by Shri R.I. Patel for which authors are thankful. The printed circuit board assembly and other hardware work was neatly done by Shri J.K. Dave and Shri H.D. Parikh. An enclosure for any electronics project is an important part. The authors are thankful to Shri M.N. Trivedi of PRL workshop for its fabrication. The authors are also thankful to Shri S.P. Bhatnagar who is at present in Physics Department of South Gujarat University, for providing help in preparation of character generator. Thanks are due to Shri Surendra Pal for his helpful suggestions. It would not have been possible to complete this work but for the encouragement given by Professors Satya Prakash, Vijaykumar and B.H. Subbaraya.

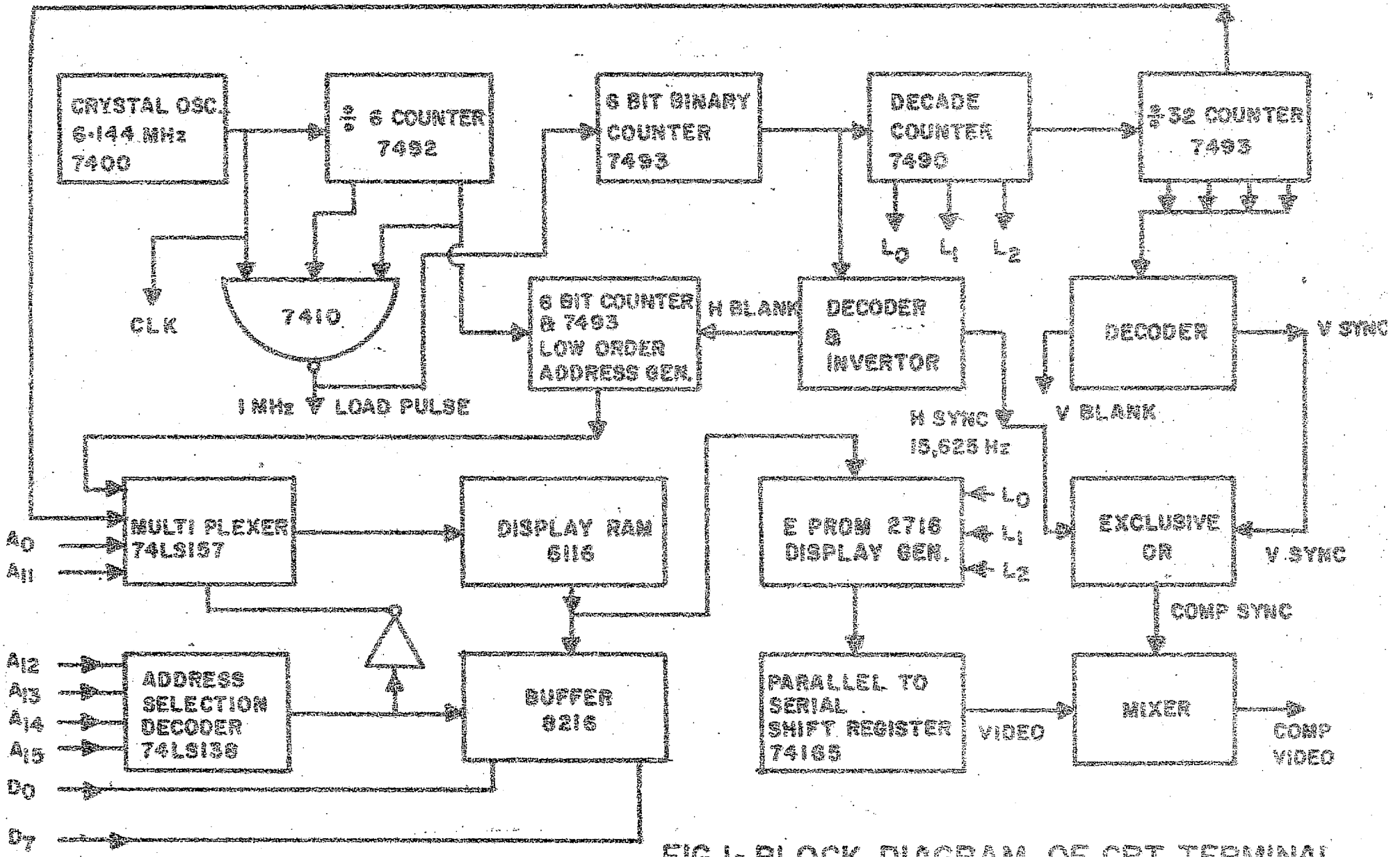


FIG.1: BLOCK DIAGRAM OF CRT TERMINAL

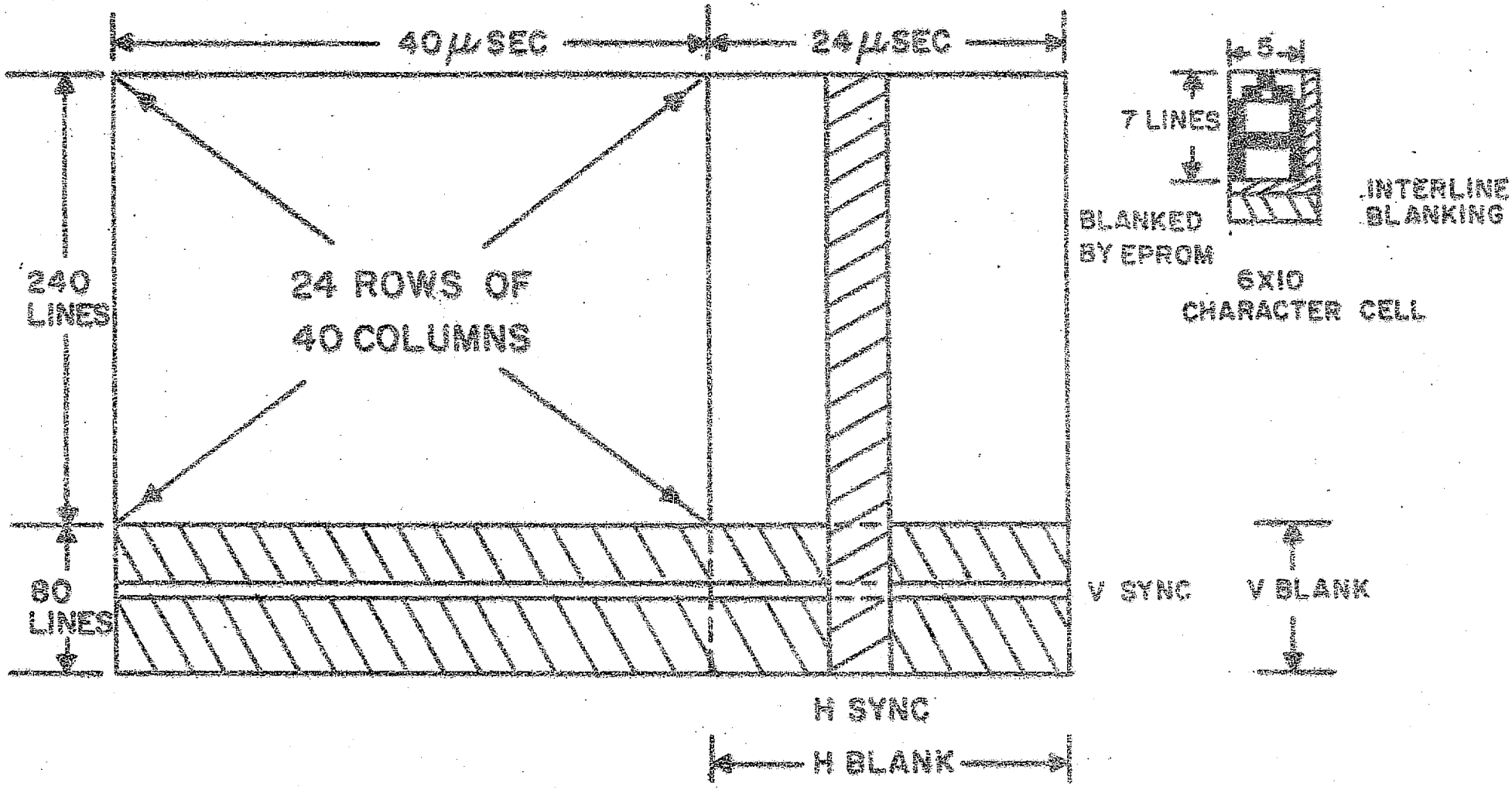


FIG.2. DISPLAY FORMAT

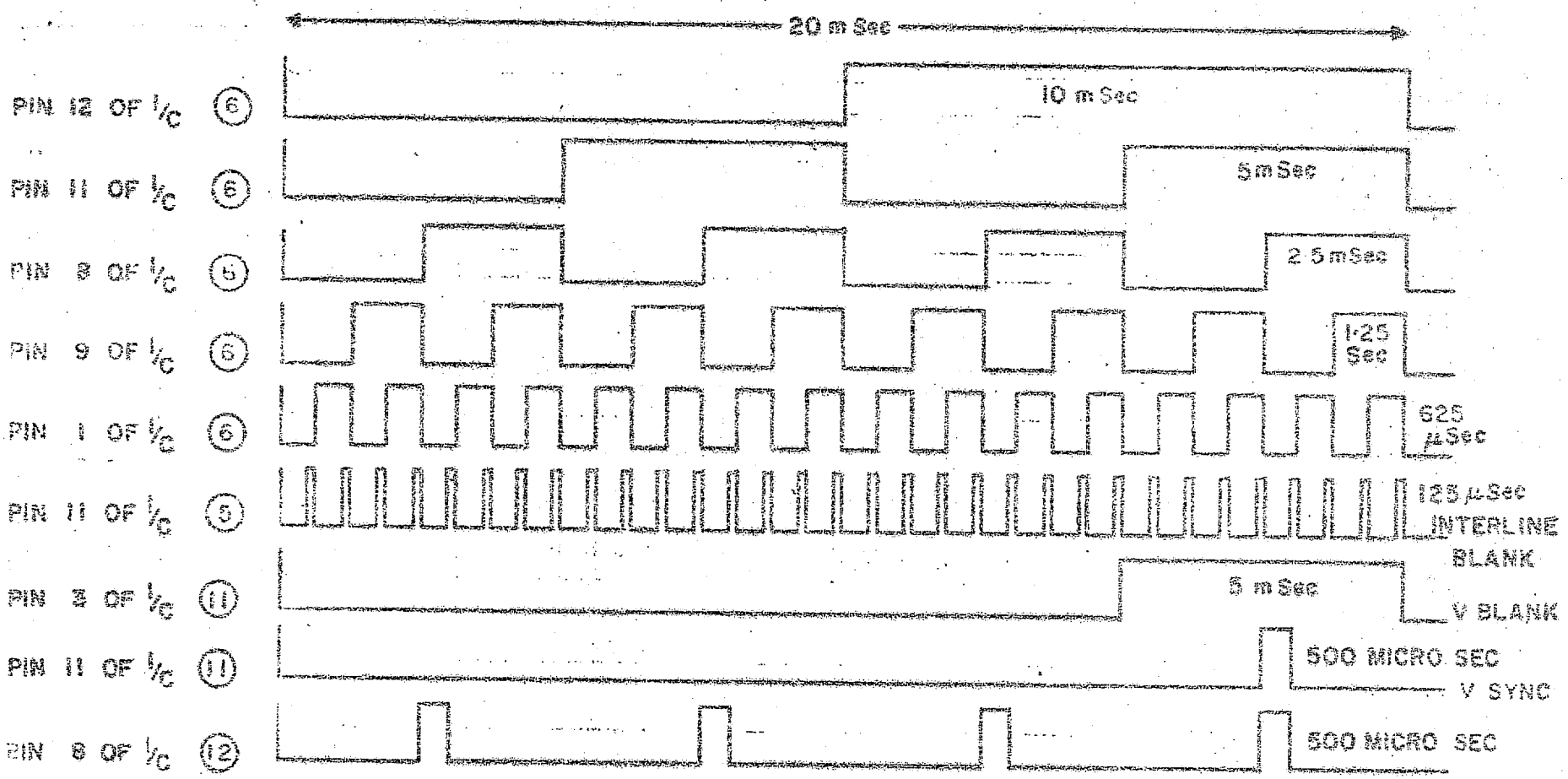


FIG. 3.

WAVE FORMS I (VERTICAL)

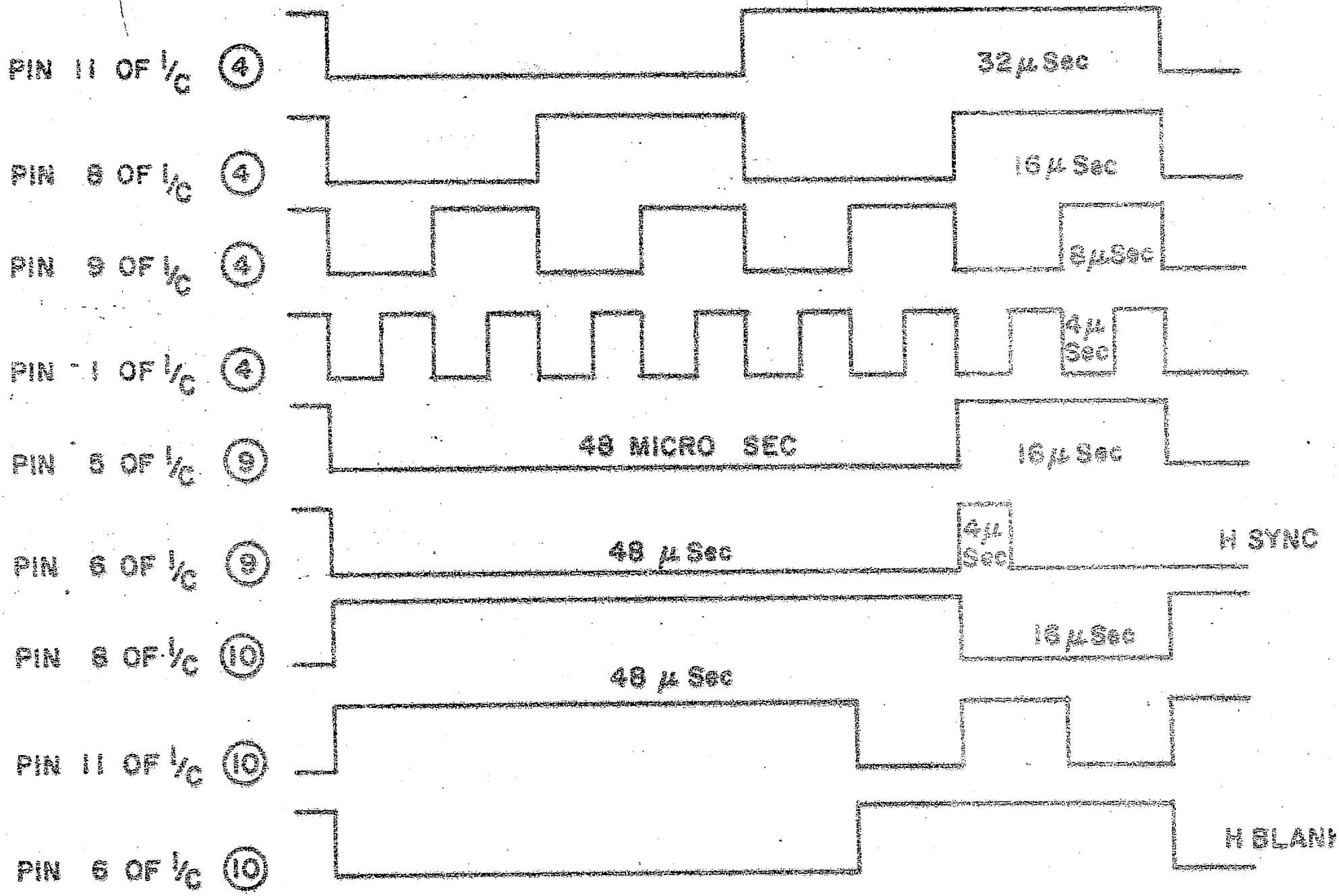


FIG. 4.

WAVE FORMS II (HORIZONTAL)

FIG. 5 SYNC AND ADDRESS GENERATOR

FIG. 6. DISPLAY RAM CHARACTOR GENERATOR AND VIDEO
COMPUTOR BUS INTERFACE.

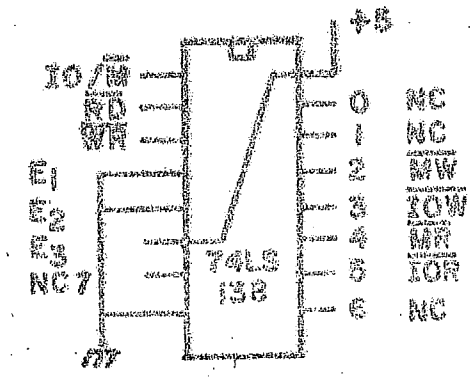
4000-FFFF	NOT DECODED ON BOARD	
3800-3FFF	RAM SOCKET	6116
3000-37FF	RAM SOCKET	6116
2800-2FFF	NOT USED	
2000-27FF	8155	
1800-1FFF	NOT USED	
1000-17FF		
0800-0FFF	PROM SOCKET	2716
0000-07FF	MONITOR	2716

MEMORY MAP

38-38	NOT USED	
30-37		
28-2F		
20-27	8155	
18-1F	NOT USED	
10-17		
08-0F	8253	
00-07	8251	

I/O MAP

FIG. 7 MEMORY AND I/O MAP



A_0	A_1	A_2		
IO/$\overline{M}$	$\overline{RD}$	$\overline{WR}$	INPUTS	OUTPUTS
1	1	0	3	$\overline{IOW}$
0	1	0	2	$\overline{MW}$
1	0	1	5	$\overline{IOR}$
0	0	1	4	$\overline{MR}$

FIG.8: 74LS138 / 8205 AS IO/$\overline{M}$, $\overline{WR}$, $\overline{RD}$ DECODER

8085
X1
X2
RESET OUT
SOD
SID
TRAP
RST 7.5
RST 6.5
RST 5.5
INTR
INTA
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
GND
Vcc
HOLD
HLDA
CLK(OUT)
RESET IN
READY
IO/M
SI
RD
WR
ALE
SO
A15
A14
A13
A12
A11
A10
A9
A8
8155
AD0
AD1
AD2
AD3
AD4
AD5
AD6
AD7
IO/M
RD
WR
ALE
RESET
TIMER IN
PC3
PC4
PC5
TIMER OUT
CE
PC0
PC1
PC2
Vcc
PA0
PA1
PA2
PA3
PA4
PA5
PA6
PA7
PB0
PB1
PB2
PB3
PB4
PB5
PB6
PB7
8212
DS1
MD
DI1
DO1
DI2
DO2
DI3
DO3
DI4
DO4
STB
GND
INT
8253
D7
D6
D5
D4
D3
D2
D1
D0
CLK0
OUT0
GATE0
GND
Vcc
WR
RD
CS
A1
A0
CLK2
OUT2
GATE2
CLK1
GATE1
OUT1
8255
A7
A6
A5
A4
A3
A2
A1
A0
D0
D1
D2
GND
Vcc
A8
A9
WR
RD
CS
A10
RESET
D7
D6
D5
D4
D3
8748
8755

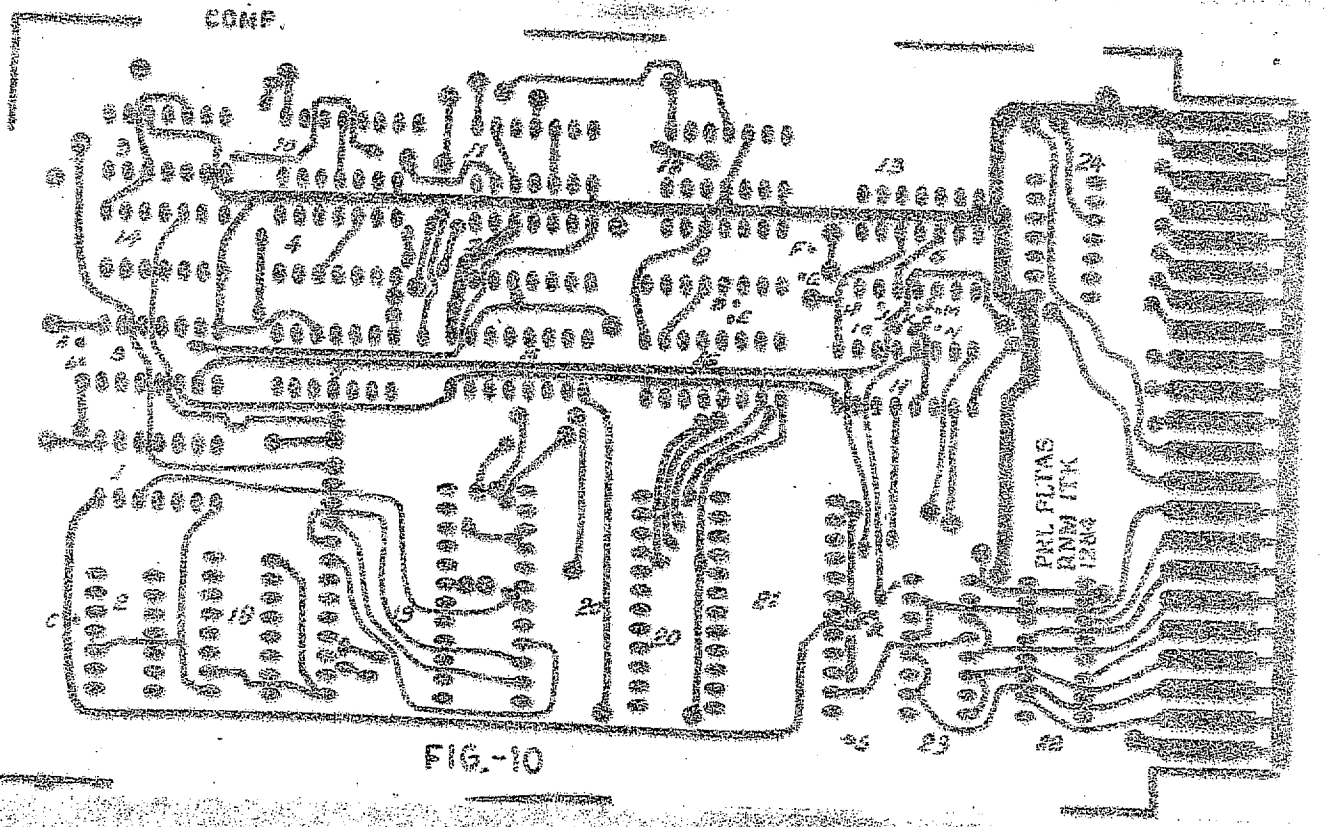


FIG.-10

FIG. 1

FIG - 15

FIG-13

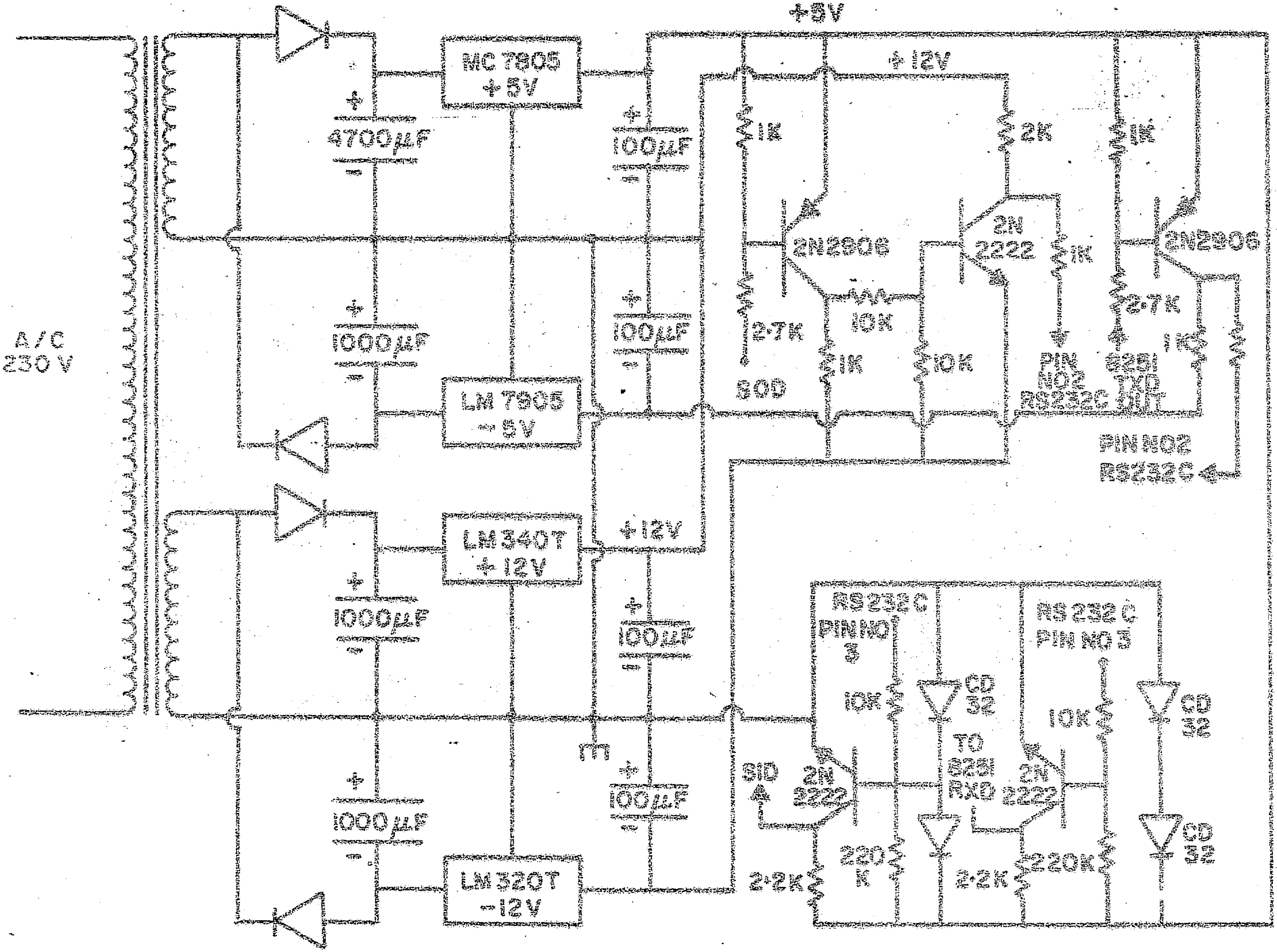


FIG.14 CIRCUIT DIAGRAM OF LOWER SUPPLY

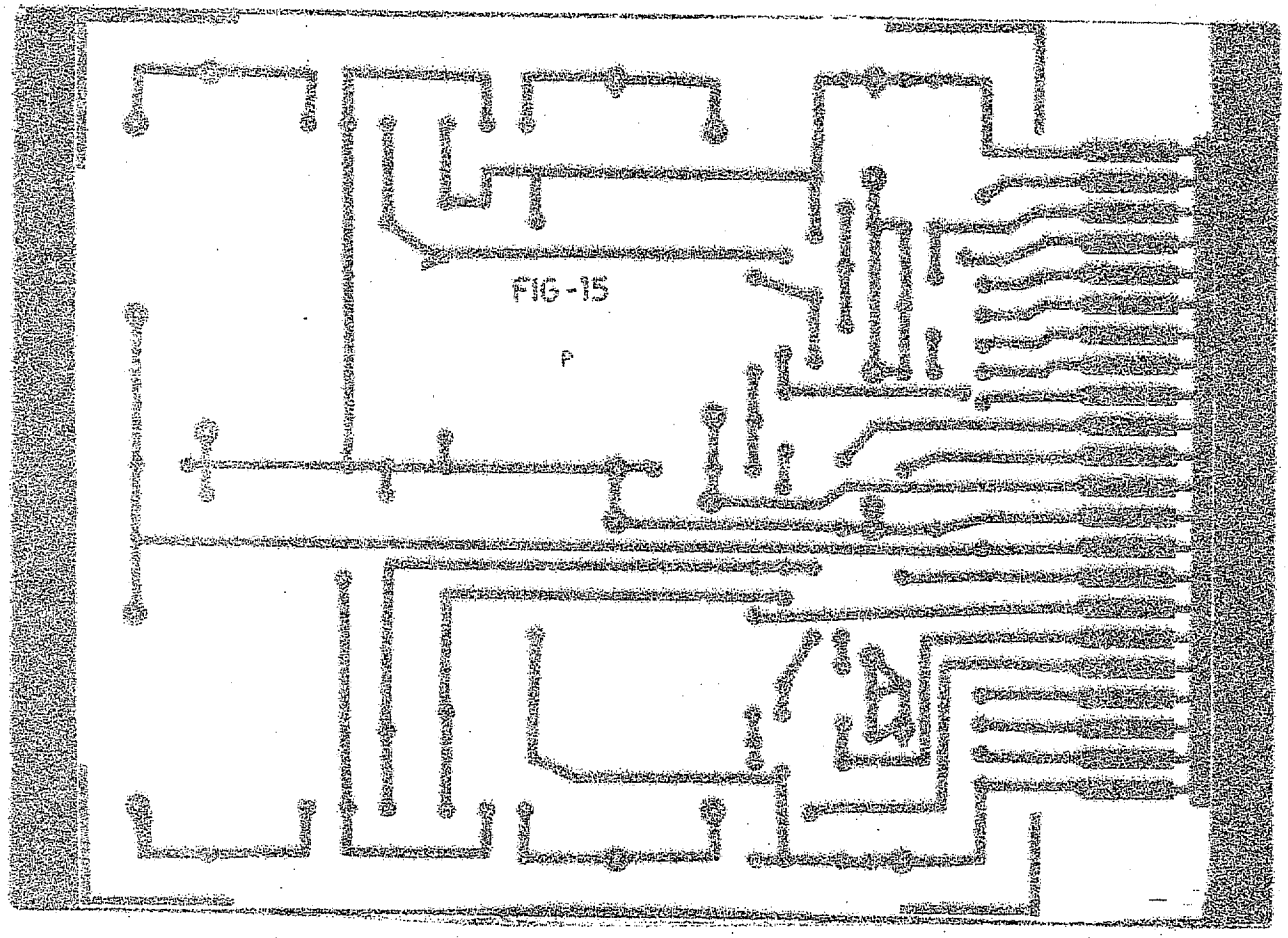


FIG-15

8085 A BASED SINGLE CARD MICROCOMPUTER

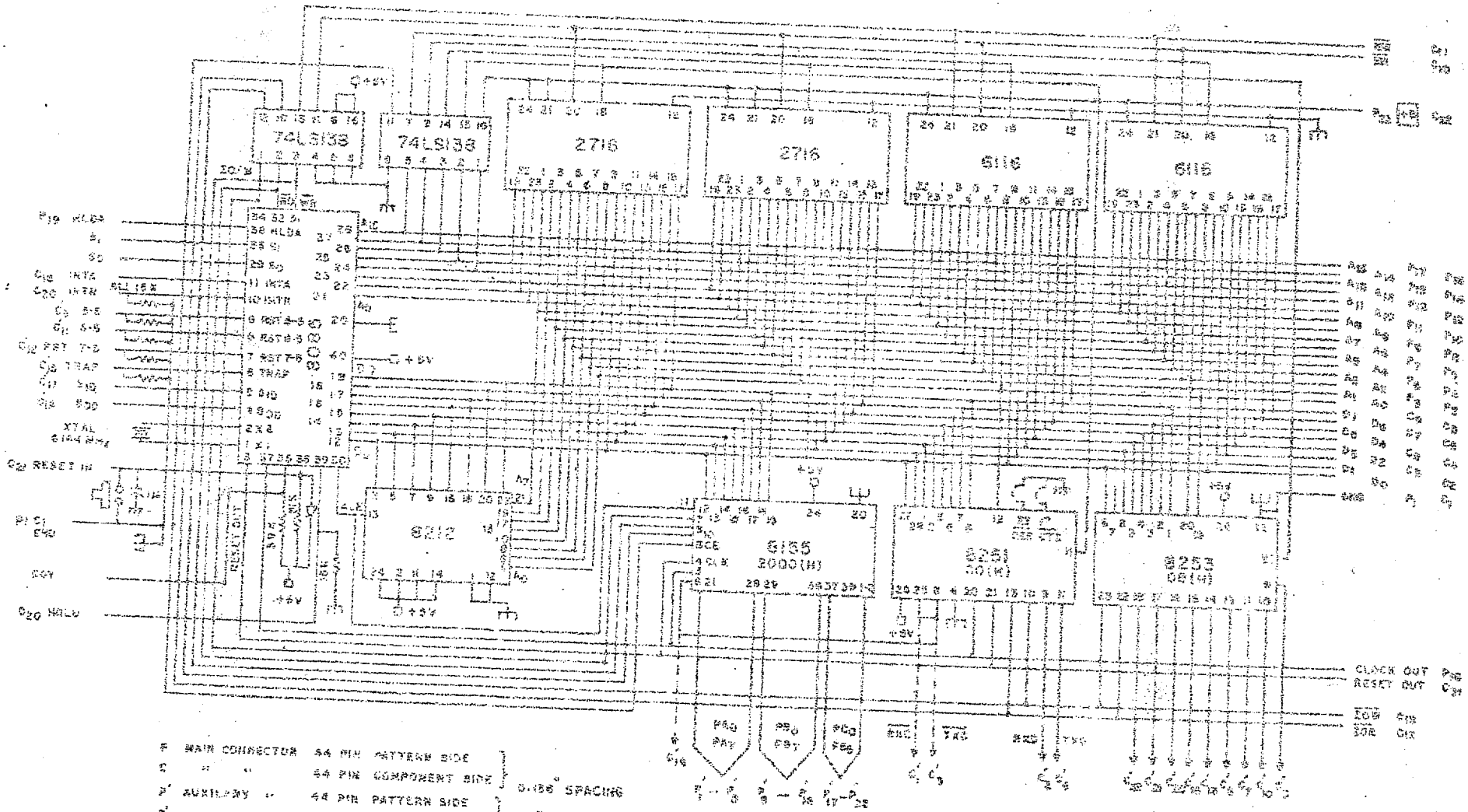


FIG-15

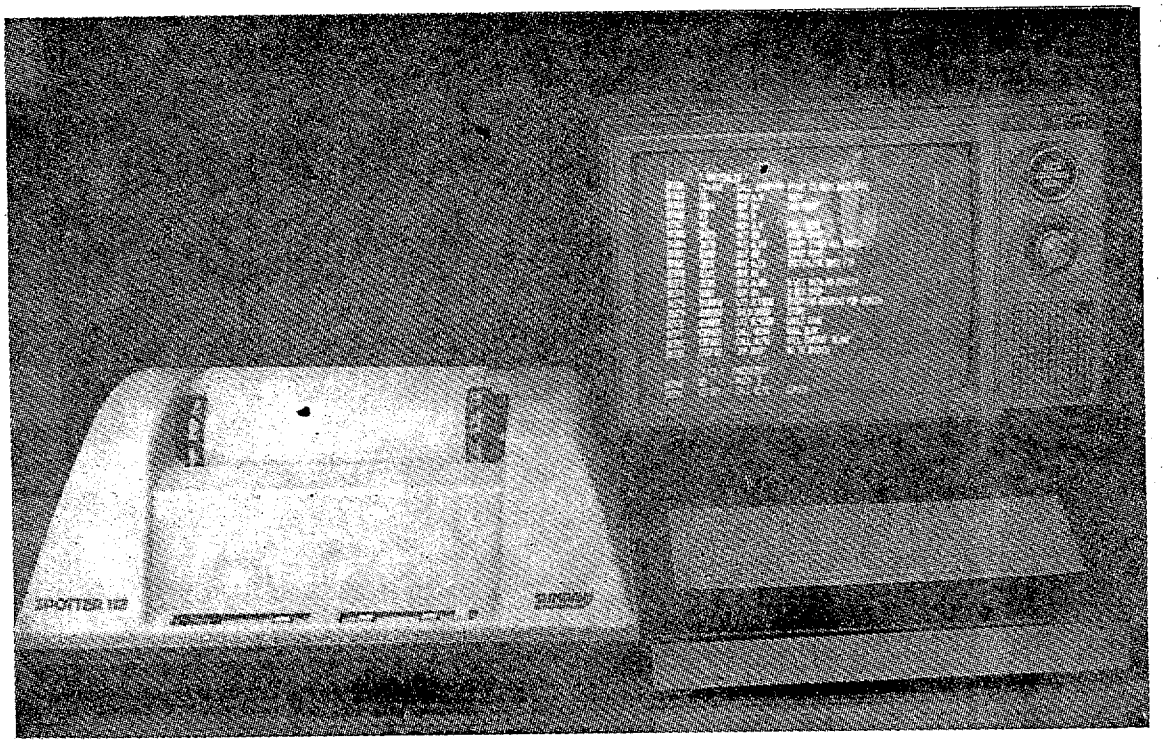


FIG-17

APPENDICES

SOFTWARE CHANGES

S.No.	Location	New Contents (HEX)
1.	0092	1E50
2.	00A7	013000
3.	0138	E65F
4.	013A	FE50
5.	0146	013000
6.	014C	FEFC
7.	0158	2180F0
8.	015B	01800B
9.	016C	2180FB
10.	018E	2180FB
11.	0191	015000
12.	01A3	E680
13.	0180	118000
14.	01E6	1180FF
15.	0380	01000C

APPENDIX B

List of components for Video Display Generator.

		Item		Qty.
1.	7400	2 Input NAND Gate	..	Four
2.	7410	3 Input NAND Gate	..	One
3.	7425	4 Input NOR Gate	..	One
4.	7486	2 Input Exclusive or Gate	..	One
5.	7490	DECADE Counter	..	One
6.	7492	DIVIDE BY TWELVE COUNTER	..	One
7.	7493	4 BIT BINARY COUNTER	..	Five
8.	74 LS138	3 To 8 LINE DECODER/MULTIPLEXER	..	One
9.	74157	QUAD 2 To 1 Line DATA Selector/ Multiplexer	..	Three
10.	74165	Parallel LOAD 8 BIT Shift Register with complementary outputs	..	One
11.	6116	STATIC RAM	..	One/Two
12.	2716	16K EPROM	..	One
13.	8216	Data Bus Bufferes	..	Two
14.	2 N 911	Transisor	..	One
15.	6.144MHZ	Crystal	..	One
16.	560 OHMS	1/4 Watt Resistance	..	Three
17.	1K OHMS	1/4" Watt Resistance	..	Three
18.	4.7K ,,	,, ,, ,,	..	One
19.	10K ,,	,, ,, ,,	..	One
20.	100 Microfared	Capacitor 16 W.V.	..	One

APPENDIX C

PIN CONNECTIONS OF 8085A MAIN BOARD

1	GND (Bottom most)
2	D0
3	D1
4	D2
5	D3
6	D4
7	D5
8	D6
9	D7
10	$\overline{MR}$
11	$\overline{MW}$
12	$\overline{IoR}$
13	$\overline{IoW}$
14	NC
15	NC/18(H) $\overline{CE}$
16	NC
17	NC
18	$\overline{INTA}$
19	NC
20	INTR
21	RESET OUT
22	+5V(Topmost)

COMPONENT SIDE

1	GND
2	A0
3	A1
4	A2
5	A3
6	A4
7	A5
8	A6
9	A7
10	A8
11	A9
12	A10
13	A11
14	A12
15	A13
16	A14
17	A15
18	CLOCK OUT
19	HLDA
20	HOLD
21	RESET (BUTTON)
22	+5V

PATTERN (SOLDER) SIDE

NOTE: CONNECTOR PIN TO PIN SPACING 0.156"

APPENDIX D

Microcomputer Port Connector Details

A 44 pin double sided connector with 0.1" distance between the pin centers has been used for I/O port, Timer and Interrupt lines. Pins on the pattern side of the PCB have been used for I/O port lines (TABLE II). PA0 to PA7 lines are terminated on a 9 pin male 'D' connector. Connections to this connector have been given below:

Table I

Port line	Pins of 'D' Connector
PA7	1
PA6	2
PA5	3
PA4	4
PA3	5
PA2	6
PA1	7
PA0	8
GND	9

This port is interfaced to keyboard.

2. Lines PB0 and PB1 of Port B are used for controlling the BAUD RATE of Printer and small DIP switch has been connected to these lines inside the chasis for this purpose.

PB0	PB1	BAUD RATE SET
0	0	110
1	0	300
0	1	600
1	1	1200

3. PORT C (23) is used for BAUD rate and Mode selection of the terminal:

BAUD RATE SELECTION

C0	C1	C2	C3	Baud Rate
0	0	0	x	110
1	0	0	x	300
0	1	0	x	600
1	1	0	x	1200
0	0	1	x	2400
1	0	1	x	4800
1	1	0	x	9600

MODE SELECTION

C4	C5	MODE
0	0	LOCAL
1	0	LINE
0	1	INTELLIGENT
1	1	DO

TABLE II

MICROCOMPUTER I/O SIGNALS

Component side		Pattern side	
1(top)	CLK 2 (8253)	1 (Top)	PC5
2	OUT 2	2	PC4
3	GATE-2	3	PC3
4	SOD	4	PC2
5	CLK(8085)/TIMER-IN8155	5	PC1
6	SID	6	PC0
		7	PB7
7	CLK 1 (8253)	8	PB6
8	TRAP	9	PB5
9	TIMER OUT (8155)	10	PB4
10	GATE-1 (8253)	11	PB3
11	RST 7.5	12	PB2
12	RST 6.5	13	PB1
13	OUT 0 (8253)	14	PB0
14	RSTS-5	15	PA7
15	OUT 1 (8253)	16	PA6
16	GATE 0	17	PA5
17	CLK 0	18	PA4
18	GND	19	PA3
19	TXD	20	PA2
20	$\overline{\text{TXC}}$	21	PA1
21	RXD		
22 (BOTTOM)	$\overline{\text{RXC}}$	22 (BOTTOM)	PA0

Connector type 225-805-22H (Amphetronix)

APPENDIX E

USE OF 2732 EPROM IN PLACE OF 2716 IN MICROCOMPUTER

1. Cut pattern from X to XX.
2. INSTALL TWO DIODES IN 4148 in place of JUMPERS
   J1 J2
3. JOIN P-P from bottom of the PCB
4. INSTALL DIODE IN 4148 at D3 and D4
5. JOIN XX point to Y point
6. Remove Jumber J3

Now first two sockets can accommodate 2732 in place of 2716. Their locations will be 0000 - OFFFand 1000 - 1FFF.

APPENDIX F

List of components for 8085A based microcomputer

			Qty.
1.	8085A	Single chip 8 Bit N-channel microprocessor	1
2..	8155	2048 BIT Static MOS Ram with I/O PORTS and TIMER.	1
3.	8212	8 Bit INPUT/OUTPUT Port	1
4.	8251A	Programmable communication interface	1
5.	8253	Programmable INTERVAL TIMER	1
6.	2716	16K UV Erasable PROM	2
7.	6116	STATIC CMOS RAM	2
8.	74 LS138	3 to 8 LINE DECODERS/MULTIPLEXERS	2
9.		CRYSTAL 6.144 MHZ	1
10.		DIODE IN 914	1
11.	RESISTANCE 3K 1/4 Watt		1
12.	,, 51K ,, ,,		1
13.	Capacitor 10MFD 10V		2
14.	Capacitor 1 MFD 10V		1
15.	Capacitor 0.1 μF 25 V		3

APPENDIX-G

LIST OF COMPONENTS FOR POWER SUPPLY AND RS 232C INTERFACE

1.	STEP DOWN TRANSFORMER PRIMARY 230 Volts with two Secondaries i. 0-10V @ 2 AMPs ii. 0-20V @ 100 mA	1
2.	Rectifire diodes type 1N 4001	4
3.	Al. Electrolyte 5000 µF 16/25 Volts	1
4.	-do- 1000 µF 16/25 volts	3
5.	-do- 100 µF 16 volts	4
6.	MC 7805 CK Three Terminal Regulator for +5 volts	1
7.	7905 " " " -5 "	1
8.	7815 " " " +15 "	1
9.	7915 " " " -15 "	1
10.	Heat Sinks for MC 7805 CK	1
11.	NPN Transister 2 N 2222	3
12.	PNP " 2 N 2906	2
13.	DIODE " CD 32/22	4
14.	Resistors 1K 1/4 Watt	5
15.	" 2.2K " "	3
16.	" 2.7K " "	1
17.	" 10K " "	4
18.	" 220K " "	2

APPENDIX H

```
0000    31A020      LXI SP,20A0       INTIALIZE STACK POINTER
0003    C36003      JMP 0360          JUMP TO REMAINING PART OF
0008    22EF20      SHLD 20EF         INIT. ROUTINE, SAVE H,L
000B    E1          POP H             GATE USER PC
000C    22F220      SHLD 20F2         SAVE
000F    F3          PUSH PSW
0010    E5          POP H
0011    22ED20      SHLD 20ED         SAVE FF'S & A
0014    210000      LXI H,0000        CLEAR H,L
0017    39          DAD SP            GATE STACK POINTER
0018    22F420      SHLD 20F4         SAVE SP
001B    21ED20      LXI H,20ED        SET SP TO SAVE BC & DE
001E    F9          SPHL
001F    C5          PUSH B            SAVE BC
0020    D5          PUSH D            SAVE DE
0021    C3FA03      JMP 03FA          JUMP TO START OF TTY MONITOR
0024    C3AE20      JMP 20AE          TRAP
0028    C3C220      JMP20C2           RST   5.0
002C    C3B520      JMP 20B5          RST   5.5
0030    C3C520      JMP 20C5          RST   6.0
0034    C3C820      JMP 20C8          RST   6.5
0038    C3CB20      JMP 20CB          RST   7.0
003C    C3CE20      JMP 20CE          RST   7.5

        'BRANCH'

003F    DB23        IN 23             TEST PORT C LINES C4 & C5
0041    E620        ANI 20            AND JUMP TO
0043    C20800      JNZ 0008          MONITOR IF EITHER IS 1
0046    DB23        IN 23
0048    E610        ANI 10
004A    C25000      JNZ 0050          LINE MODE IF C4 IS 1
004D    C3B400      JMP 00B4          ELSE LOCAL MODE

        'LINE MODE'

 0050   DB01        IN 01             STATUS FLAG OF 8251
 0052   E602        ANI 02            IF NO CHARACTER
0054    CA6C00      JZ 006C           JUMP TO KEY BOARD
0057    DB00        IN 00
0059    4F          MOV C,A           ELSE
005A    CDC405      CALL 05C4         DISPLAY THE CHARACTER TO SCREEN
005D    C36C00      JMP 006C          THEN JUMP TO KEY BOARD

        'CO' CHARACTER OUT

0060    F5          PUSH PSW          SAVE STATUS
0061    DB01        IN 01             FLAG FOR INPUT 8251
0063    E604        ANI 04
0065    CA6100      JZ 0061           WAIT IF BUFFER FULL
0068    F1          POP PSW           ELSE
0069    D300        OUT 00            TRANSMIT CHARACTER
006B    C9          RET
```

'KEY BOARD'

006C	CD7201	CALL 0172	BLANK CURSOR
006F	CDE105	CALL 05E1	IS THERE CHARACTER AT KEY BOARD
0072	DA5000	JC 0050	IF NONE LOOP BACK TO LINE MODE
0075	110010	LXI D,1000	ELSE
0078	CDF105	CALL 05F1	DELAY
007B	CDE105	CALL 05E1	READ KEY BOARD AGAIN
007E	DA5000	JC 0050	IF NO CHARACTER LOOP BACK
0081	CD6000	CALL 0060	IF YES TRANSMIT IT
0084	C35000	JMP 0050	JUMP TO LINE MODE AGAIN

'PRINT'

0087	E5	PUSH H	SAVE REGISTER
0088	D5	PUSH D	
0089	C5	PUSH B	
008A	CDEE00	CALL 00EE	SET 'PRINT BAUD'
008D	2100F0	LXI H,F000	POINT TO SCREEN BEGINNING
0090	1618	MVI D,18	NO OF LINES 24
0092	1E50	MVI E,50	NO OF CHARACTER PER LINE 80
0094	0E0A	MVI C,0A	'CR'
0096	CDC700	CALL 00C7	PRINT OUT
0099	0E0D	MVI C,0D	'LF'
009B	CDC700	CALL 00C7	PRINT OUT
009E	4E	MOV C,M	SCREEN CHARACTER
009F	CDC700	CALL 00C7	PRINT OUT
00A2	23	INX H	NEXT CHARACTER
00A3	1D	DCR E	FULL LINE OVER ?
00A4	C29E00	JNZ 009E	IF NO PRINT NEXT CHARACTER
00A7	003000	LXI B,0030	POINT TO NEXT LINE
00AA	09	DAD B	
00AB	15	DCR D	24 LINES OVER ?
00AC	C29200	JNZ 0092	IF NO GO TO NEXT LINE
00AF	C1	POP B	ELSE JOB IS DONE
00B0	D1	POP D	
00B1	E1	POP H	
00B2	C9	RET	

'LOCAL'

00B4	CD9005	CALL 0590	GET CHARACTER FROM KEY BOARD
00B7	4F	MOV C,A	
00B8	CDC405	CALL 05C4	DISPLAY IT
00BB	C3B400	JMP 00B4	REPEAT THE PROCESS

'DATA FOR PRINTER BAUD RATE'

00BE	2301	INX.H	110	BAUD RATE
00C0	6D00	LXI B,006D	300	BAUD RATE
00C2	3600	MVI M,00	600	BAUD RATE
00C4	1900	DAD D	1200	BAUD RATE

```
                ' PRINT OUT '

00C7    F3          DI          DISABLE INTERRUPTS
00C8    C5          PUSH B      SAVE
00C9    D5          PUSH D
00CA    3EC0        MVI A,C0    START BITS MASK
00CC    0607        MVI B,07    NO OF BITS
00CE    30          SIM         TRANSMIT THRU SOD
00CF    110202      LXI D.0202  LOAD D FOR BIT TIME DELAY
00D2    CDEA07      CALL 07EA   CALL BIT TIME
00D5    79          MOV A,C     TAKE BITS
00D6    1F          RAR         GATE LSB
00D7    4F          MOV C,A     PUT BACK
00D8    3E80        MVI A,80    SHIFTED ENABLE BIT
00DA    1F          RAR         SHIFT IN DATA FROM CARRY BIT
00DB    EE80        XRI 80      INVERT IT
00DD    05          DCR B       COUNT BITS
00DE    F2CE00      JP 00CE     IF MORE BITS REPEAT
00E1    3E40        MVI A,40    ELSE SEND STOP BITS
00E3    30          SIM
00E4    110403      LXI D,0304  WAIT FOR FAKE PARITY
00E7    CDEA07      CALL 07EA   + 3 BITS
00EA    D1          POP D

00EB    C1          POP B
00EC    FB          EI
00ED    C9          RET

                ' PRINT BAUD '

00EE    DB22        IN 22       B0, B1 LINES
00F0    E603        ANI 03
00F2    87          ADD A       ADD DATA
00F3    21BE00      LXI H,00BE  POINT TO DATA FOR PRINTER BAUD
00F6    85          ADD L
00F7    6F          MOV L,A     GENERATE DATA IN H,L
00F8    7E          MOV A,M
00F9    23          INX H
00FA    66          MOV H,M
00FB    6F          MOV L,A
00FC    22B120      SHLD 20B1   STORE AT 20B1
00FF    C9          RET

               'DISPLAY TEST'

0100    FE20        CPI 20      IS DATA PRINTABLE (ABOVE 20H )
0102    D23001      JNC 0130    IF YES DISPLAY, ELSE BRANCH
0105    FE0D        CPI 0D      CR
0107    CA9F01      JZ 019F
010A    FE0A        CPI 0A      LF      !
010C    CAAA01      JZ 01AA
010F    FE09        CPI 09      TAB
0111    CABB01      JZ 01BB
0114    FE08        CPI 08      BACK SPACE <----
```

```
0116    CAF101      JZ 01F1
0119    FE0B        CPI 0B          UP
011B    CAE001      JZ 01E0
011E    FE0C        CPI 0C          RIGHT
0120    CAD601      JZ 01D6
0123    FE1E        CPI 1E          HOME
0125    CACD01      JZ 01CD
0128    FE1B        CPI 1B          ESC
012A    CAFB01      JZ 01FB
012D    C9          RET

        'DISPLAY'

0130    F5          PUSH PSW
0131    E5          PUSH H
0132    2AB820      LHLD 20B8       CURSOR ADDRESS
0135    77          MOV M,A         DISPLAY CHARACTER
0136    23          INX H           NEXT
0137    7D          MOV A,L
0138    E65F        ANI 5F
013A    FE50        CPI 50          ARE 80 CHARACTERS OVER
013C    C44501      CZ 0145         GO NEXT LINE
013F    22B820      SHLD20B8        STORE NEW ADDRESS
0142    E1          POP H
0143    F1          POP PSW
0144    C9          RET

        'NEXT LINE'

0145    C5          PUSH B
0146    013000      LXI B,0030      ADD 48 TO ADDRESS
0149    09          DAD B           POINTER
014A    C1          POP B
014B    7C          MOV A,H
014C    FEFC        CPI FC          WAS IT 24TH LINE
014E    CC5201      CZ 0152         IF SO CALL 'SCROLL'
0151    C9          RET

        'SCROL'

0152    C5          PUSH B
0153    D5          PUSH D
0154    E5          PUSH H
0155    1100F0      LXI D,F000      FIRST LINE
0158    2180F0      LXI H,F080      SECOND LINE
015B    01800B      LXI B,0B80      LAST LINE DISPLACEMENT
015E    7E          MOV A,M         COPY SECOND LINE
015F    12          STAX D          TO FIRST LINE
0160    13          INX D
0161    23          INX H           CONTINUE TILL 24TH LINE
0162    0B          DCX B
0163    78          MOV A,B
0164    B1          ORA C
0165    C25E01      JNZ 015E        CONTINUE COPYING IF NOT OVER
0168    CD8E01      CALL 018E       BLANK 24TH LINE
```

```
016B   E1          POP H
016C   2180FB      LXI H,FB80    POINT TO 24TH LINE
016F   D1          POP D
0170   C1          POP B
0171   C9          RET

       'CURSOR'

0172   F5          PUSH PSW      SAVE
0173   E5          PUSH H
0174   D5          PUSH D
0175   2AB820      LHLD 20B8     CURSOR ADDRESS
0178   7E          MOV A,M       SAVE CHARACTER
0179   F5          PUSH PSW
017A   365F        MVI M,5F
017C   11FF3F      LXI D,3FFF    DISPLAY UNDER LINE
017F   CDF105      CALL 05F1     WAIT
0182   F1          POP PSW       GET BACK OLD CHARACTER
0183   77          MOV M,A       DISPLAY
0184   11FF3F      LXI D,3FFF
0187   CDF105      CALL 05F1     WAIT
018A   D1          POP D
018B   E1          POP H         RESTORE
018C   F1          POP PSW
018D   C9          RET

       'BLANK'

018E   2180FB      LXI H,FB80    LAST LINE
0191   015000      LXI B,0050    80 CHARACTERS
0194   3E20        MVI A,20      BLANK (SPACE )
0196   77          MOV M,A
0197   23          INX H         BLANK WHOLE LINE
0198   0B          DCX B
0199   78          MOV A,B
019A   B1          ORA C
019B   C29401      JNZ 0194      ALL CHARACTERS OVER ?
019E   C9          RET           IF YES ALL DONE

       ' CR '

019F   F5          PUSH PSW
01A0   3AB820      LDA 20B8      CURSOR ADDRESS
01A3   E680        ANI 80        GO LEFT END
01A5   32B820      STA 20B8      STORE NEW ADDRESS
01A8   F1          POP PSW
01A9   C9          RET
```

```
        ' LF '

01AA    F5          PUSH PSW
01AB    E5          PUSH H
01AC    D5          PUSH D
01AD    2A8820      LHLD 2088       CURSOR ADDRESS
01B0    118000      LXI D,0080      ADD 126
01B3    19          DAD  D
01B4    CD4B01      CALL 014B       TEST IF LAST LINE (LL)
01B7    C3EA01      JMP 01EA        'STORE AND RETURN'

        ' TAB '

01B8    E5          PUSH H
01BC    2A8820      LHLD 2088       CURSOR ADDRESS
01BF    7D          MOV A,L
01C0    C608        ADI 08          INCREMENT BY 8
01C2    E6F8        ANI F8          3 LOW BITS '0'
01C4    6F          MOV L,A
01C5    228820      SHLD 2088       STORE NEW ADDRESS
01C8    E1          POP H
01C9    C9          RET

        ' HOME '

01CD    E5          PUSH H
01CE    2100F0      LXI H,F000      CURSOR ADDRESS
01D1    228820      SHLD 2088       LEFT UPPER CORNER
01D4    E1          POP H
01D5    C9          RET

        ' RIGHT '

01D6    E5          PUSH H
01D7    2A8820      LHLD 2088       CURSOR ADDRESS
01DA    23          INX H           INCREMENT BY ONE AND
01DB    228820      SHLD 2088       STORE
01DE    E1          POP H
01DF    C9          RET

        ' Up '

01E0    F5          PUSH PSW
01E1    E5          PUSH H
01E2    D5          PUSH D
01E3    2A8820      LHLD 2088       CURSOR ADDRESS
01E6    1180FF      LXI D,FF80      SUBTRACT 80 IN 2'S COMPEMENT
01E9    19          DAD D           AND
01EA    228820      SHLD 2088       STORE
01ED    D1          POP D
01EE    E1          POP H
01EF    F1          POP PSW
01F0    C9          RET
```

```
                ' LEFT '

01F1    E5          PUSH H
01F2    2AB820      LHLD 20B8       CURSOR ADDRESS
01F5    2B          DCX H           DECREMENT
01F6    22B820      SHLD 20B8       AND STORE.
01F9    E1          POP H
01FA    C9          RET

                ' ESC '

01FB    0E24        MVI C,24        ' $ '
01FD    C3C405      JMP 05C4        DISPLAY IT

               'MAIN BAUD '

0344    DB23        IN 23           C0, C1, C2 POSITION
0346    E607        ANI 07
0348    215003      LXI H,0350      POINT TO 'MAIN BAUD TABLE'
034B    87          ADD A
034C    85          ADD L           POINT TO DESIRED BAUD RATE
034D    6F          MOV L,A         DATA
034E    C9          RET

                ' MAIN BAUD TABLE '

0350    1440        9600        BAUD
0352    2840        4800        BAUD
0354    5040        2400        BAUD
0356    A040        1200        BAUD
0358    4041        600         BAUD
035A    8042        300         BAUD
035C    D146        110         BAUD

                ' INITIALS '

0360    CD4403      CALL 0344       POINT TO MAIN BAUD RATE
0363    7E          MOV A,M         DATA
0364    D324        OUT 24          LOW COUNT
0366    23          INX H
0367    7E          MOV A,M         FOR 8155
0368    D325        OUT 25          HIGH COUNT
036A    3EF0        MVI A,F0        START TIMER ALL PORTS
036C    D320        OUT 20          INPUT PORT
036E    3ECE        MVI A,CE        INITIALISE 8251 FOR
0370    D301        OUT 01
0372    3E05        MVI, A, 05      8 BIT DATA NO PARITY
0374    D301        OUT 01          2 BIT STOP
0376    2100F0      LXI H,F000      STARTING ADDRESS FOR SCREEN
0379    22B820      SHLD 20B8       STORE
037C    01000C      LXI B,0C00      WHOLE PAGE
037F    CD9401      CALL 0194       CALL BLANK
0382    CD7201      CALL 0172       CALL CURSOR BLANK
0385    C33F00      JMP 003F        GO TO BRANCH
```

```
        ' CI '

0590        D5          PUSH D
0591        CD7201      CALL 0172       CURSOR ADDRESS
0594        CDE105      CALL 05E1       CHECK KEY BOARD
0597        DA9105      JC 0591         NO CHARACTER CHECK AGAIN
059A        110010      LXI D,1000      DELAY KEY DEBOUNCE
059D        CDF105      CALL 05F1
05A0        CDE105      CALL 05E1       CHECK KEY BOARD
05A3        DA9105      JC 0591         NO CHARACTER CHECK AGAIN
05A6        D1          POP D           ELSE DONE
05A7        C9          RET

        ' TEST KEY '

05A8        F5          PUSH PSW
05A9        F5          PUSH PSW
05AA        FE0E        CPI 0E
05AC        CC8700      CZ 0087
05AF        F1          POP PSW
05B0        FE0F        CPI 0F
05B2        CAFA03      JZ 03FA
05B5        F1          POP PSW
05B6        C9          RET

        ' CO '

05C4        79          MOV A,C         DISPLAY CHARACTER IN C
05C5        E67F        ANI 7F          CHARACTER IN A
05C7        CD0001      CALL 0100       GO AND DISPLAY
05CA        C9          RET

        ' KEY BOARD '

05E1        DB21        IN 21           READ KEY BOARD PORT
05E3        07          RLC             TEST BIT 7, SHIFT IT
05E4        D8          RC
05E5        0F          RRC             IN CARRY & RESTORE BYTE
05E6        CDA805      CALL 05A8       CALL 'TEST KEY'
05E9        C9          RET
```

APPENDIX I

HEXDUMP OF CHARACTER GENERATOR

```
DD3000 32FF

3000 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3010 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3020 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3030 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3040 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3050 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3060 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3070 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3080 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3090 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
30A0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
30B0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
30C0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
30D0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
30E0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
30F0 FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3100 00 00 00 00 00 00 00 00 08 08 08 08 00 00 08 00
3110 14 14 00 00 00 00 00 00 14 14 FF 14 FF 14 14 00
3120 08 3E 0C 12 2A 1C 08 00 00 24 10 08 04 42 00 00
3130 08 14 14 0C 2A 12 2C 00 0C 08 08 08 00 00 00 00
3140 10 08 04 04 04 08 10 00 04 08 10 10 10 08 04 00
3150 08 2A 1C 08 1C 2A 08 00 00 08 08 3E 08 08 00 00
3160 00 00 00 00 00 08 08 04 00 00 00 3C 00 00 08 00
3170 00 00 00 00 00 0C 0C 00 00 20 10 08 FF FF 00 FF
3180 1C 22 32 2A 26 32 1C 00 08 0C 08 08 08 08 1C 00
3190 1C 22 20 1C 02 02 3E 00 3E 20 10 18 20 22 1C 00
31A0 10 18 14 12 3E 10 10 00 3E 02 1E 20 20 22 1C 00
31B0 38 04 02 1E 22 22 1C 00 3E 20 10 08 04 04 04 00
31C0 1C 22 22 1C 22 22 1C 00 1C 22 22 3C 20 10 0E 00
31D0 00 00 08 00 00 08 00 00 00 00 08 00 00 08 08 04
31E0 10 08 04 02 04 08 10 00 00 00 3E 00 3E 00 00 00
31F0 04 08 10 20 10 08 04 00 1C 22 20 10 08 00 08 00
3200 1C 22 3A 2A 3A 02 1C 00 08 14 22 22 3E 22 22 00
3210 1E 24 24 1C 24 24 1E 00 1C 22 02 02 02 22 1C 00
3220 1E 24 24 24 24 24 1E 00 3E 02 02 0E 02 02 3E 00
3230 3E 02 02 0E 02 02 02 00 30 02 02 3A 22 22 3C 00
3240 22 22 22 3E 22 22 22 00 1C 08 08 08 08 08 1C 00
3250 70 20 20 20 20 22 1C 00 22 12 0A 06 0A 12 22 00
3260 02 02 02 02 02 02 3E 00 22 36 2A 2A 22 22 22 00
3270 22 26 2A 32 22 22 22 00 1C 22 22 22 FF 22 20 00
3280 1E 22 22 1E 02 02 02 00 1C 22 22 22 2A 12 2C 00
3290 1E 22 22 1E 0A 12 22 00 3C 02 02 1C 20 20 1E 00
32A0 3E 08 08 08 08 08 08 00 22 22 22 22 22 22 1C 00
32B0 22 22 22 22 22 14 08 00 22 22 22 22 2A 36 22 00
32C0 22 22 14 08 14 22 22 00 22 22 22 14 08 08 08 00
32D0 3E 20 10 08 04 02 3E 00 1C 04 04 04 04 04 1C 00
32E0 00 02 04 08 10 20 00 00 38 20 20 20 20 20 38 00
32F0 08 14 22 00 00 00 00 00 00 00 00 00 00 00 00 FF
```

D3300 33FF

```
3300  04 08 10 00 00 00 00 00 00 00 00 3C 20 3C 22 3C 00
3310  02 02 1A 26 22 22 1E 00 00 00 3E 04 04 04 38 00 00
3320  20 20 2C 32 22 22 3C 00 00 00 38 24 BC 04 38 00 00
3330  38 24 04 02 04 04 04 00 00 00 BC 22 22 3C 20 3C 00
3340  02 02 1A 26 22 22 22 00 08 00 05 08 08 08 90 00 00
3350  20 00 20 20 20 04 24 18 02 02 22 12 04 14 22 00 00
3360  98 08 08 08 08 08 90 00 00 00 34 2A 2A 22 22 00 00
3370  00 00 1A 26 22 22 22 00 00 00 18 24 24 24 18 00 00
3380  00 00 1E 22 22 1E 02 02 00 00 1C 22 22 3C 20 20 00
3390  00 00 1A 26 02 02 02 00 00 00 38 04 18 20 1C 00 00
33A0  08 08 18 08 08 08 90 00 00 00 22 22 22 32 4C 00 00
33B0  00 00 22 32 22 14 08 00 00 00 22 22 2A 3E 14 00 00
33C0  00 00 22 14 08 14 22 00 00 00 22 22 22 3C 20 38 00
33D0  00 00 3E 10 08 04 3E 00 00 30 08 08 04 08 08 30 00
33E0  08 08 08 00 08 08 08 00 06 08 08 10 00 02 06 00 00
33F0  00 00 00 2C 1A 00 00 00 FF FF FF FF FF FF FF FF FF
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HEXDUMP OF KEYBOARD ENCODER

D
D3000 31FF

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3000  1B 31 32 33 34 35 36 37 FF FF 71 77 65 72 74 79
3010  FF FF 61 73 64 66 67 68 00 00 20 7A 78 63 76 62 42
3020  38 29 30 3A 3F 40 5E 5C 73 69 6F 70 70 0A 0D FF
3030  8A 48 4C 3B 58 7F 1B 07 6E 6D 2C 2E 2F 08 0A 1E
3040  1B 21 22 23 24 25 26 27 FF FF 51 57 45 52 54 59
3050  FF FF 41 53 44 46 47 48 0C 08 20 5A 58 43 56 42
3060  28 29 2D 24 3D 60 7E 7C 58 49 4F 50 5D 0A 0B FF
3070  4A 49 4C 2B 5D 7F 1B 07 4E 4D 3C 3E FF 08 0A 1E
3080  1B 31 32 33 34 35 36 37 FF FF 51 57 45 52 54 59
3090  BF FF 41 53 44 46 47 48 0C 08 20 5A 58 43 56 42
30A0  38 39 30 3A 3F 00 5E 5C 15 49 4F 50 5D 0A 0B FF
30B0  4A 49 4C 3B 58 7F 1B 07 4E 4D 2C 2E 2F 08 0A 1E
30C0  1B 21 22 23 24 25 26 27 FF FF 51 57 45 52 54 59
30D0  FF FF 41 53 44 46 47 48 0C 08 20 5A 58 43 56 42
30E0  28 29 2D 24 3D 60 7E 7C 58 49 4F 50 5D 0A 0B FF
30F0  4A 49 4C 2B 5D 7F 1B 07 4E 4D 3C 3E 3F 08 0A 1E
3100  FF FF FF FF FF FF FF FF FF FF FF 11 17 05 12 14 19
3110  FF FF 01 13 04 06 07 08 FF FF FF 1A 18 03 16 02
3120  FF FF FF FF 1F 00 1E 1C 15 09 0F 10 10 FF FF FF
3130  04 08 0C FF FF 18 FF FF FF 08 0D FF FF FF FF FF
3140  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3150  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3160  BF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
3170  BF FF FF BF FF FF FF FF FF FF FF BF 11 17 05 12 14 19
3180  FF FF FF FF 13 04 06 07 08 FF FF FF 1A 18 03 16 02
3190  0A 08 0C FF 1F 00 FF 1E 1C 15 09 0F 10 10 FF FF FF
31A0  FF FF FF FF FF 18 FF FF FF 08 0D FF FF FF FF FF FF
31B0  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
31C0  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
31D0  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
31E0  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
31F0  FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF FF
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(BIT TIME)

THIS SUBROUTINE IS CALLED BY 'PRINT OUT'. IT TAKES TWO BYTE DELAY. DATA FROM LOCATIONS 20B1 & 20B2 LOADS IN H,L. IT ALSO TAKES A MULTIPLIUS N FROM E REGISTER. CONTENTS OF H, L ARE ADDED N + 1 TIMES AND TRANSFERRED TO D E. NOW IT CALLS 'DELAY' TO PROVIDE TIME DELAY.

```
07EA    E5       PUSH H
07EB    2AB120   LHLD 20B1     DELAY DATA IN H, L
07EE    29       DAD H         DOUBLE IT
07EF    1D       DCRE
07F0    C2EE07   JNZ 07EE     ADD N + 1 TIMES
07F3    EB       XCHG          H, L TO D, E
07F4    E1       POP H         RESTORE H
07F5    CDF105   CALL 05F1     DELAY
07F8    C9       RET
```

CONTENTS OFF 20B1 & 20B2 FOR VARIOUS BIT RATES

2301	FOR	110	BAUD
6D00	FOR	300	BAUD
3600	FOR	600	BAUD
1900	FOR	1200	BAUD
0B00	FOR	2400	BAUD