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A CMOS MICROCOMPUTER BASED ON CDP-1802

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DOCUMENT CONTROL AND DATA SHEET

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9.A.Purpose	:	Design details of CMOS micro-computer card based on CDP-1802.
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10. Originating Unit/ Divion and Address	:	Planetary & Atmospheric Sciences Area, Physical Research Laboratory, Navarangpura, Ahmedabad-380009.
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12. Abstract	:	Design and fabrication details of a small micro-computer card based on CDP-1802 micro-processor have been described. It is of 6" x 4" size and has facilities for serial I/O (20mA loop), 20 programmable I/O lines, Interrupt, DMA and 3 control inputs. Microprocessor Bus & control signals are made available on 44 pin edge connector, 2K ROM, 1K RAM is available on board.
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A CMOS MICROCOMPUTER BASED ON CDP-1802

Introduction

CMOS devices have become popular due to their low power consumption and noise immunity. CDP-1802 is a 8 bit microprocessor developed by RCA in 1975 and is first of the CMOS microprocessors. 80C85, 80C86 and 65C02 which are CMOS counterparts of their NMOS brethren 8085, 8086 and 6502 have been announced only recently. NSC 800 is a little different CMOS microprocessor falling in between Z80 and 8085. Quite some work has been done on CDP 1802 and it is popular in those applications where its low power consumption and noise immunity is of help for example space instrumentation and industrial and automatic controls. We have designed a single board microcomputer based on this microprocessor whose specifications are given in Appendix-A. It is a small (6"x4") card and has facilities for serial and parallel I/O.

The Microprocessor

The internal architecture of 1802 has been given in Figure-1. This microprocessor has 16 general purpose, 16 bit registers R(0) - R(F) which can be used as program counter, stack pointer as well as for temporary storage of data. Any register can be assigned any job except that after reset the microprocessor uses R(0) as a program counter. Data transfer normally take place between High and Low bytes of Register R(N) to D register (accumulator) and D register to the Memory pointed by any register. Exchange between registers has not been provided. Unfortunately this microprocessor does not provide, instructions for CALL and RETURN for subroutines. These have to be performed by software (Ref.2). There are large number of short branch instructions which can be used within one page of memory and long branches which can transfer control to anywhere in the memory. Four flags have been provided which can be used for input signals. A, Q flip-flop is also available which can be set and reset by software. Its output can be used as serial output. One Interrupt $\overline{INT}$ line is provided. Interrupt starts execution at locations pointed by R(1) register. SAVE, MARK and RETURN instructions have been provided to handle interrupt. DMA facility is on chip and can be used by $\overline{DMA\ IN}$, $\overline{DMA\ OUT}$ and SCO & SCI State code output lines. DMA uses R(0) as program counter.

The detailed software discussion is beyond the scope of this document and it has been given elsewhere[1]. A list of Instructions has been given in Appendix-B.

Hardware

The circuit diagram of the microcomputer card has been shown in Figure-2. 1802 is a static microprocessor and can be operated DC to 3 MHz depending upon the power supply voltage used. For a power supply voltage of +5 volts it is usually operated at 2 MHz or less. In this microcomputer it has been operated at 2 MHz. The microprocessor has a on chip clock oscillator and only a crystal and resistor need to be connected to pins 1 and 39. Two small capacitors (20 PF) are sometimes required from thse pins to ground. $\overline{EF4}$ and Q have been utilized for serial Input and Output respectively. Two transistors and associated circuitry have been provided for connecting it to a terminal with 20 mA current loop interface. The circuit works with a Teletype ASR33. For other terminals it is preferable to use RS 232C Interface which can be implemented on separate board. (Ref.8, p.84). State Code lines SC0 and SC1 have not been utilized. $\overline{\text{DMA IN}}$, $\overline{\text{DMA OUT}}$, $\overline{\text{INTERRUPT}}$, $\overline{EF1}$, $\overline{EF2}$ and $\overline{EF3}$ lines have been pulled up with 22 K/47K resistors. All the signals have been brought out on the 44 pin edge connector.

1802 utilizes multiplexed address bus. Address lines A8 to A15 appear on A0 to A7 lines for a brief period with beginning of each mahine cycle and can be latched in a 8 bit latch with the help of timing pulse TPA. In this board CDP-1852 has been used as a 8 bit latch. 4-16 decoder CD 4514 has been used for address decoding. The A15 line has extra logic by which it can be either kept permanently at 1 by external switch or else it can be connected to regular A15 line of 1802 (de-multiplexed of course). This way programs at 8000 or 0000 can be run, When A15 is '1', program execution starts at 8000, when it is '0' program execution would start at location 0000. Externally controlled A15 designated as A15' has been brought out on card edge connector to facilitate decoding of external memories.

Onboard 24 pin socket intended for a ROM/EPROM has facility to install any EPROM of upto 4 K bytes. It has been enabled 8000 to 8BFF. The 1K RAM has been realised by a pair of 2114 which are located at 8C00. ROM 1832 can be installed without any extra connection in the 24 pin socket. However, 2716 would require few short jumpers. IC's 4023 and 4011 have been used to perform task of generating memory enable signals.

1802 has 4 modes of operation decided by the control inputs $\overline{\text{CLEAR}}$ and $\overline{\text{WAIT}}$. These are controlled by two SPDT switches debounced by pair of inverters 4049. Switch connections have been brought to the edge connectors.

4 modes of operation are given below :

CLEAR	WAIT	MODE
H	H	RUN
H	L	PAUSE
L	H	RESET
L	L	LOAD

Normally RESET and RUN modes are used and only one switch connected as CLEAR can perform its function.

Software

This microcomputer can run on monitor software available on ROM type CDPR 512, (Ref.4). This requires use of serial data terminal for data entry and readout. The monitor is of autobaud type i.e. it adjusts its baud rate (within certain limits), on receiving the (CR) signal from the terminal. Operation is as follows :

1. Reset the microcomputer,
2. Set the Address to 8000,
3. Set the clear switch to RUN.
4. Press CR key on the terminal.

The monitor will respond with an asterick.*

Memory Load Command !M

!M command followed by Address (Hex) and a space loads the pair of hex digits at locations starting from the above address, for example

! M 0000 1122 33 44

will load 11 22 33 44 at location 0000, 0001, 0002 & 0003 respectively.

Memory read command ?M

?M command followed by Address (Hex) and a space followed by No. of bytes print the Address and contents of Memory at the above address.

?M 0000 08

will print 8 bytes of data stored at 0000.

Program Execute Command SP

SP command followed by Address (Hex) and a (CR) will transfer the control to the above address.

S P000 CR will start execution at 0000, location.

Register storage

Registers R(0) and R(F) are stored at locations 8C00 to 8C20 and can be read out by ?M8C 00 20 command. Full description of the UT4 monitor is given in Ref.3.

Acknowledgements

The author is thankful to Shri K.S. Modh who prepared the printed circuit artwork of the prototype and Shri J.T. Vinchhi for his help in fabrication of the unit. Thanks are also due to Shri Y.B. Acharya for the useful suggestions.

REFERENCES

1. COSMAC Micro-processor Product Guide MPG-180C.
2. User Manual for the CDP 1802 COSMAC Microprocessor MPM-201A.
3. COS/MOS Memories, Microprocessors and Support Systems SSD-280.
4. CDPR-512 - UT4 utility program operation Manual MPM-224.
5. Build the COSMAC "ELF" a low cost microcomputer, Part I, Joseph Weisbaker, Part-1. Popular Electronics, August 1976, pp.33-38.
6. "DO", Part II, Popular Electronics, Sept. 1976, pp.37-40.
7. How to upgrade A basic ELF micro-computer, Edward M. McCormick, Popular Electronics, February, 1978, p.65-68.
8. Expanding the ELF-II by Martin Meyer, Popular Electronics, March 1978, pp. 62-65.
9. A simple Microcomputer based on CMOS micro-processor, CDP-1802, R.N. Misra and Y.B. Acharya, J.I.E.T.E., Vol.27, No.12, 1981, pp.649-651.

Note : RCA product guides and data books (items 1-4) are available from COMEL Products 179/5 2nd Cross (1st Floor), Lower Palace, Orchards, Bangalore-560003.

APPENDIX-A

Specifications

1. Processor	CMOS microprocessor CDP 1802
2. Serial Interface	20 MA Loop Autobaud (can work upto 600 BPS)
3. Parallel Interface	A socket provided for CDP-1851 onboard. 20 I/O lines programmable. Memory Mapped, Separate 44 Pin connector provided.
4. Flags	$\overline{EF1}$, $\overline{EF2}$, $\overline{EF3}$ available. $\overline{INT}$, $\overline{DMA\ IN}$, $\overline{DMA\ OUT}$ lines available at the edge connector.

6. All signals, eg. Data Bus, Address Bus, $\overline{MRD}$, $\overline{MWR}$ etc. provided on the edge connector.
7. Size 6" x 4"
8. Power requirements + 5V (current depends on the ROM/RAM used and 20mA loop).

APPENDIX-B

INSTRUCTION SET OF 1802

OPCODE	MNEMONIC		OPCODE	MNEMONIC		OPCODE	MNEMONIC	
00	IDL		69	INP	1	C5	LSNQ	ADDR16
0N	LDN	,N	6A	INP	2	C6	LSNZ	ADDR16
1N	INC	,N	6B	INP	3	C7	LSNF	ADDR16
2N	DEC	,N	6C	INP	4	C8	NLBR	ADDR16
30	BR	ADDR8	6D	INP	5	C9	LBNQ	ADDR16
31	BQ	ADDR8	6E	INP	6	CA	LBNZ	ADDR16
32	BZ	ADDR8	6F	INP	7	CB	LBNF	ADDR16
33	BDF	ADDR8	70	RET		CC	LSIE	ADDR16
34	B1	ADDR8	71	DIS		CD	LSQ	ADDR16
35	B2	ADDR8	72	LDXA		CE	LSZ	ADDR16
36	B3	ADDR8	73	STXD		CF	LSDF	ADDR16
37	B4	ADDR8	74	ADC		DN	SEP	N
38	NBR	-	75	SDB		EN	SEX	N
39	BNQ	ADDR8	76	SHRC		F0	LDX	
3A	BNZ	ADDR8	77	SMB		F1	OR	
3B	BNF	ADDR8	78	SAV		F2	AND	
3C	BNI	ADDR8	79	MARK		F3	XOR	
3D	BN2	ADDR8	7A	REQ		F4	ADD	
3E	BN3	ADDR8	7B	SEQ		F5	SD	
3F	BN4	ADDR8	7C	ADCI	,D8	F6	SHR	
4N	LDA	,N	7D	SDBI	,D8	F7	SM	
5N	STA	,N	7E	SHLC		F8	LDI	,D8
60	IRX		7F	SMBI	,D8	F9	ORI	,D8
61	OUT	1	8N	GLO	,N	FA	ANI	,D8
62	OUT	2	9N	GHI	,N	FB	XRI	,D8
63	OUT	3	AN	PLO	,N	FC	ADI	,D8
64	OUT	4	BN	PHI	,N	FD	SDI	,D8
65	OUT	5	C0	LBR	,ADDR16	FE	SHL	
66	OUT	6	C1	LBQ	,ADDR16	FF	SMI	,D8
67	OUT	7	C2	LBZ	,ADDR16			
68			C3	LBDF	,ADDR16			
			C4	NOP				

APPENDIX-C

Pin connection of CMOS microcomputer

Component side		Pattern side	
1.	CLEAR	1	CLEAR
2	A15 = 1 (INPUT)	2	WAIT
3	WAIT	3	A15'
4	TTYIN	4	TTY IN
5	+5	5	GND
6	$\overline{\text{DMA IN}}$	6	TTY OUT
7	$\overline{\text{DMA OUT}}$	7	$\overline{\text{INT}}$
8	$\overline{\text{MWR}}$	8	SC1
9	Q	9	SC0
10	$\overline{\text{MRD}}$	10	TPA
11	TPB	11	D7
12	A7	12	D6
13	A6	13	D5
14	A5	14	D4
15	A4	15	D3
16	A3	16	D2
17	A2	17	D1
18	A1	18	D0
19	A0	19	N0
20	$\overline{\text{EF1}}$	20	N1
21	$\overline{\text{EF2}}$	21	N2
22	$\overline{\text{EF3}}$	22	GND

APPENDIX - D

Pin connection of I/O PORT

(Connector type - 225-805-22-H (Amphetronix Ltd.)

Component Side			Pattern side		
1	+5		1	+5	
2	NC		2	F	
3	NC		3	NC	
4	BRDY		4	NC	
5	BSTB	PORT B	5	NC	
6	B0		6	NC	
7	B1		7	ARDY	
8			8	ASTB	
9			9	A0	
10			10	A1	
11			11	A2	
12			12	A3	PORT A
13			13	A4	
14			14	A5	
15			15	A6	
16		NC	16	A7	
17			17	B7	
18			18	B6	PORT B
19			19	B5	
20			20	B4	
21			21	B3	
22			22	B2	

APPENDIX E

LIST OF COMPONENTS

INTEGRATED CIRCUITS

CDP 1802 Microprocessor	..	1
CDP 1852 8 bit latch	..	1
CDP 1851 I/O Port (Optional)	..	1
CDPR 512/2716 ROM/EPROM	..	1
2114/6514 1Kx4 RAM	..	2
CD 4514 4-16 Decoder	..	1
CD 4049 Hex Inverter	..	1
CD 4023 Triple 3IP NAND	..	1
CD 4011 Quad. 2 IP NAND	..	1

DISCRETE DEVICES

Crystal 2 MHz	..	1
Resistors 22K/15K 1/4W	..	6
1K	..	2
3K9	..	1
15K	..	2
220E	..	1
390E	..	1
Capacitors 100 µF 10V	..	1
0.1 µF 50V Ceramic	..	3

ILLUSTRATIONS

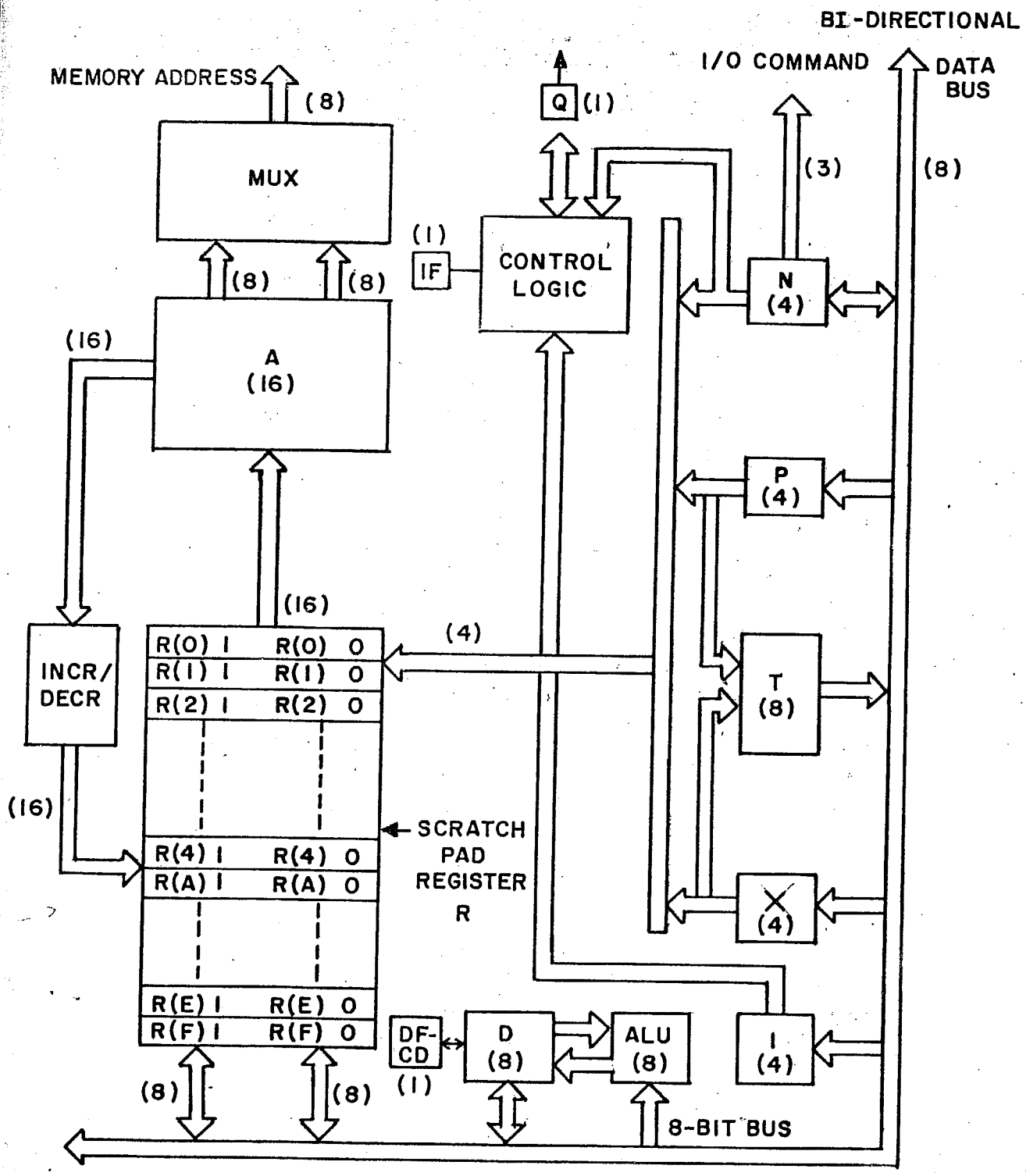


FIG.1 INTERNAL STRUCTURE OF THE CDP 1802 MICROPROCESSOR

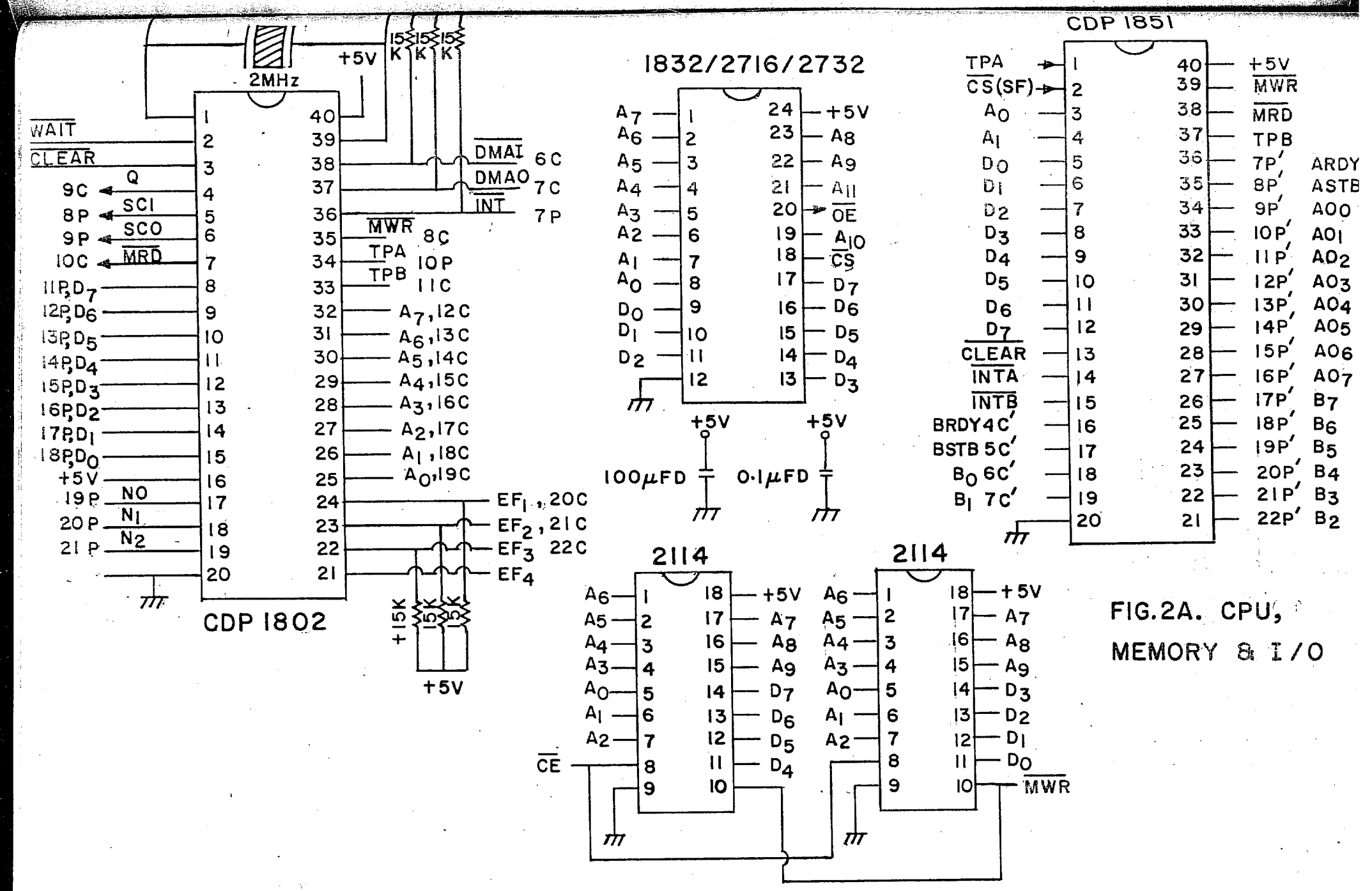


FIG.2A. CPU, MEMORY & I/O

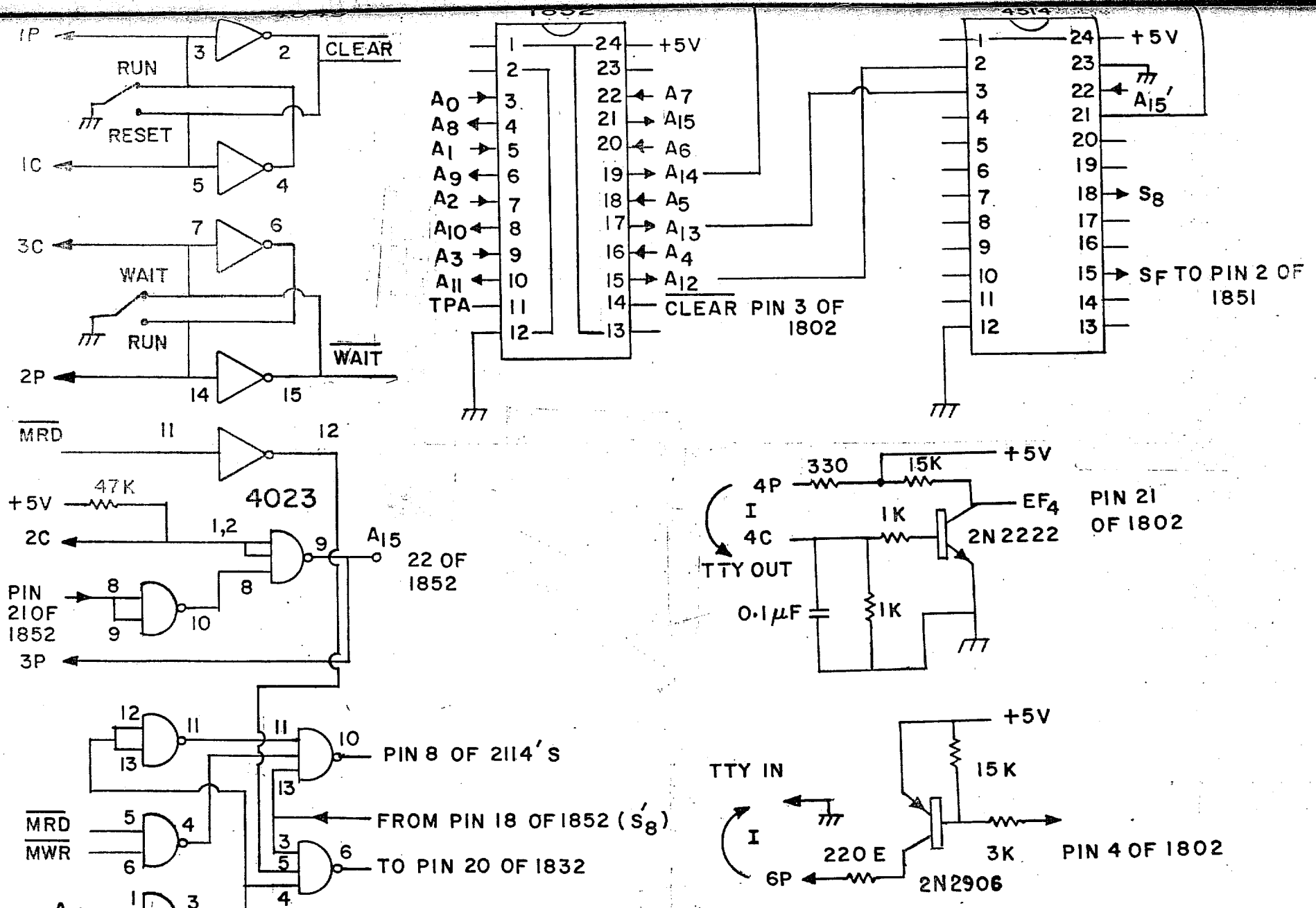
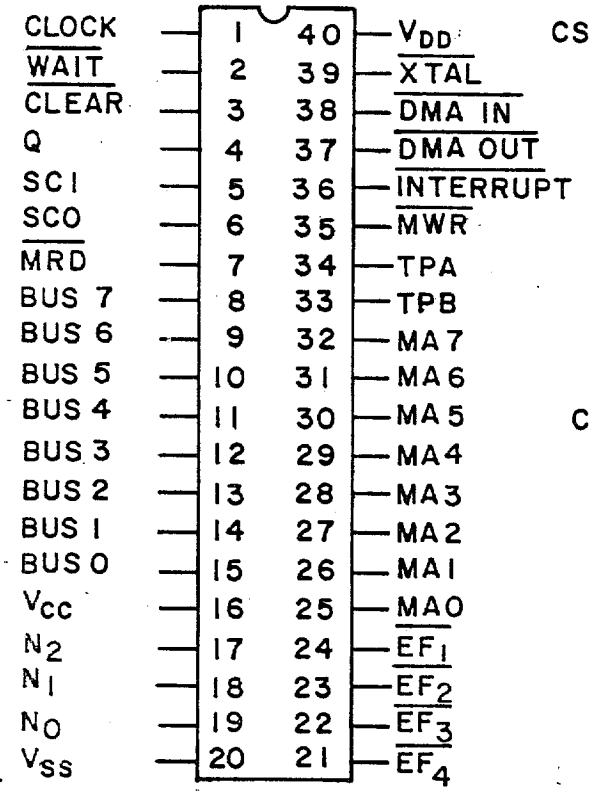


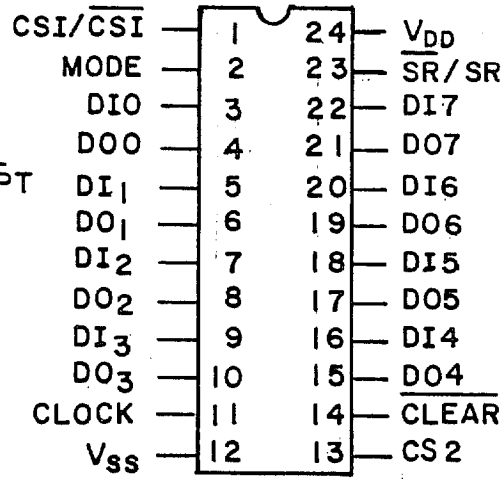
FIG.2B. CONTROL & SERIAL I/O

FIG.3 TERMINAL ASSIGNMENT DIAGRAMS

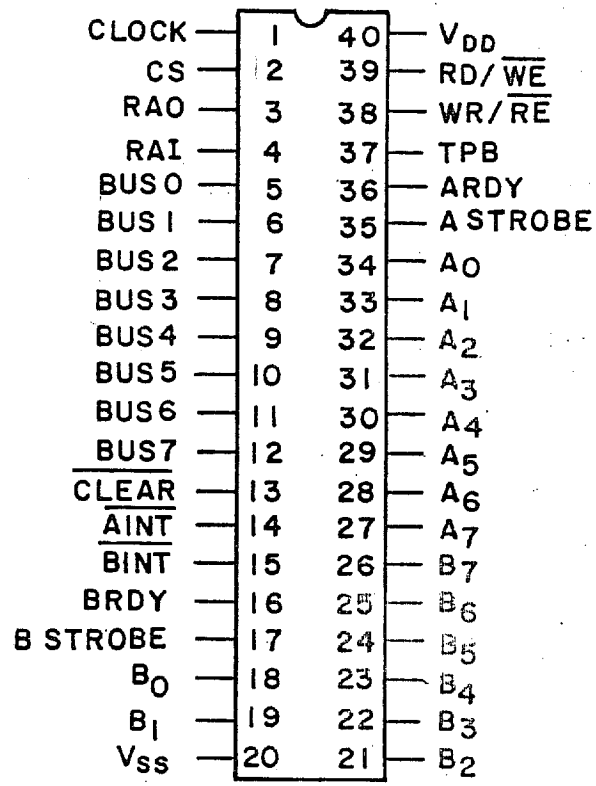
CDP 1802 COSMAC MICROPROCESSOR

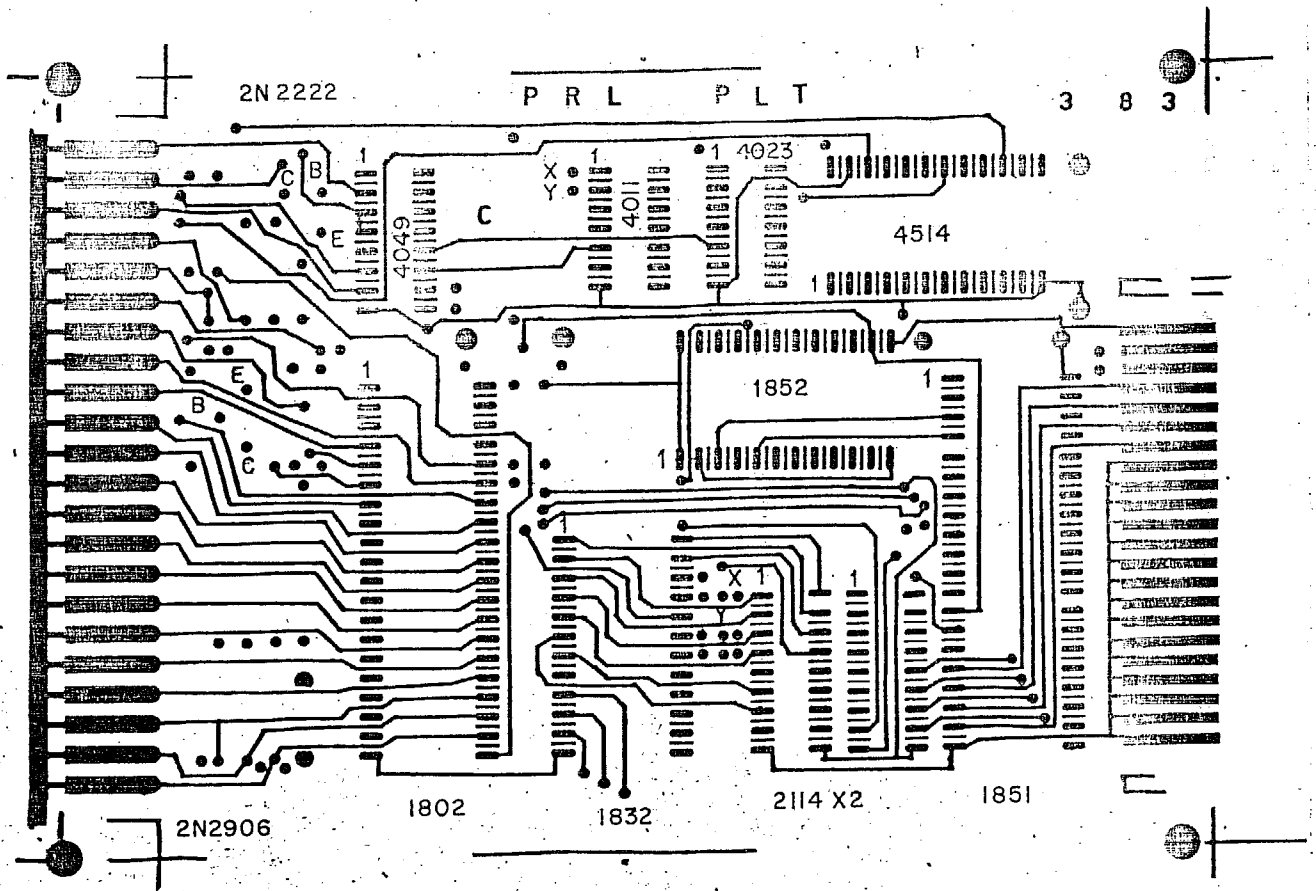


CDP 1852 BYTE I/O



CDP 1851 PROGRAMMABLE I/O INTERFACE





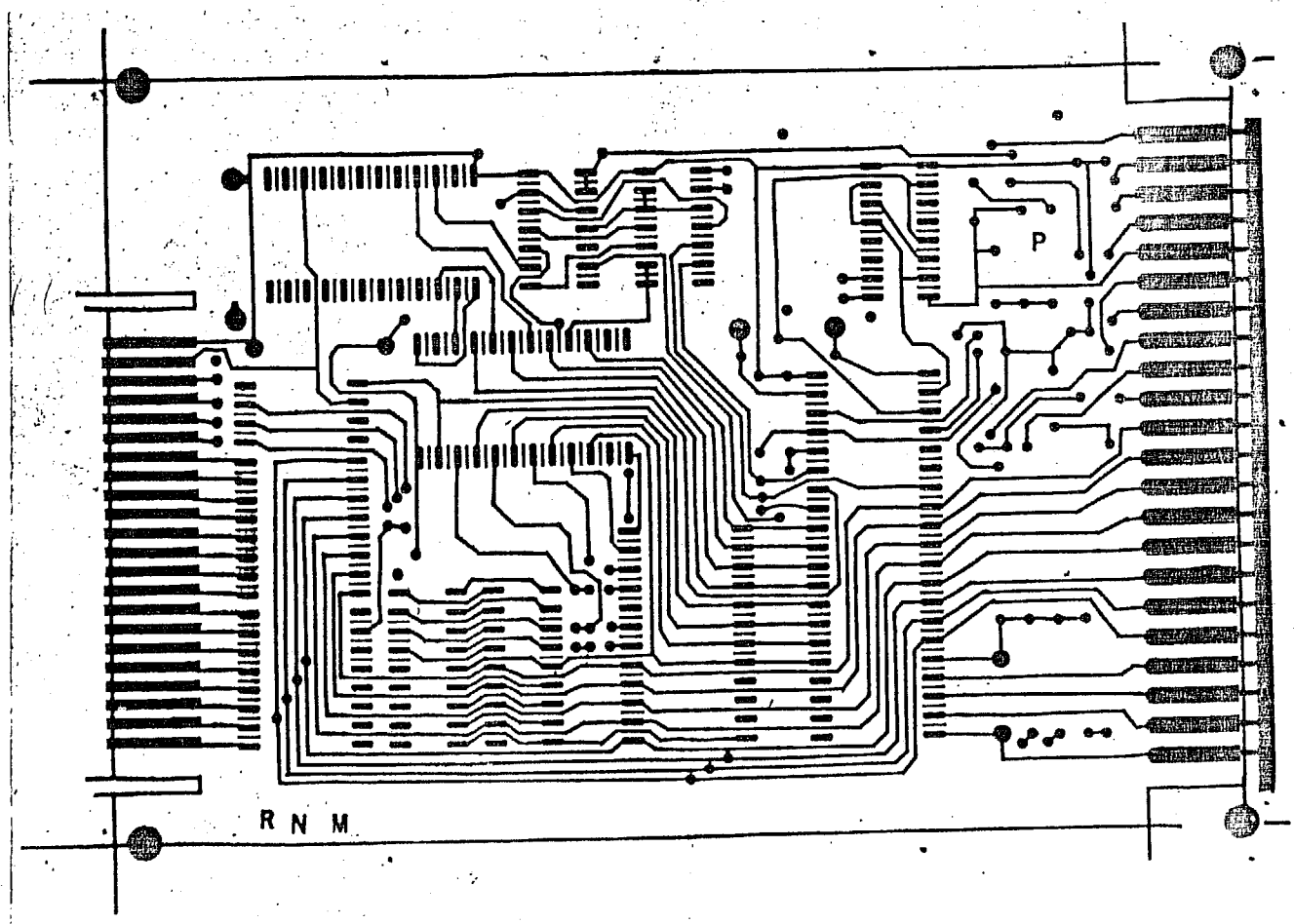


FIG.4. PRINTED CIRCUIT BOARD LAYOUT & PLACEMENT OF PARTS.