P R L

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A Computer Aided Design of Pseudo Random Bit Sequence Generator and its Applications in Telemetry

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A B S T R A C T

In this note the author describes the principle of operation and applications of a pseudorandom bit sequence (PRBS) generator. A system using the PRBS generator has been designed at PRL for the testing of the telemetry downlink for Solrad 11 satellites. A general computer program has been developed to compute maximal and actual lengths of the PRBS obtained from the simulated circuit specified by a user. A sample output using the above computer program is also shown.

1. INTRODUCTION :

Technique of using PRBS is picking up in the testing of equipments used in digital communication and satellite tone ranging. Engineers had been waiting for a noise source which is random as far as evaluation of a particular system performance is concerned but still predictable to get same set of measurements on a routine basis or the same source can be used as a test set for the evaluation of similar systems in day to day testing. The testing, morever, should be quick and should also be free from subjective errors as far as practicable. PRBS satisfies all these conditions. It has numerous useful properties for the testing of a variety of equipments, large flexibility in controlling output patterns and is still very simple in construction.

2. PRINCIPLE OF OPERATION :

An N-stage closed loop shift register with feedback tappings is the heart of a PRBS generator (fig.1). The exclusive - OR output from two of the stages of the shift register (mod 2 addition) is fed back into the input of the first stage and a PRBS is available at the output. By proper selection of two stages - the last one and an intermediate - a maximal length PRBS can be obtained. A maximal length sequence is the one where all possible combinations of N 1's and 0's (except all 0's) is generated without repeating any combination, N being the number of stages in the

shift register. The sequence length in this case is 2^N-1 bits. Different bit-rates can be realized by just changing the rate of clock pulses to the shift register. An interesting property of the maximal length PRBS is that each of the half-rate bit sequences - the two sequences formed by taking alternate bits - follows the same orginal full rate sequence. By interlacing two such sequences a maximal length sequence of double the rate can be generated economically, as the cost of the logic circuits increases with increasing speed requirements.

In the maximal length sequence of complete length the number of ones is one more than the number of zeros. If a run of length n means, n consecutive outputs of same type, the maximal length PRBS has approximately half the runs of length 1, one fourth of length 2, one eighth of length 3 and so forth.

3. APPLICATIONS :

In a typical set up[1] for test and evaluation of digital systems a 'data generator' produces pseudo-random pattern of selected length as a stimulus for the system under test. The 'error detector' generates an indentical pattern internally, compares it bit by bit with the output of the system under test and determiues the rate at which errors occur. The

statistical nature of a pseudorandom binary sequence is very similar to that of a truly random pulse train normally found in any PCM system. The digital system under test can be checked for bit error rate, block error rate and skew symmetry[2] directly. The amount and rate of jitter in the data can be simulated by using a VCO in the 'data generator' as a source of clock pulses. Similarly the dc shift and carrier loss conditions can also be simulated.

By using the technique of PRBS, the PCM signals were simulated in Physical Research Laboratory (PRL), Ahmedabad, for testing the PCM decoding equipment indiginously developed and built to decipher the signals from SOLRAD 11A and B Satellites. These satellites were launched by Naval Research Laboratory, Washington D.C., U.S.A., in March 1976. They are nearly 180 degrees apart in the circular orbit at about 119,000 km. height above the surface of the earth. The signals are convolutionally encoded with constraint length 7 and rate 1/2. The data rate is 102.4 bits/sec., and there are 32 words of 12 bits each in one PCM frame with sync pattern of 1101 0111 0101. The simulated PCM signal has the same bit rate and uses the PRBS between two successive frame sync patterns before it is convolutionally encoded. The complete test set-up is shown in fig.2.

By controlling the RF transmitter output the performance of the entire receiving telemetry link is tested a few minutes before each 'satellite pass' lasting about twelve hours. For the same antenna gain, and same Noise Figure of the receiving chain of equipments, an operator, before the pass, can monitor the RF power required to be transmitted to keep the PCM decommutator at the locking threshlaold, which is indicated by the LOCK lamp on its front panel.

PRBS can be easily adapted to test communication circuits as its power spectrum can be easily controlled by either changing the number of stages (N) of the shift register or the clock frequency (fc) or both. The spectrum[3] is of $\frac{\sin x}{x}$ type with nulls at fc and its harmonics and the spectral line width of $fc/2^N-1$ Hz. Its probability density distribution almost matches with that of true gaussian noise if the output is properly filtered. In modern satellite tone ranging equipments also, use of PRBS is becoming popular. By using active transponder on board the satellite, delay between the transmitted and received PRBS is measured to compute the range of the satellite. This technique is very useful for satellites in near synchronous orbits, as the conventional radar techniques demand very narrow pulses

and hence large bandwidth for the required resolution.

4. SEQUENCE TESTING PROCEDURES :

Though simple in construction, the testing of PRBS for its output pattern is really a task. The maximal length increases exponentially with number of stages used in the shift register. For small sequence length, it is possible to monitor it on an oscilloscope or a logic state analyser. This method starts becoming impractical if the number of stages exceeds 5 (maximum length = 31 bits). It is very interesting to note that there is no standard iterative formula to select the feedback stages for obtaining maximal length pattern. The circuit has to be built by trial and error method as intuition proves to be of little help. Morever, for the same number of stages in the shift register, a number of maximal length sequences are possible. The sequence can be worked out on paper for a particular feedback configuration but this method also becomes quite cumbersome for more number of stages. Alternately, an arbitrary selection of feedback stages can be made, a circuit can be hooked up and the output can be recorded on digital tape for successive clock pulses numbering minimum three times the maximal length expected. The tape is read into computer and a printout of 1's and 0's is obtained by suitable software

program. The length of actual sequence, after which the entire sequence repeats, can also be found out by software. This method was successfully tested in PRL for upto 12 stages in the shift-register. This finally led to the software simulation of the circuits for obtaining PRBS.

5. CIRCUIT SIMULATION THROUGH SOFTWARE :

A new computer program (fig.3) has been developed to find the maximal and actual lengths of the sequences for user selected number of stages and the feedback configuration. The software is written in FORTRAN IV language and has been successfully implemented on PDP11V03 microcomputer. The program has been developed in an interacting mode i.e. the user can select the number of stages in the shift register as well as the feedback stages during its execution phase. The program was converted into the machine language by using softwave Fortran compiler available for the PDP11V03 system in PRL. The compiled output has been stored on a floppy disk. User can call the compiled program into the computer memory by issuing a command through the console typewriter (DEC writer, LA36). User types the number of shift register stages desired and the feedback stages to be selected in response to the programmed querries from the computer. After the computation

of the maximal and actual lengths, the result is printed on the console typewriter and the computer asks for the next set of values the user may wish to try. Selection of the last stage in the shift register for feedback is necessary even if the user wants to simulate a pseudorandom pattern which is not the maximal length one. As an example, in a particular PCM system if the number of bits in the frame sync pattern is N, the PCM frame length may be much less than the maximum length sequence formed by an N - stage shift-register. If IA and IB are the two feedback stages such that $IA < IB < N$, the bit sequence available at the output of the Nth stage will have maximum length of $2^{IB}-1$ bits only, delayed by (N-IB) bits. In this case computer prints out on the console that circuit has entred in a subcycle and the user can type new set of desired parameters.

The starting state for all the shift register stages is assumed to be 'set' but can be easily modified if user requires it for a specific application. A sample output (fig.4) shows the versatility of the program developed. A user can select upto 30 stages in the shift register. This limitation arises because of the limited user area available from the computer memory and hence its number

handling capacity. A few statements can be added into the program to obtain the printout in 1's and 0's of the actual sequence for the selected circuit configuration. In a different type of feedback configuration the output of the last stage can be fed directly to the input. The input of an intermediate stage - i thstage - is controlled by the (i-1)th stage and the feedback from last stage through an exclusive OR gate. This configuration can also be simulated by modifying the feedback statement in the above computer program.

6. CONCLUSIONS :

The software developed here, for simulating the PRBS generator is shown to be very useful in finding out the circuit configuration for any desired sequence length normally required in the telemetry applications. It was a very handy tool for testing the PCM bit synchronizer and decommutator indiginously developed in PRL for SOLRAD 11 data processing. It is now possible to design the PRBS generator within a short time making use of the above softwave.

ACKNOWLEDGEMENTS :

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2. J.R.Duerr, "A Data Error Analyzer for Tracking Down Problems in Data Communications" Hewlett - Packard Journal, Vol. 25/6, PP 11-20, February 1974.

3. R.G.Rolls, P.R.M. Webster, "Pseudorandom noise sources as stimuli for quantization distortion measurements on P.C.M. systems" Marconi Instrumentation, Volume 14/4, PP 89-96, April 1974.

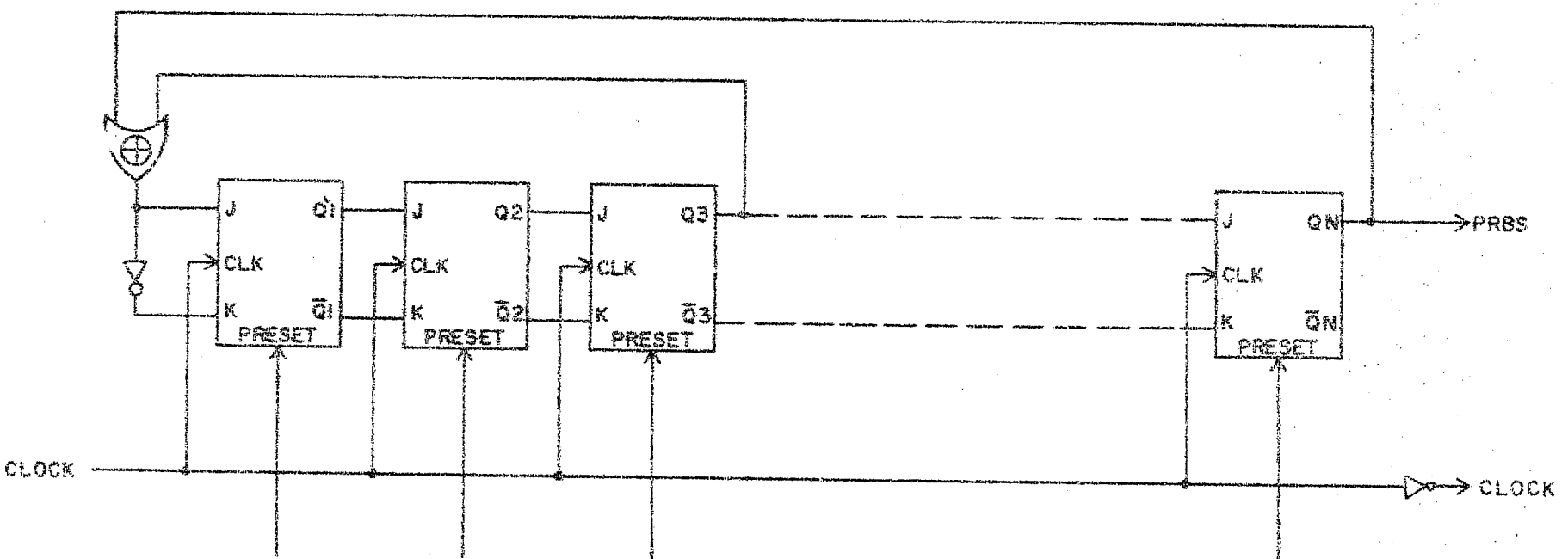


Fig.1 : PRBS generator - typical circuit.

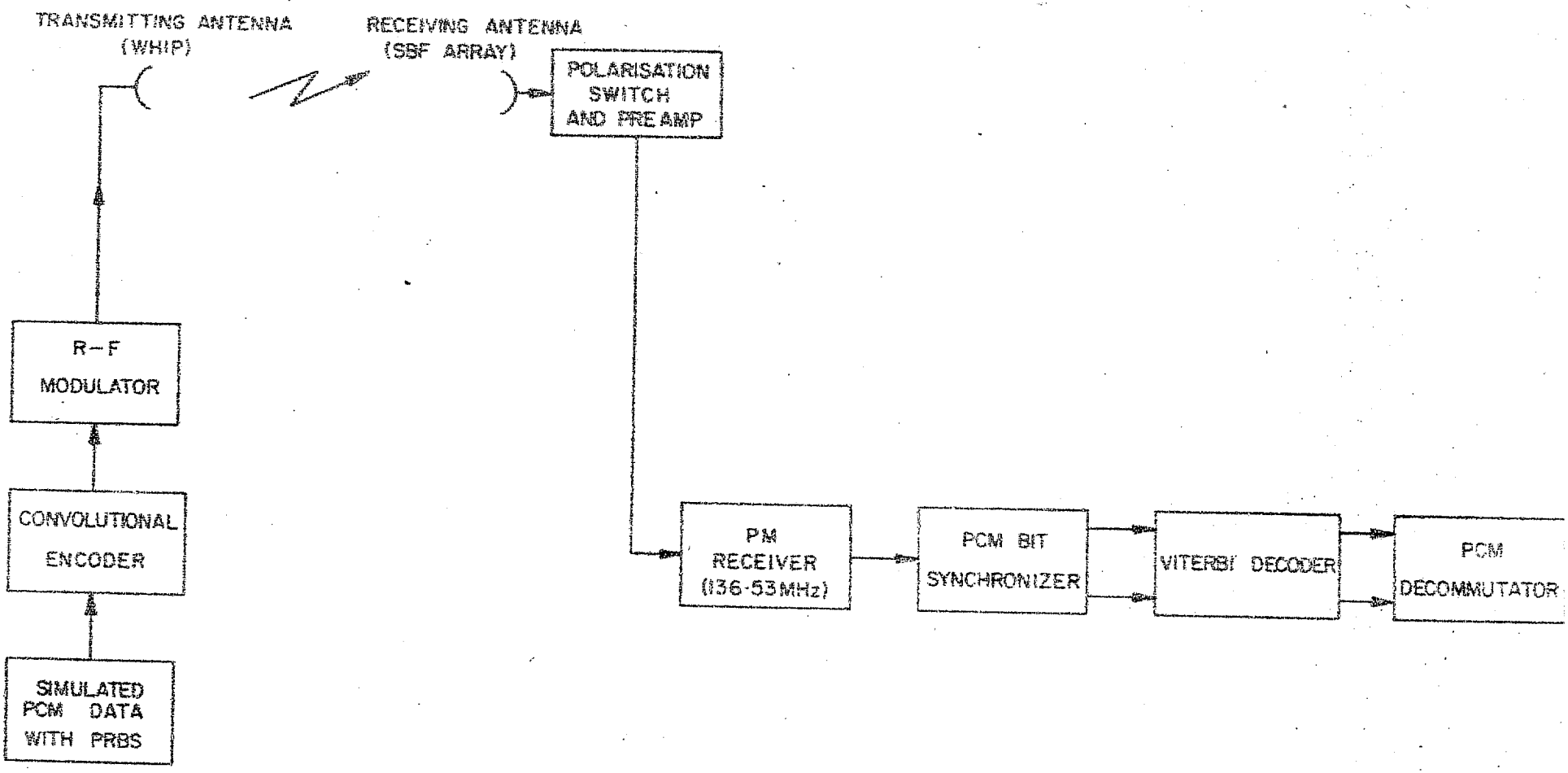
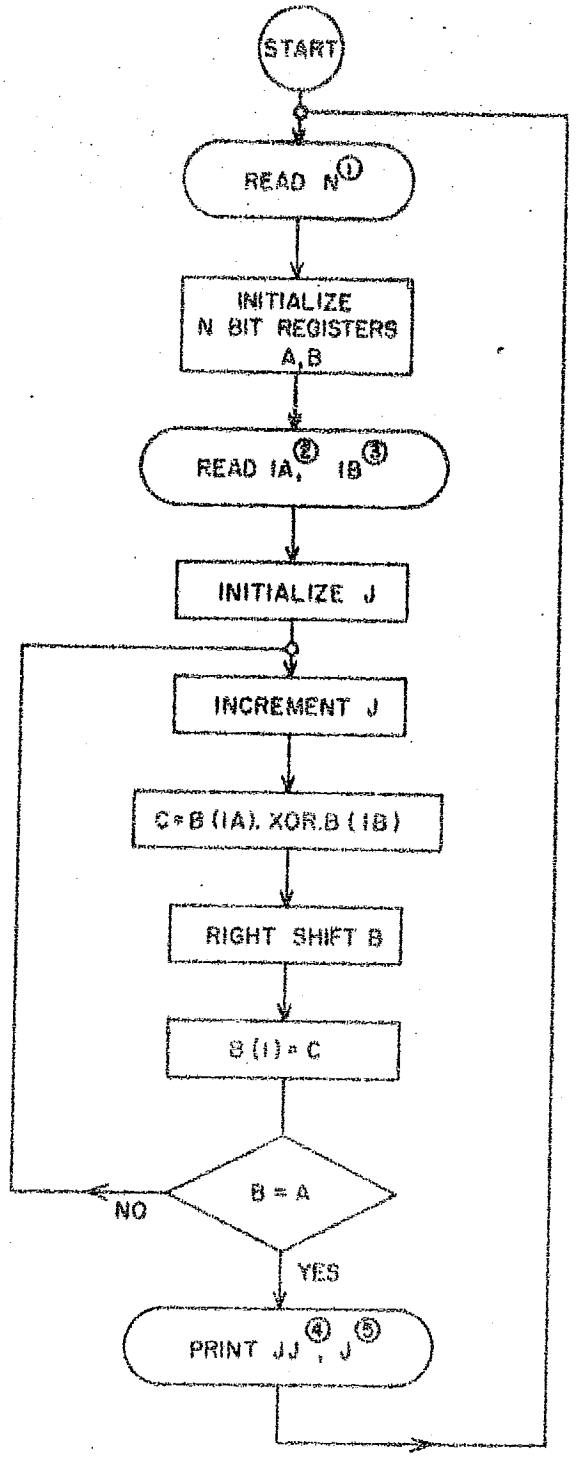


Fig.2 : Test set-up for SOLRAD 11 telemetry downlink.



① NUMBER OF STAGES IN THE SHIFT REGISTER
② FEED-BACK STAGE
③ FEED-BACK STAGE
④ MAXIMAL LENGTH
⑤ ACTUAL LENGTH

Fig.3 : Flow chart of program for computing PRBS length.

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^C
.RUN DX1:PSEUDO

   THIS PROGRAM COMPUTES MAXIMAL AND ACTUAL LENGTH OF
   A PSEUDO RANDOM BIT SEQUENCE GENERATED BY AN N-STAGE
   CLOSED LOOP SHIFT REGISTER WITH FEEDBACK THROUGH AN
   EXCLUSIVE-OR GATE FROM TWO USER SELECTED STAGES.


   HOW MANY STAGES IN SHIFT REGISTER ?
   7

   FEEDBACK FROM WHICH TWO STAGES ?
   2       7

    MAXIMAL LENGTH=        127....BITS
    ACTUAL LENGTH=         93.....BITS


   HOW MANY STAGES IN SHIFT REGISTER ?
   7

   FEEDBACK FROM WHICH TWO STAGES ?
   1       7

    MAXIMAL LENGTH=        127....BITS
    ACTUAL LENGTH=         127....BITS


   HOW MANY STAGES IN SHIFT REGISTER ?
   4

   FEEDBACK FROM WHICH TWO STAGES ?
   1       4

    MAXIMAL LENGTH=        15.....BITS
    ACTUAL LENGTH=         15.....BITS


   HOW MANY STAGES IN SHIFT REGISTER ?
   4

   FEEDBACK FROM WHICH TWO STAGES ?
   1       3

   CIRCUIT ENTERS IN A SUBCYCLE AND
   DOES NOT RETURN TO INITIAL STATE
```

Fig.4: Sample output of the computer program shown in fig.3.