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A 40-CHANNEL 1-BIT DIGITAL AUTOCORRELATOR FOR RF SPECTRAL LINE RECEIVER

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Abstract

In this report, we shall first present an outline of the theory of the method of autocorrelation of measuring power spectra of random signals with gaussian statistics, with particular reference to the 1-bit method of computing autocorrelation functions. This is then followed by detailed descriptions of the subsystems of a 40-channel 1-bit autocorrelator developed in the Infrared Astronomy Area of the Physical Research Laboratory, Ahmedabad. Using noise input, the correlator was tested in conjunction with the 70 MHz IF amplifier, which forms a part of an RF spectral line receiver developed for the purpose of detecting OH emissions at 18 cm wavelength from interstellar hydroxyl molecules. Two sets, one of 7 and the other of 50 minutes of integration time, of test observations were analysed to compute autocorrelation functions and power spectra. It is concluded that the highest accuracy of spectral measurements would be achieved provided the latter are made in the flat region of the response of the bandpass filter.

I. Introduction:

The 21-channel 1-bit digital autocorrelator developed by Weinreb (1963) at M.I.T., U.S.A. established the potential of this method as a powerful tool for making high resolution observations of narrow band emissions, e.g. RF emissions from interstellar hydroxyl (OH) radical at 18 cm , water molecule (H_2O) at 1.35 cm, carbon monoxide (CO) at 2.6 mm wavelength etc. Since then many radio astronomy observatories all over the world are using this device as an "on-line" correlator for detection of radio frequency line emissions (Davies et al. 1969; Pell and Little, 1975; Ables et al. 1975; Pointon, 1977). A correlation receiver provides radio astronomers with, effectively, a variable filter bank whose overall frequency range can be controlled by simply varying the clock-rate of the autocorrelator. This makes a correlator versatile in the sense that different astronomical problems, requiring different overall bandwidths, can be studied using the same correlator.

II. The method of Autocorrelation Function for measurement of Power Spectra:

The power spectrum P(f) of a time series x(t) is defined as

$$P(f) = 2 \int_{-\infty}^{\infty} R(\tau) \exp(-j2\pi f \tau) d\tau \qquad \ldots (1)$$

which is the Fourier Transform (FT) of the Autocorrelation Function (ACF), $R(\tau)$, given by

$$R(\tau) = \lim_{T \to \infty} \frac{1}{2T} \int_{-T}^{T} x(t).x(t+\tau)d\tau \quad \ldots (2)$$

τ being the time lags.

In practice, however, both these expressions need modifications as follows:

(a) Since $x(t)$ is available only for a finite duration, τ and t should have finite limits. In other words, both $R(\tau)$ and $x(t)$ must be truncated.

(b) Due to the truncating of $x(t)$, there will be a finite number of multiplications and intergrations as seen from eqn. (2), and $R(\tau)$ will be estimated for discrete values of τ $(=n \triangle \tau)$, where n is an integer varying from 0 to N-1, N being the total number of time lags.

(c) If the data are digitized, two more modifications are required: (i) $x(t)$ will be sampled periodically giving samples $x(k \triangle t)$, where k is an integer between 1 and K, the total number of samples. (ii) Each of these samples must be clipped or quantized. For example,

in the 1-bit digitization only two amplitude ranges $x(k\Delta t) > 0$ and $x(k\Delta t) < 0$ are used with little effect on the spectral measurement.

Introducing the modifications of sampling and truncation only into eqn. (1) and (2), we obtain

$$P'(f)=2\Delta T \sum R'(n\Delta T)\, w(n\Delta T)\, \exp(-j2\pi fn\Delta T) \quad .. (3)$$

$$R'(n\Delta T)= \frac{1}{K} \sum_{k=1}^{K} x(k\Delta T).\, x(k\Delta T + |n|\Delta T) \quad .. (4)$$

Eqn.(3) and (4) do not include modifications due to quantization. $(n\Delta T)$ is the weighting function introduced to take care of the smoothing which is necessary after truncating the ACF. Thus, $R(n\Delta T)$ need not be known for $|n| \geq N$.

Taking the statistical average of eqn.(3) yields

$$P^*(f)=\overline{P'(f)}=2\Delta T \sum_{n=-\infty}^{\infty} R'(n\Delta T)\, w(n\Delta T)\, \exp(-j2\pi fn\Delta T) \quad .. (5)$$

This means, the mean $P^*(f)$ of 1-bit spectral estimate is given by the F.T. of the truncated and sampled ACF.

Now, the relationship between $P^*(f)$ and $P(f)$, the true power spectrum, is given by substituting the

following inverse F.T. of $R(n \Delta\tau)$ and $w(n \Delta\tau)$ in eqn.(5) :

$$R(n \Delta\tau) = \tfrac{1}{2} \int_{-\infty}^{\infty} P(f) \exp(j2\pi fn \Delta\tau) df \quad .. (6)$$

$$w(n \Delta\tau) = \int_{-\infty}^{\infty} W(f') \exp(j2\pi f' n \Delta\tau) df \quad .. (7)$$

We get,

$$P^*(f) = \sum_{i=-\infty}^{\infty} \int_{-\infty}^{\infty} P(f) W(f'-f-if_s) df \quad .. (8)$$

where the sampling frequency $f_s = (\Delta\tau)^{-1}$, and i is an integer. The operations described by eqn. (8) are depicted in Figure 1. Two operations are performed on $P(f)$:

(i) $P(f)$ is convolved with $W(f)$, a narrow band function of bandwidth, $\Delta f = f_s/N$. Smoothing results due to convolution so that spectral features narrower than Δf are wiped out.

(ii) Thus smoothed spectrum is repeated periodically at integral multiples of f_s.

$$P^*(f) = \int_{-\infty}^{\infty} P(f)\, W(f'-f)\, df, \quad |f| < f_s/2$$

$$= 0, \quad |f| > f_s/2 \qquad \ldots (9)$$

In practice, $f_s = 2\, B_{20}$ where B_{20} is the spectrum width at which it is 20 db below its mid-band value. With this sampling frequency, less than 1% error occurs in the measurement of power spectrum near the mid-band due to sampling.

III. Choice of the weighting function, $w(n \Delta T)$:

For most applications three weighting functions are common. Figure 2 shows the uniform, cosine (or Hanning) and Blackman weighting functions. The first gives a narrow main lobe but high secondary responses, while the Blackman function yields a broad main lobe and low (-29 db) secondary lobes. The Hanning function is very commonly used in radio astronomy applications.

The shape of the spectral scanning function, $W(f)$, depends on its ACF, $w(n \Delta T)$ which must satisfy the following restrictions:

$$w(0) = 1 = \int_{-\infty}^{\infty} W(f)df$$

$$w(n\Delta\tau) = w(-n\Delta\tau) \qquad \ldots (10)$$

$$w(n\Delta\tau) = 0, \text{ for } |n| \geq N$$

IV. The 1-bit method of computing Autocorrelation Functions:

Most of the RF line emissions from interstellar molecules are very weak in intensity and, therefore, highly sensitive spectral line receivers are needed for spectral analysis work in radio astronomy. Due to higher accuracy of measurement digital techniques are preferred to analog techniques. Many-bit or finely quantized digital techniques are very cumbersome and expensive. A 1-bit per sample correlator, which is simple in construction and inexpensive, while retaining the phase information of a signal, looses its amplitude information. But, by applying the Van Vleck (1966) correction, a good estimate of the ACF can be made. Figure 3 describes the operation of a 1-bit autocorrelator which is based on the Van Vleck's theorem.

According to this theorem, if x(t) is a sample of a time data series with gaussian statistics and zero

mean, then y(t), its hard-clipped version, is defined as

$$y(t)=1, \text{ for } x(t) > 0$$
$$= 0, \text{ for } x(t) < 0 \quad \ldots (11)$$

Now, if $\rho_x(\tau)$ and $\rho_y(\tau)$ are the true normalized ACF's of x(t) and y(t) respectively, then

$$\rho_x(\tau) = \text{Sin}\left[\pi/2 \quad \rho_y(\tau)\right] \quad \ldots (12)$$

where $\rho_x(\tau) = \frac{R_x(\tau)}{R_x(0)}$, $\rho_y(\tau) = \frac{R_y(\tau)}{R_y(0)}$

Eqn. (12) is the Van Vleck correction which converts the normalized ACF of the clipped signal, $\rho_y(\tau)$, into the normalized ACF of the original signal, $\rho_x(\tau)$. The estimates of ρ_x and ρ_y are defined as

$$\rho_x'(\tau) = \sin\left[\pi/2 \quad \rho_y'(\tau)\right] \quad \ldots (13)$$

where $$\rho_y'(\tau) = \frac{1}{K}\sum_{k=1}^{K} y(k\Delta t).\, y(k\Delta t + \tau) \quad \ldots (14)$$

and $\tau = n\Delta\tau$.

Eqn. (14) describes the operation performed by a 1-bit autocorrelator. It should be noted here that in addition to the signal being of gaussian statistics, it must be be band-limited to a finite bandwidth beyond which the power spectrum is made negligible. The sampling should then be made at a rate which is at least equal to the Nyquist criterion.

V. Experimental Set-up:

A block diagram of the 1-bit digital autocorrelator alongwith a single side-band (SSB) receiver is shown in Figure 4. A wide band noise generator was used as the source of signal for testing the performance of the autocorrelator system. The receiver was used to yield an output noise level of about 2 V p/p necessary for the bandpass filter.

V.(a) Buffer Amplifier, Filter and Clipper:

In Figure 5 are shown the circuits of a buffer amplifier, an active filter and a single stage clipper. A unity gain buffer amplifier is built using IC 741-1 in an inverting mode. The non-inverting input is connected to a resistance network (R_1, R_2 and R_3) and a potentiometer (R_4) to overcome any DC-voltage appearing at the output of a single-side-band receiver. This

is followed by an active filter, built using IC 741-2 to 7. As it is already pointed out, one of the basic requirements of a 1-bit digital autocorrelator is that the signal must be band limited. The filter is designed using a combination of low-pass and high-pass filters. Its response is shown in Figure 6. A roll-off of 20 db per octave on high and low frequency sides was achieved. The response is flat from 4 kHz to 40 kHz with rms fluctuations of the order of 0.5 db.

The output of the filter is fed to an amplifier made using an op-amp (741-8). This is also used in an inverting mode and the non-inverting input is connected to a voltage divider network formed by the resisters R_5 through R_8 and a trim-potentiometer R_9 through a 1K resistor. This amplifier is required to raise the voltage level sufficiently high to overcome the effect due to non-zero clipping. The output is then fed to a clipper made using an op-amp (710). By definition, an ideal clipper is one having characteristics such that its output $y(t)$ = logical 1, when the input $x(t) > 0$ and output $y(t)$ = logic 0, when the input $x(t) < 0$. But in practice this cannot be realised because of various reasons such as stability, noise problems, etc. In practice, some limit on amplitude is fixed so that $y(t)$ = logical 1, when the input, $x(t) > \epsilon$ and

$y(t)$ = logic 0, when the input $x(t) < \epsilon$. The value of ϵ depends upon the circuit components. In our case, the input applied to the clipper was around 8 volts p/p and the clipping level ϵ = 150 mV. Thus, the ratio of the input to the clipping level was 34.5 db, reducing the non-zero clipping effect to a great extent.

V.(b) Sampler, Synchronous Detector and Correlator:

The output of the clipper, $y(t)$, is then applied to the sampler shown in Figure 7. The sampler output, $y(k \Delta t)$, is the instantaneous value of $y\ t)$ at $t = k\Delta t$. The data are sampled at regular intervals at the clock rate, equal to that of sampling frequency, f_s, using 747 D type edge-triggered Flip Flop (F/F). According to the Nyquist criterion $f_s = 2\ B_{20} = 200$ kHz. B_{20} means the 20 dB bandwidth. The $y(t)$ information present at the input D is transferred to the output Q on the positive-going edge of the clock pulse. The advantage of this IC (7474) is that the clock-triggering occurs at a voltage level of the clock pulse and is not related to transition time of the positive-going pulse. Irrespective of whether the clock input is at high level or at low level, the input signal at D has no effect on the output Q. One can set/reset the F/F (7474) randomly between two sampling pulses so that the error is random

if F/F refers to its previous state. This will reduce the possibility of unwanted high correlation between successive samples which may cause serious errors in the spectrum.

The duration t_s of the sampling pulse was 0.5μ-seconds, which is 1/20th of the period of the highest frequency components of the signal. The output of the sampler is then passed over to a synchronous detector, where it is compared with a control signal C. C=1 when the receiver is connected to the noise source and C=0 when it is connected to a reference, in case the receiver is used in a switched mode. As we were not operating in the switched mode, the line C is permanently connected to logical 1. It also has a control signal B and the correlator is 'ON' only when B=1. Thus, when B=1 and C=1, P=Ao and Q=$\overline{Ao}$; when B=1, and C=0, P=$\overline{Ao}$ and Q=Ao; and when B=0, P=Q=0. Thus, the outputs are P and Q where P=B (AoC + $\bar{A}o\bar{C}$) and Q=B (Ao$\bar{C}$ + $\bar{A}$oC) which are then fed to the 1-bit correlator.

The correlator consists of a series of 1-bit shift-registers (7473) and comparators (7402). A shift-register shifts the information by 1-bit at the clock rate and thus delays the information by an element of time $\triangle T = \frac{1}{f_s}$. The output of each stage of the

shift-register is compared with the signal obtained from the synchronous detector. If they are same, then the output of the correlator is logical 1. A read pulse, T_R, is applied to the read circuit (7402) which gives out a pulse to the counter. The rate of T_R is the same as that of f_s, so as to have synchronism in the output pulses. The logic equations for the outputs are:

$$T_R\,(PA_1 + Q\bar{A}_1)$$

$$= T_R \left[B\,(A_0C + \bar{A}_0\bar{C})\;\; A_1 + B\,(A_0\bar{C} + \bar{A}_0C)\;\bar{A}_1 \right]$$

$$= T_R \cdot B \left[A_0A_1C + \bar{A}_0A_1\bar{C} + A_0\bar{A}_1\bar{C} + \bar{A}_0\bar{A}_1C \right] \quad \ldots \quad (15)$$

Thus, when C=1 and B=1, a pulse is given to the counter at the occurrence of the T_R pulse when both the inputs of the comparator are same. The outputs are then connected to Data Counter register circuits. In all there are 40 channels of the correlator, comprising 39 shift-registors (giving 39 time lags) and comparators together with 1 channel corresponding to zero time lag. Ideally, the true autocorrelation would mean that a pulse should be subtracted from the counters when the comparator output is zero, but this needs very expensive up/down counters and an appropriate controller. Since

the operation of the counter can change at the maximum rate of f_s, it is not advisable to use the up/down counter system. This is achieved by simple calculations as will be described later. To have the zero lag observations, the number of samples is directly counted in the first channel.

V.(c) Data Counter Registers:

In Figure 8 is shown one channel of the data counter register circuit. The output of each channel of the correlator is fed to a series of nine decade counter chips (7490). The maximum capacity of each counter is 10^9 counts. On a single card 4-channel data are accumulated and stored. All the 4-bit outputs of each of the decade counter chips (7490) are connected to the four inputs of a parallel-in parallel-out, serial-in serial-out and right and left shift-register chip (7495). Except the left shift all the available operation modes of this chip (7495) are used. Thus, the 36-bit output of the data counter of each channel is connected to the inputs of 7495 chips. All Q_D outputs of the data-registers (7495) are connected to the serial inputs (D_S) of the next chip. Since there are only four channels on any single card the serial input (D_S) of the 4th channel is permanently connected to

ground. Its Q_D output of the most significant digit data-register is connected to the serial input (D_s) of the 3rd channel data-register. The most significant digit Q_D output of the 3rd channel data-register is then connected to the serial input (D_s) of the 2nd channel data-register and finally the Q_D output of its most significant digit data-register is connected to the serial input (D_s) of the 1st channel data-register. The Q_D output of the most significant digit data-register of the 1st channel is connected to data multiplexer circuits. Thus, there are 10 outputs from the data counter register circuits to the data multiplexer. Various pulses like, transfer of information, rest pulse, right shift, mode controls, etc., are generated by the control circuits and are explained in detail later. At the end of the integration time T, the switch S_1 (Figure 11) of the control programmer is pressed to give a "GO" pulse. This, in turn, first transfers the data from output of the decade counter to the output of 7495 registers. The counters are then reset and new set of observation is started.

V.(d) Data Multiplexer:

As described earlier, each data counter-register card has 4 channels each having a maximum length of 10^9 counts. There are basically two ways of connecting

the data counter-register cards. The first way is to connect the serial output of the last card to the serial input of its previous card, and its serial output is connected to the serial input of its previous card and so on. The serial data output of the first card is connected to the serial input of the data display circuit. In such a method of connection the data from the last card have to travel all along the remaining nine cards before it can finally be displayed.

The second method is that within the card the information is shifted serially and the output of each card is multiplexed in a 16-input multiplexer. Figure 9 shows the circuit diagram of the data-multiplexer. This circuit makes use of the reset, C_P, $\div 36$, C_{PP} and 4 Hz pulses derived from control circuits. The reset pulse resets all the F/F's and counters. There are ten D-F/F (7474) used as shift-registers. The clocks of all D-F/F (7474) are connected together. The "divide by 36" input is given to a pair of JK-F/F (7473) connected in cascade. This further divides the "divide by 36" pulse by 4. Thus, after every 144 4 Hz pulses a monoshot (74121-1) is triggered and a pulse is generated which is connected as one of the input to 4-input NAND gate (7440), the other input being from C_{PP}. The output of this NAND gate (7440) is connected to a common clock line of

D-F/F (7474). The output of the monoshot (74121-1) is also connected to a pair of JK-F/F (7473) chip. This is connected in cascade to work as an address counter. This is incremented once when a clock pulse is applied to D-F/F (7474). Each of the Q outputs of the D-F/F (7474) is connected separately as one input to 2-input NAND gate (7400), the other input being 4 Hz pulse, the rate at which right shift is desired. The outputs of these gates (7400) are connected to individual transistor drivers via the inverter drivers (7440). This is essential because each of these has to drive about 36 unit loads of (4 channels) the data-registers (7495). The serial output of each card containing 4 channels is connected to a 16-input multiplexer chip (74150). Once the circuit is reset (by switch S_1 of the control programmer), the C_{PP} pulse transfers the D-input of F/F (7474-1), which is connected to $\bar{Q}$ of JK-F/F (7473-1) to its output (7474-1). Thus, the 4 Hz pulses are now passed on to channels 1 to 4, causing the right shift of the data. These data via the multiplexer are then fed to a display unit. When all the 4-channel data are transferred to the display unit, the monoshot (7412-1) generates a pulse. This pulse, in turn, is applied to all the D-F/F (7474). Since the Q output of the D-F/F (7474-1) is connected

to D-input of next F/F (7474-2) and its Q output is connected to next D-F/F (7474-3) input the Q output of F/F (7474-2) goes to high level. At the same time, the input of F/F (7474-1) was zero, and, therefore, its output (7474-1) goes low. This prevents the 4 Hz pulses from passing on to channels 1 to 4, and ensures the application of 4 Hz pulses to the channels 5-8. Since the monoshot (74121-1) output is also connected to the address counter (7473-5 to 8) the multiplexer now gives data from channels 5 to 8 and so on.

At the end, when all the data are multiplexed and the Q output of F/F (7474-10) goes from high to low, the 4 Hz pulses are stopped using the JK-F/F (7473-2) $\bar{Q}$ output.

V.(e) Data Display Circuit:

The entire data of the 40 channels are displayed on a single nine digit 7-segment LED display (HP 7730 series). The data display system, shown in Figure 10, consists of two rows each of 9 chip registers (7495). The first row is connected in a serial mode i.e. the Q_D output of one is connected to the D_S input of the next and so on. Its mode control is permanently

connected for right shift mode. The outputs of the 1st row of the data display register (7495-1-9) are connected to the input of the 2nd row of the data display register (7495-10-18). The 2nd row is permanently connected for parallel in/parallel out mode. The outputs of the 2nd row of the display registers (7495-10-18) are connected to the 7-segment decoder driver (7446-1-9) and its outputs, in turn, are connected to the 7-segment LED display (HP 7730-1-9) through proper current-limitting resistances.

The data output terminal of the data multiplexer is connected to the serial input of the first row of the data register (7495-1-9). When the 1st channel data of card one is right-shifted, the data enters into the display circuitry. When 36 shifts are over, the 1st channel data is completely transferred to the display circuit. A display or transfer pulse generated by the control circuitry is applied to the 2nd row (7495) and the data of the first row are displayed. At the same time the 4th channel data are now shifted to channel 3-registers. The 3rd channel data are shifted to 2nd and the 2nd channel data are now available on the 1st channel. When the next 36 bit right shifts are completed the 2nd channel data are displayed.

When the 4-channel data are displayed the multiplexer supplies the right shift pulse to the next set of four channels. The output is taken from this new card as the multiplexer address has also now changed.

This continues till all the channels are displayed via the multiplexer. The counts are thus displayed channel by channel and are recorded manually.

V.(f) Control Circuits:

As shown in Figure 11, the control circuits are divided into four sub-circuits, namely (i) channel display and 4 Hz pulse generator, (ii) the control programmer, (iii) the sampling, shift and read pulse generator and (iv) the mode-controller. The details of various controls and their functions are as follows:

(i) Channel display and 4 Hz pulse generator:

The circuit generates the basic 4 Hz pulses required for right-shifting the data available at the registers (7495) of the counter register circuits as soon as parallel transfer pulse (C_{PP}) is applied to the registers. This C_{PP} pulse, which transfers the data from the counters (7490) to the registers (7495),

is generated by the control programmer. A free-running multivibrator is built using a pair of 2-input NAND gates (7400). A trim pot R_1 adjusts the frequency of the multivibrator. This output is then inverted twice again using 2-input NAND gates (7400). These inverters serve as buffers so that the following circuits do not affect the frequency of the multivibrator.

The outputs of the buffers are then connected to the control programmer. Once the "GO" command is issued by the control programmer, the 4 Hz pulses are available to a divide- by-36 counter. Now, each counter/register has a capacity of 9 digits; therefore, to shift the information from one channel to the display circuit needs 36-bit right-shift. This divide-by-36 counter is made using a decade counter (7490-1) chip as divide-by-nine and a JK F/F (7473-1) as divide-by-four. The output of this divide-by-36 counter is available at the output of the F/F (7473-1), which, in turn, is fed to the following two circuits:

1. a channel counter made by cascading two decade counters (7490) followed by BCD to 7-segment decoder drivers (7446). The output of the decoder driver is then connected to two 7-segment LED displays (HP 7730 series) via current limiting resistors to display the channel number.

2. a monoshot through two 2-input NAND gates. This serves as a buffer as well as provides a delay, so that the last bit information is first right-shifted into the display circuitry from the counter-register circuits and then a parallel-in/parallel-out transfer pulse is applied to the display circuits.

(ii) Control programmer:

This generates the initial reset pulse to reset all circuitry except the counter/register cards. When the integration time is over, a 'GO' pulse is given by the switch S_1. A debouncing circuit formed by two 4-input NAND gates (7440) is used to overcome the noise pulses generated due to make and break of the switch contacts. This pulse is given to all the reset points of the various control circuits. The inverted pulse is then used to trigger a monoshot (74121-1) at high-to-low transition. The Q output of the monoshot is then fed to one input of a 2-input NAND gate whose other input is the $\overline{4\ \text{Hz}}$ clock pulse. The output is connected as the clock input to a JK F/F (7473-1). The J-input is connected to logical 1 permanently. Normally the clock input is at logical 1, but as soon as both the 4 Hz clock and the Q output of the monoshot (74121-1) become logical 1, the clock

input goes low and the JK F/F is triggered. The output of this JK F/F is again connected as one of the inputs of a 2-input NAND gate, the other input being the 4 Hz clock. The output of the NAND gate is inverted and used as a clock to the three JK F/F (7473-2, 3, 4). The J-input of the first F/F (7473-2) is connected to logical 1. Thus, at each high-to-low transition of this clock the logical 1 will right-shift to the output of the F/F's. This arrangement is made so that once the information is transferred, the correct right-shift should start after a time delay. Once the logical 1 output is available at Q of the JK F/F (7473-4), this is connected to a 2-input NAND gate along with the 4 Hz pulses. This pulse is then used to drive the channel counter and other controls.

The output of the JK F/F (7473-3) is also connected to a monoshot (74121-2) connected in low-to-high transition triggering mode. When the logical 1 of the J-input of the JK F/F (7473-2) appears at the input of the monoshot (74121-2), it is triggered to generate a pulse which is then fed to the mode controller. This ensures that the right-shift of data will take place only after the mode controller has operated and the data are available for right-shifting to the data multiplexer.

(iii) Sampling, shifting and read pulse generator:

This circuit generates the various pulses required for sampling, shifting and reading the autocorrelator data. The sampling interval should be accurate and, therefore, a quartz crystal oscillator is built using two pairs of a 2-input NAND gate (7400). The output of this oscillator is fed to a decade counter (7490) connected in divide-by-five mode to give a basic 200 kHz sampling frequency. The output is then connected to a monoshot (74121-1) connected in high-to-low transition triggering mode. The output $\bar{Q}$ of this monoshot is connected to an inverter driver (7440) whose output is then used as a sampling pulse (f_s). This output is also connected to another monoshot (74121-2) whose output is used as a shift pulse (T_s) after inverter drivers (7440). The output of the monoshot (74121-2) is also connected to another monoshot (74121-3) whose output is used as a read pulse (T_R) after driver inverters.

(iv) Mode Generator:

This circuit generates a sequence of operation for controlling the operation of the correlator and counter register cards. The sequence of operation is as follows: First it sets the mode for the parallel

transfer of the data from the data counter of each channel to the data register. Then it generates a pulse for actual transfer after which it generates reset signals for the data counters and correlator shift-registers. After this, it generates the mode for right-shift of the data. When a 'GO' pulse is given by the switch S_1 of the control programmer, it resets all the F/F (7474 & 7473). When a pulse appears at S_D of 7474 from the control programmer, its Q output goes high which, in turn, triggers a monoshot (74121-1). This, in turn, sets the parallel-in/parallel-out mode for the data shift register. The Q output pulse (C_{PP}) of this monoshot through a driver is used to transfer the parallel information available at the output of the data counter (7490) to the output of the data registers (7495). The $\bar{Q}$ output of the monoshot (74121-1) is connected to monoshot (74121-2) to trigger in low-to-high transition mode. The complementary outputs Q & $\bar{Q}$ of the monoshot (74121-2) are connected to two monoshots (74121-3 and 4) and the $\bar{Q}$ output is used as a reset pulse for the correlator shift register. The monoshot (74121-4) is connected in high-to-low transition triggering mode and used to reset all the data counters. The Q output of the monoshot (74121-3) is connected as clock to JK F/F (7473). Initially at reset the $\bar{Q}$

output of this F/F is at logical 1. This is connected to mode control and, therefore, when this F/F (7473) is clocked, the output falls to 0 and thus the data shift registers are now ready for right-shifting the data.

Figure 12 shows the various waveforms in a sequence used for the operation and control of the entire correlator system.

V.(g) Computation of ACF and Power Spectrum:

The counts recorded are processed in a computer for obtaining autocorrelation function and power spectrum. Following Weinreb (1963), it is seen that the autocorrelation function of the noise signal is given in terms of the contents of the counters as

$$R'(\tau) = \frac{2C_n - C_1}{C_1}, \quad n = 1 \text{ to } 40 \qquad \ldots (16)$$

The autocorrelation functions obtained from these formulae are then corrected using the Van Vleck correction of eqn.(12).

The corrected autocorrelation functions are then used to derive the power spectrum. A cosine weighting function was chosen. Thus,

$$w(n\,\Delta T) = 0.5 + 0.5 \cos \frac{\pi n}{N} \qquad \ldots (17)$$

where $|n| < N$

The power density

$$P'(f) = 2\,\Delta T \left[R(1)\, w(1) + \sum_{n=2}^{40} R(n)\, w(n\,\Delta T) \times \cos(2\pi\, n.\Delta T.f) \right] \qquad \ldots (18)$$

A noise source was used as the noise input to the receiver. Observations were taken with different integration times. Figures 13(a) and 13(b) show plots of normalized ACF for observation sets for 7 and 50 minutes of integration times respectively. The corresponding normalized power spectra are shown in Figure 14(a) and 14(b). It can be seen that the variations of noise power in the band 4-40 kHz (over which the filter response is flat) are within $\pm$ 0.8 dB in the case of the 7 minutes sample and within $\pm$ 0.3 dB in the case

of the 50 minutes sample. RF spectral line observations will be most accurate if confined to the flat response of the system.

Acknowledgements

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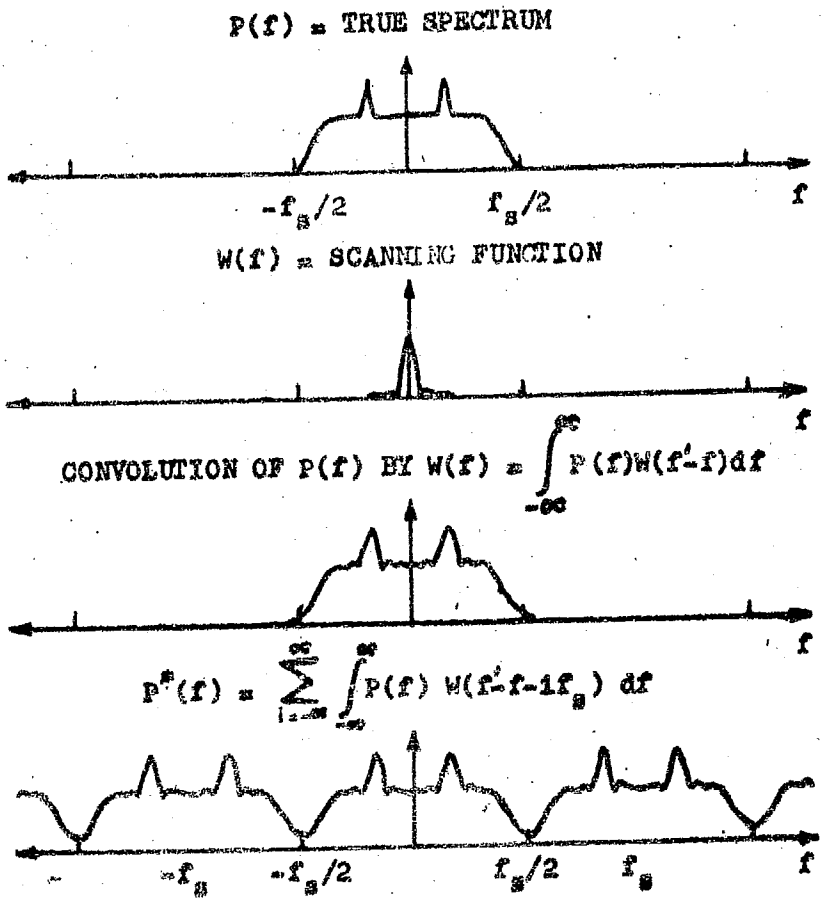
Pointon, L., J. Phys. E., Sci. Instrum., Vol.10, No.8, pp.753-848, 1977.

Van Vleck, J.H. and Middleton, D., Proc. IEEE, Vol.54-A pp.2-19, 1966.

Weinreb, S., MIT, Technical Rep. No.412, Department of Electronic Engineering, 1963.

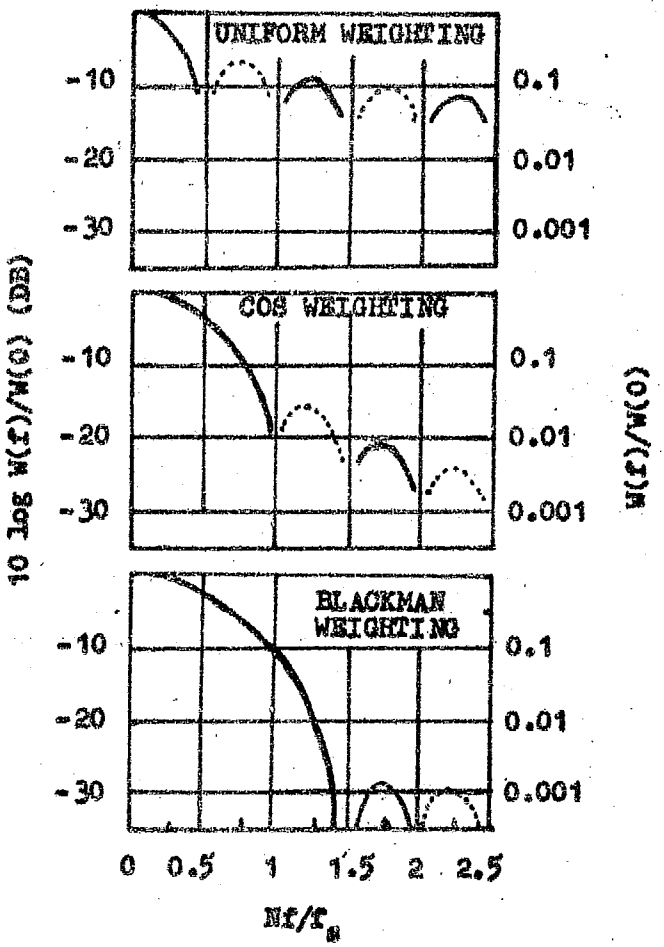
List of I.C's. used in the correlator and their manufacturers

IC specification		Manufacturer
Linear IC No:		
1)	741	1) M/s. Fairchild Semiconductors 313 Fairchild Drive Mountain View, California USA.
2)	710	
Digital IC No:		
1)	SN 7400	2) M/s. National Semiconductors 808 Fuerstenfeldbruk Industriestrassee 10 West Germany.
2)	SN 7402	
3)	SN 7440	
4)	SN 7446	
5)	SN 7473	3) M/s. Texas Instruments Inc. Attleboro Massachusetts 02103, USA.
6)	SN 7474	
7)	SN 7490	
8)	SN 7495	
9)	SN 74121	
10)	SN 74150	
11)	HP 7730	... M/s. Hewlett-Packard 1507 Page Mill Road Palo Alto California, USA.



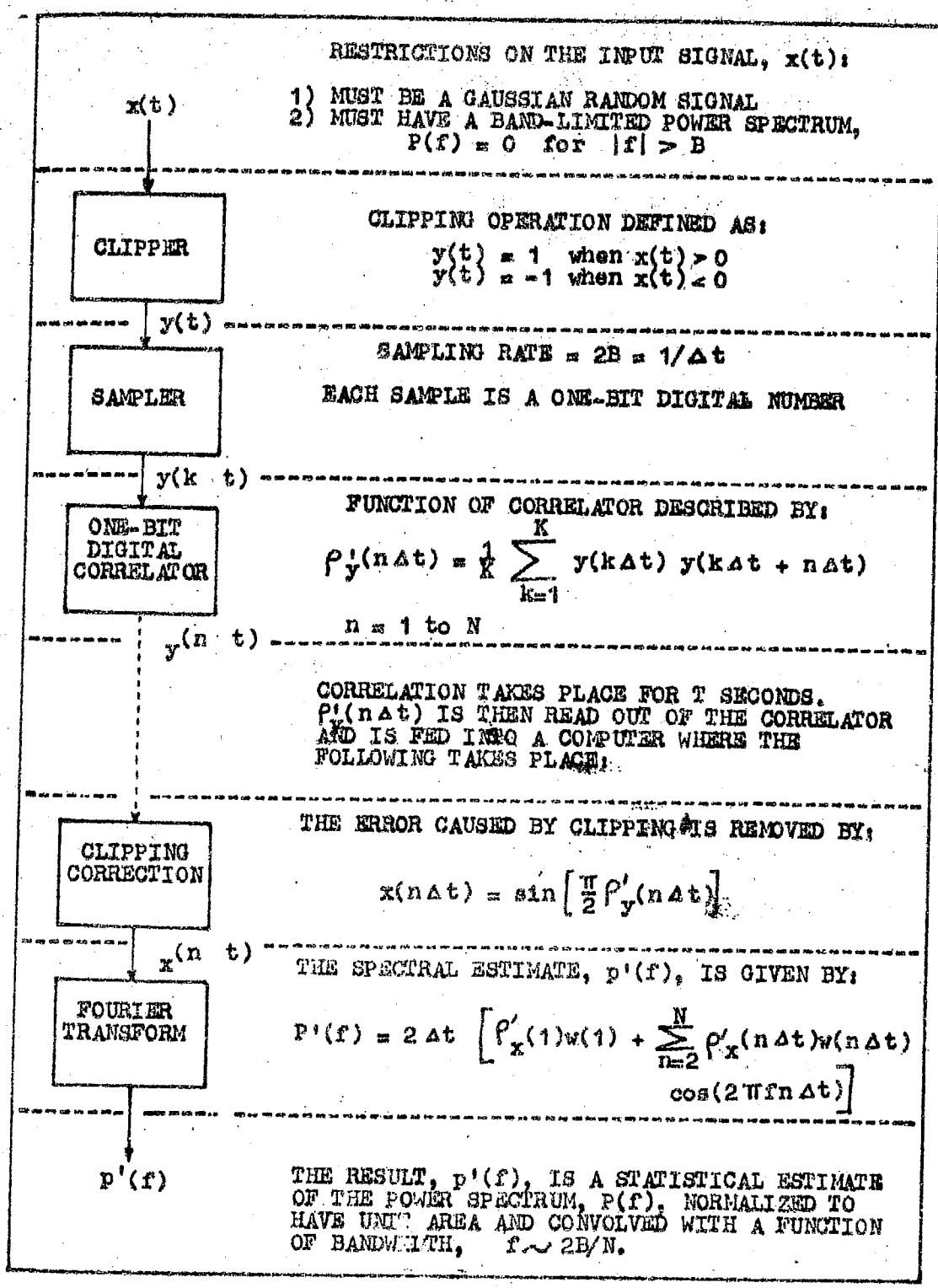
Effect of sampling and truncation of the autocorrelation function. The quantity $P^*(f)$ is the mean of a spectral measurement performed with an autocorrelation system.

Fig. 1



Three scanning functions that result from the uniform and cosine weighting functions. The broken lines indicate that W(f) is negative.

Fig. 2



The 1-bit autocorrelation method of spectral analysis.

Fig. 3

SCHEMATIC OF 1-BIT DIGITAL AUTOCORRELATOR SYSTEM

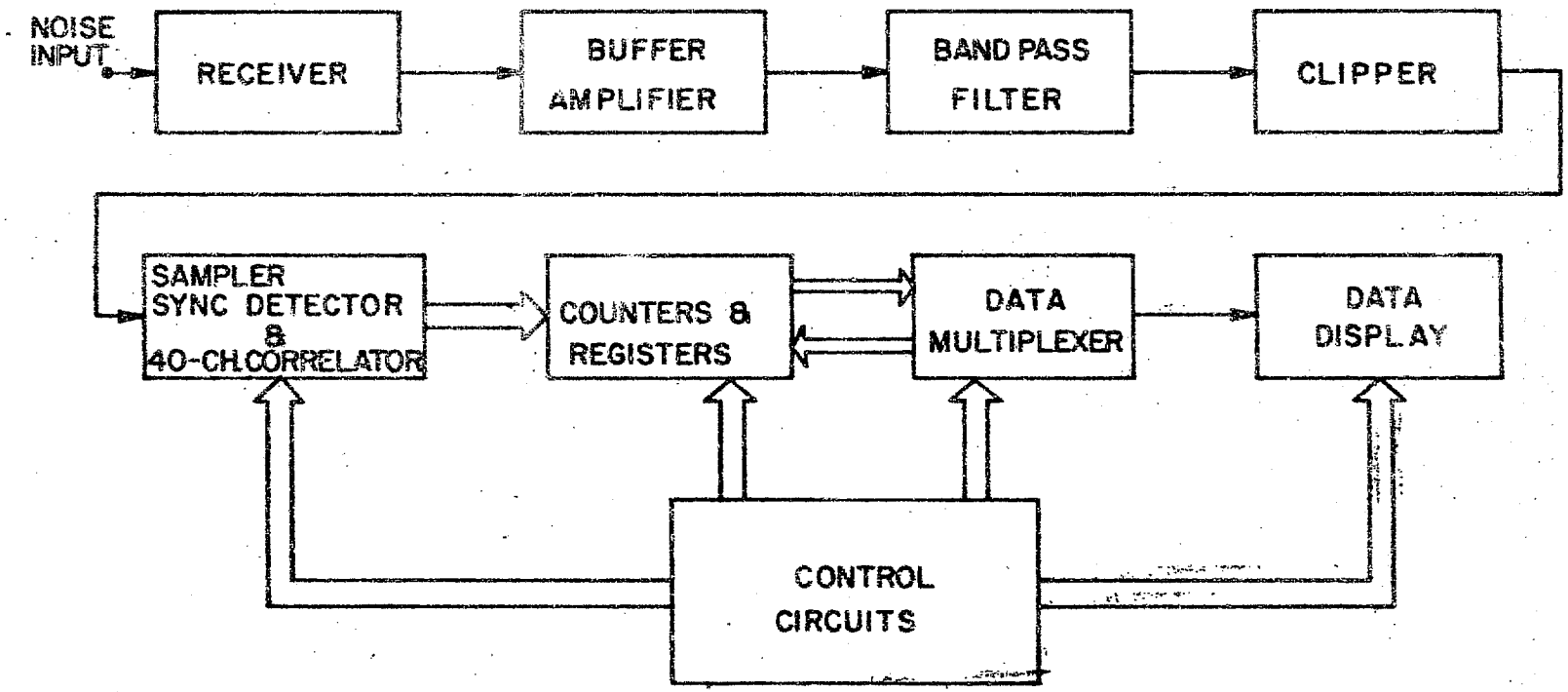


Fig. 4

BUFFER AMP FILTER AND CLIPPER

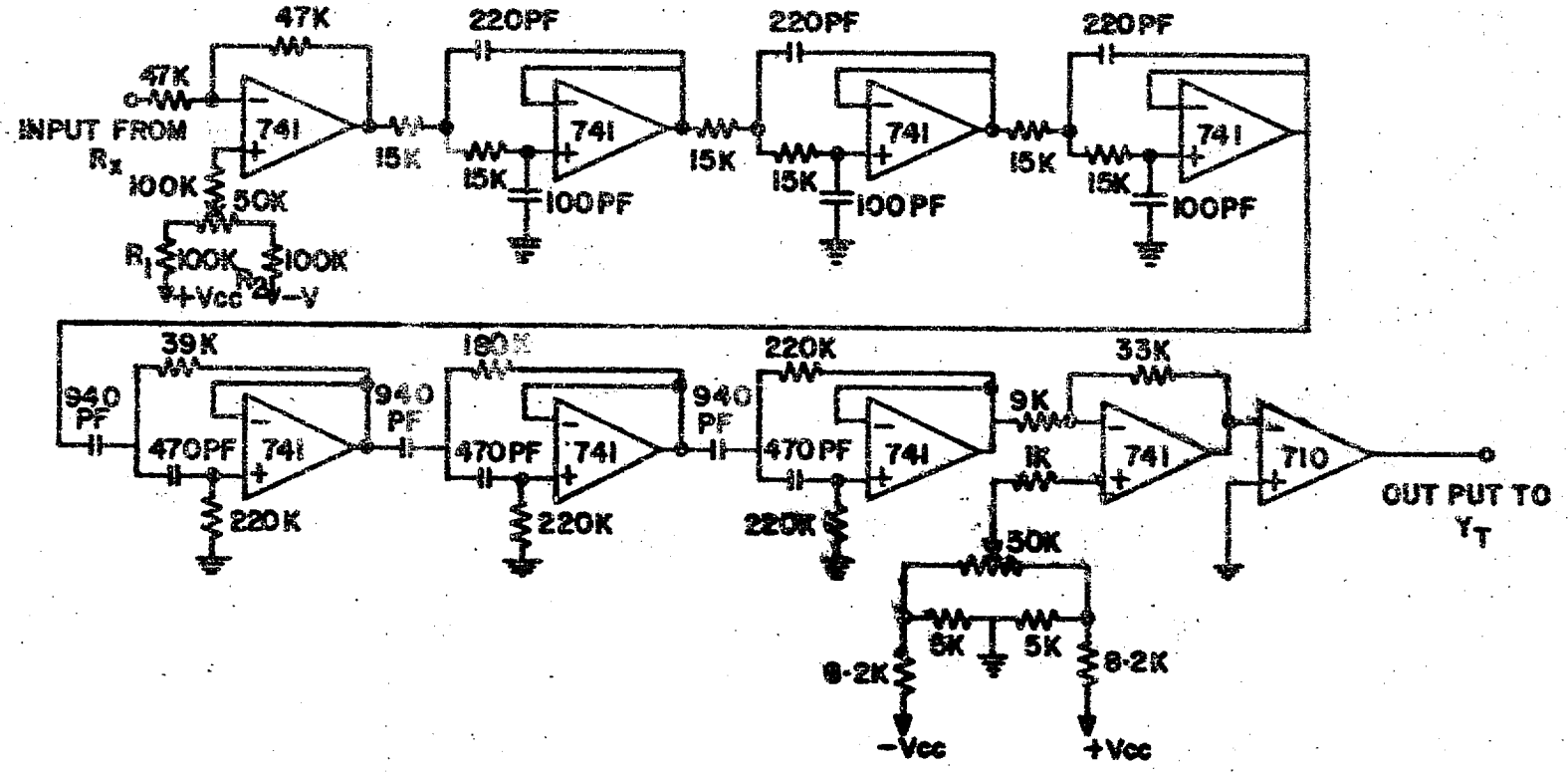


Fig. 5

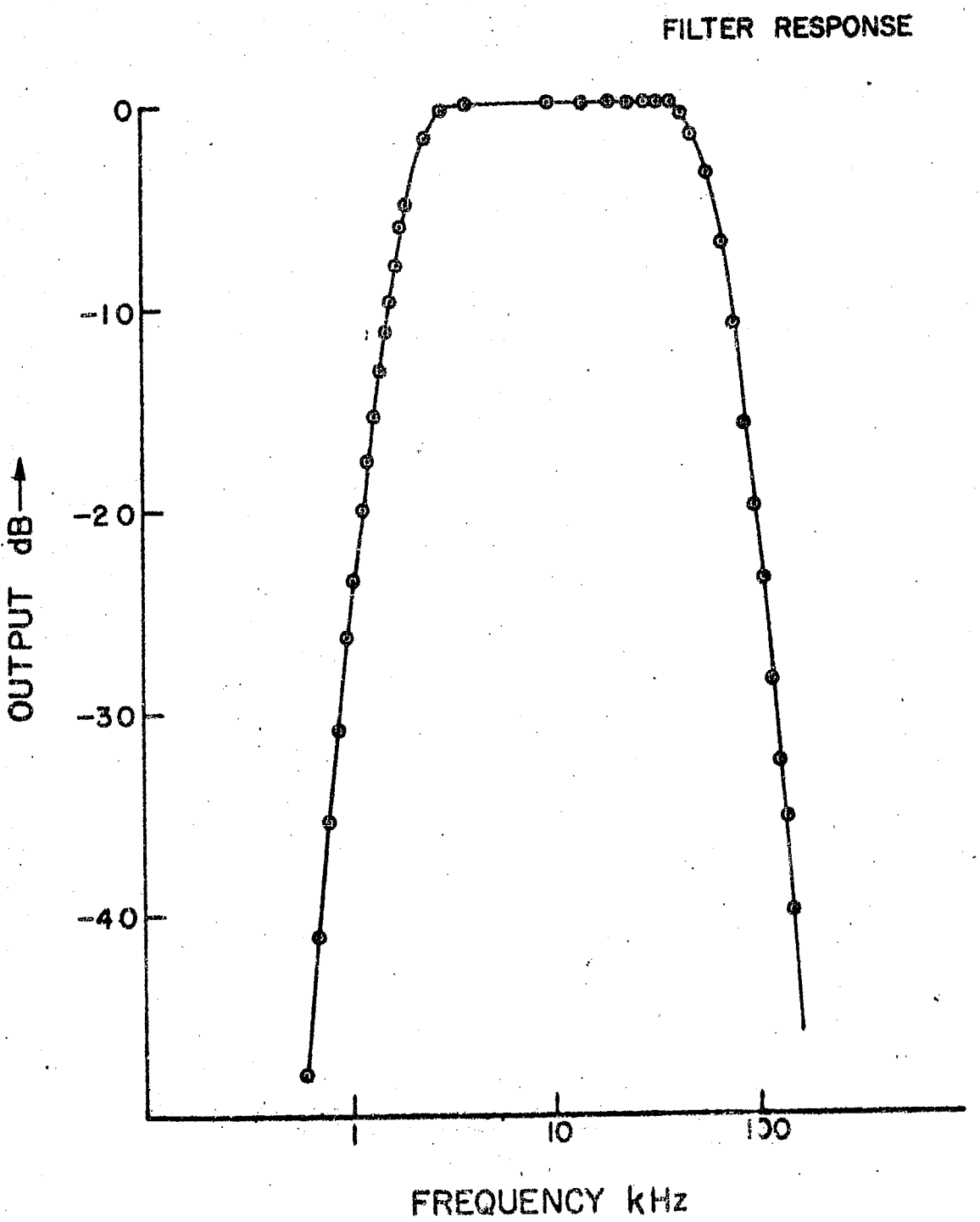
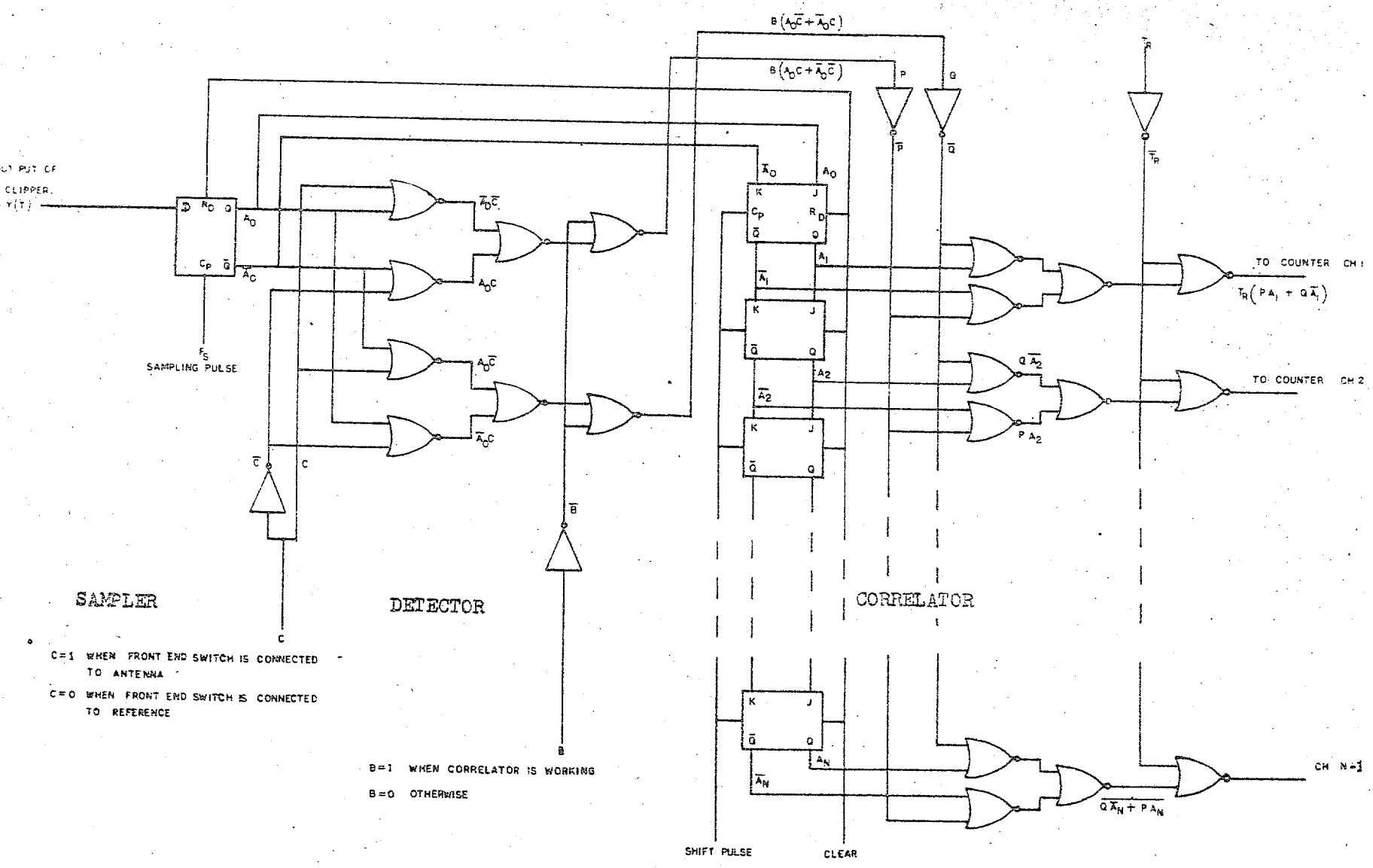


Fig. 6

SAMPLER, SYNCHRONOUS DETECTOR AND CORRELATOR



ONE CHANNEL OF COUNTER REGISTER

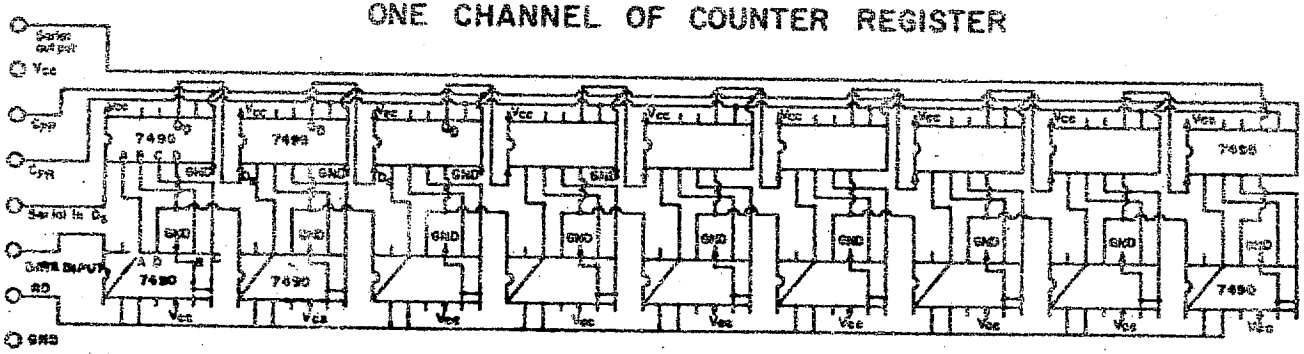


Fig. 8

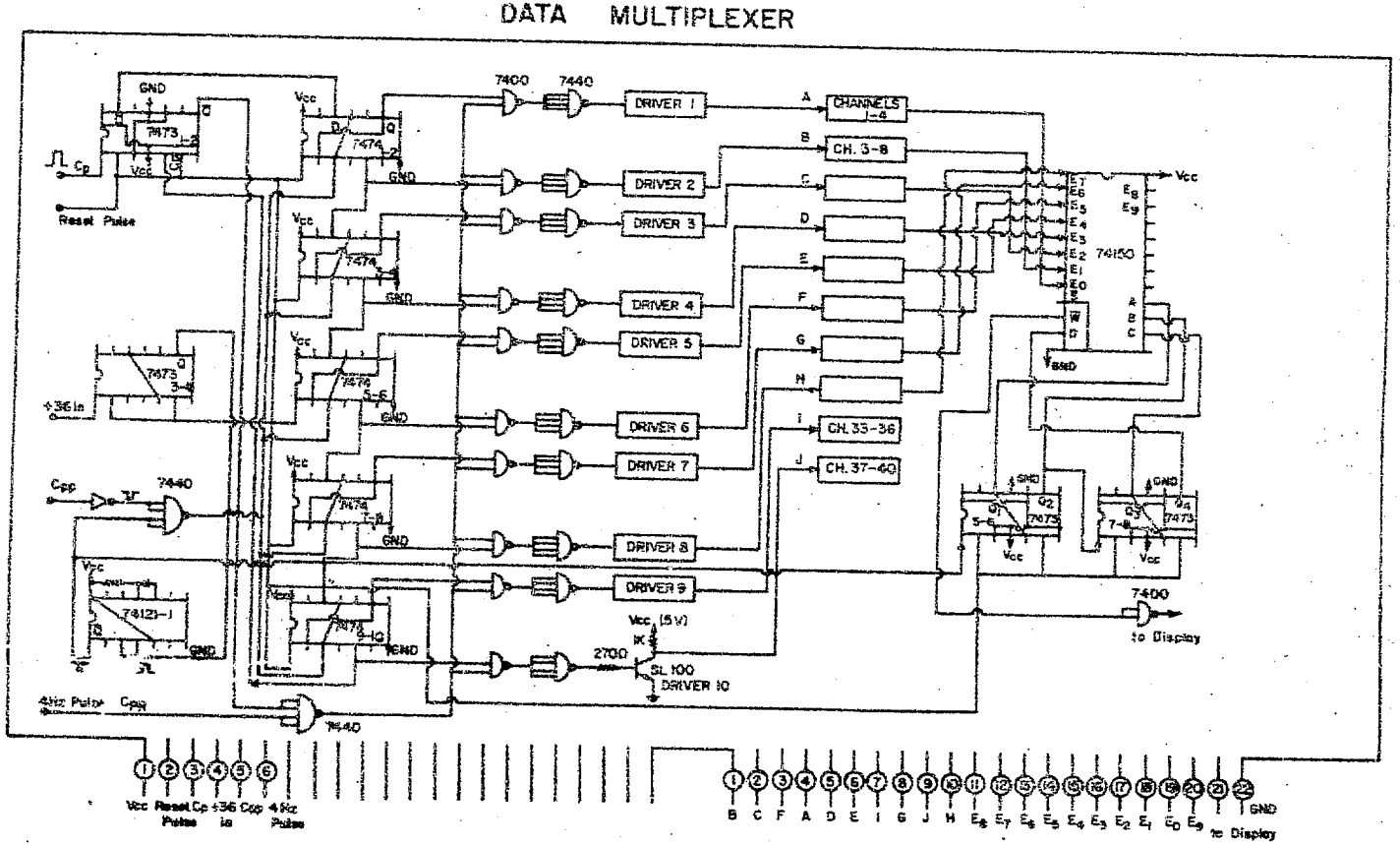

DATA MULTIPLEXER
GND
Vcc
7473
7474
7400
7440
DRIVER 1
DRIVER 2
DRIVER 3
DRIVER 4
DRIVER 5
DRIVER 6
DRIVER 7
DRIVER 8
DRIVER 9
DRIVER 10
CHANNELS 1-4
CH. 5-8
CH. 33-36
CH. 37-40
Reset Pulse
÷36 In
74121-1
4Mz Pulse
2700
SL 100
74150
to Display
Vcc Reset Pulse
Cp
÷36 In
Cpp
4 Mz Pulse
B C F A D E I G J H
GND
to Display

Fig. 9

DATA DISPLAY CIRCUIT

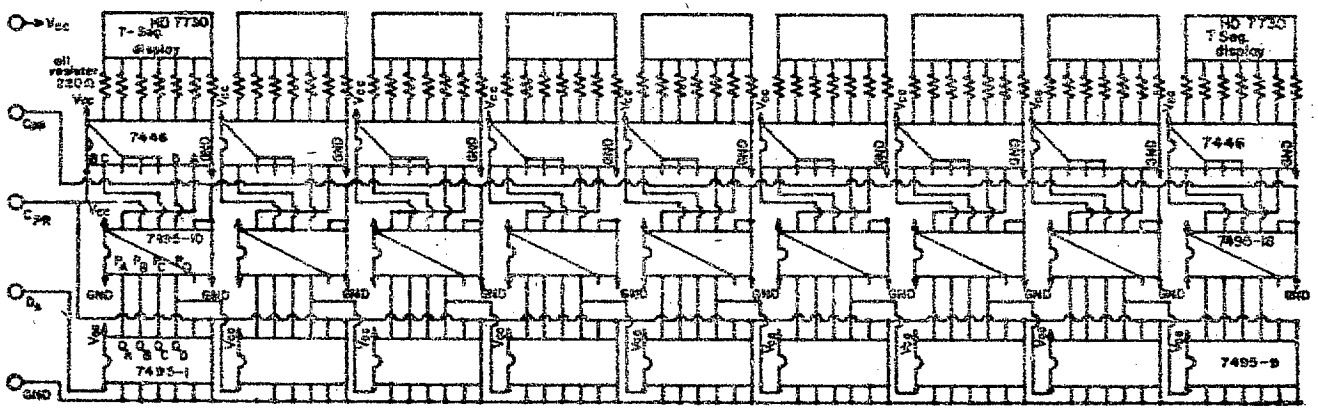
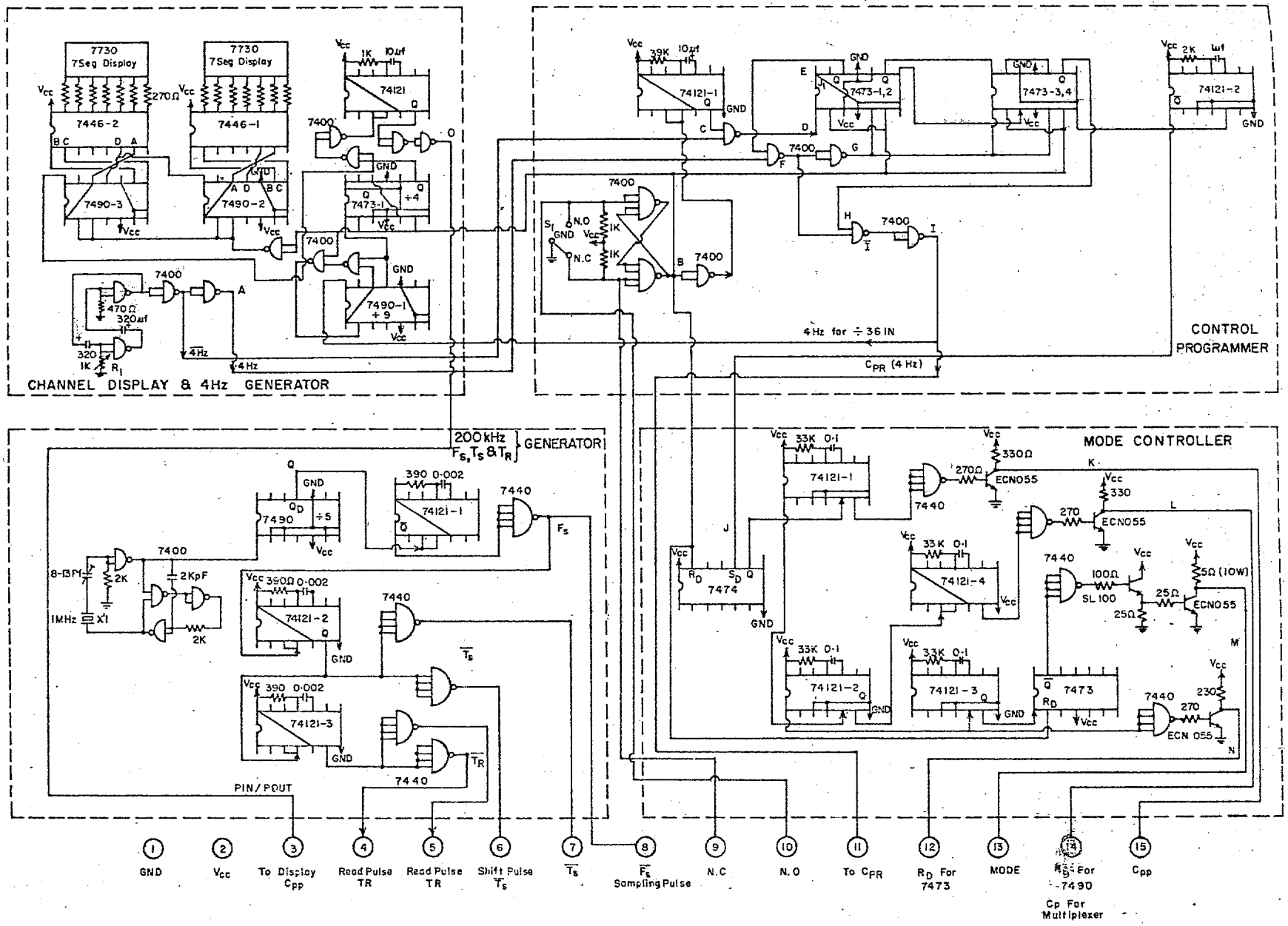
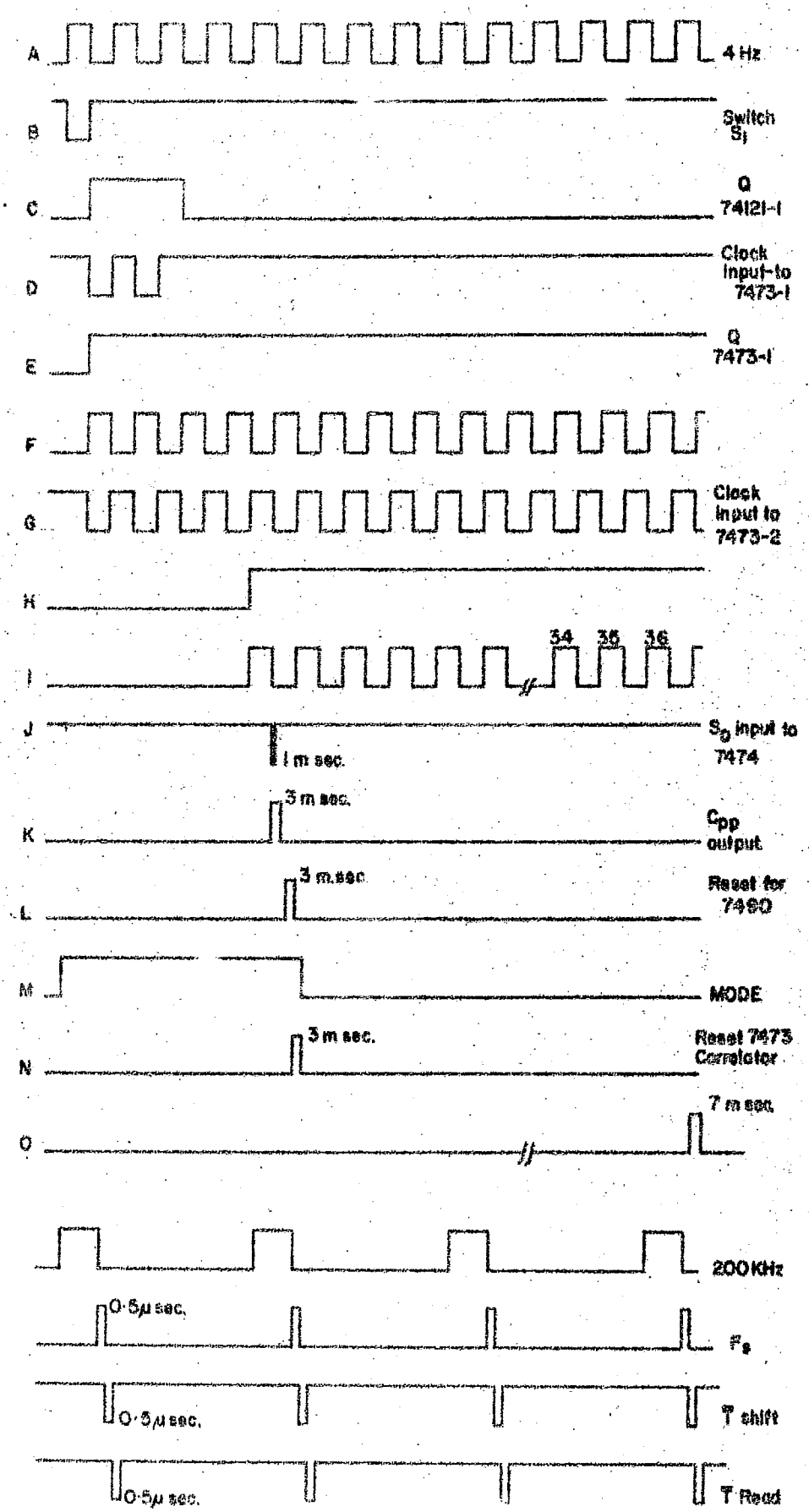


Fig. 10


7730
7Seg Display
7446-2
7446-1
7490-3
7490-2
7490-1
÷9
7473-1
÷4
74121
7400
7473-1,2
7473-3,4
74121-1
74121-2
CHANNEL DISPLAY & 4Hz GENERATOR
CONTROL PROGRAMMER
4Hz for ÷36 IN
CPR (4Hz)
200kHz
Fs, Ts & TR
GENERATOR
7490
÷5
74121-3
74121-4
7474
7440
MODE CONTROLLER
ECN055
SL100
PIN/POUT
1 GND
2 Vcc
3 To Display Cpp
4 Read Pulse TR
5 Read Pulse TR
6 Shift Pulse Ts
7 Ts
8 Fs Sampling Pulse
9 N.C
10 N.O
11 To CPR
12 RD For 7473
13 MODE
14 RD For 7490 Cp For Multiplexer
15 Cpp

CONTROL WAVEFORMS



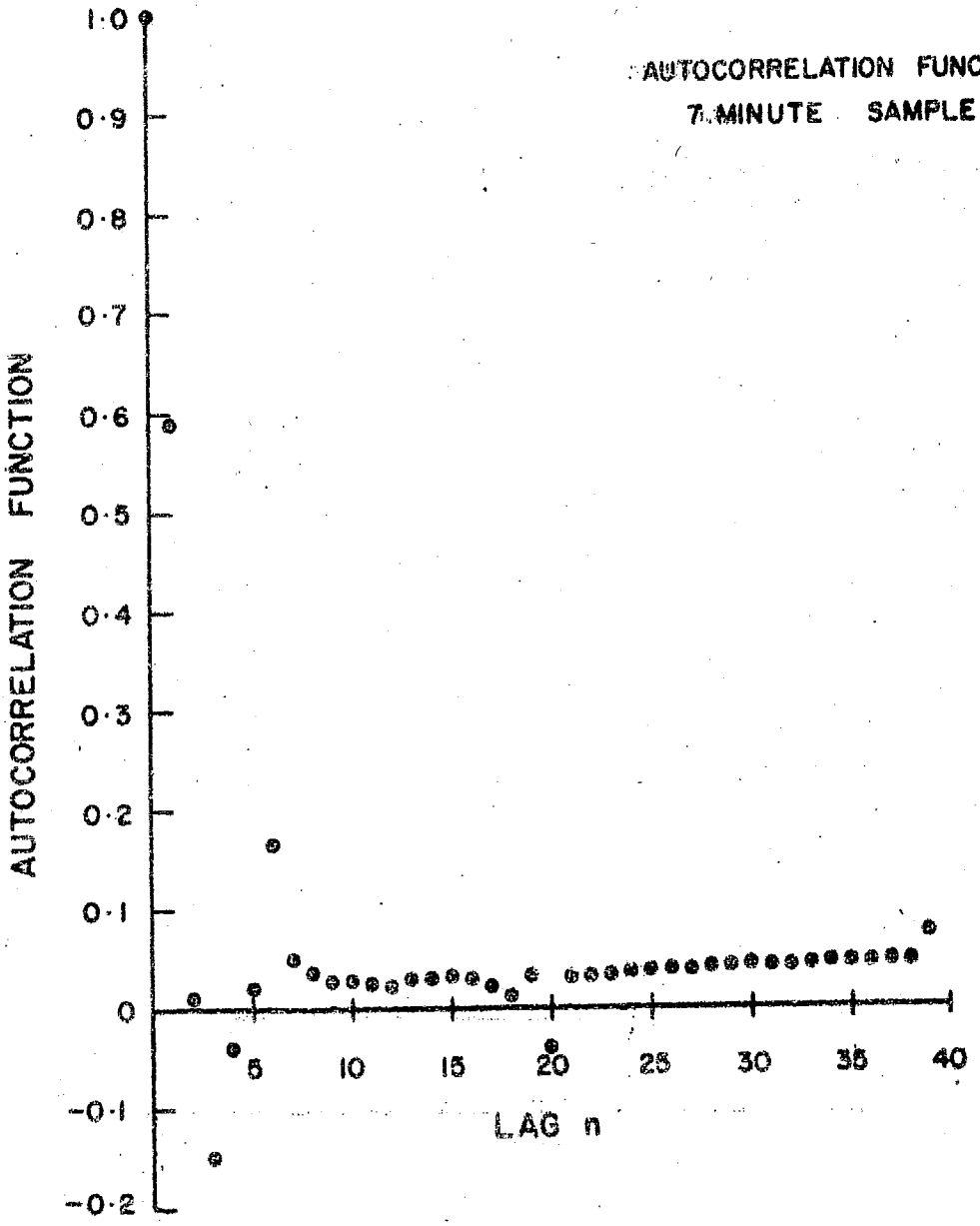

AUTOCORRELATION FUNCTION
7 MINUTE SAMPLE
AUTOCORRELATION FUNCTION
1·0
0·9
0·8
0·7
0·6
0·5
0·4
0·3
0·2
0·1
0
-0·1
-0·2
5
10
15
20
25
30
35
40
LAG n

Fig. 13(a)

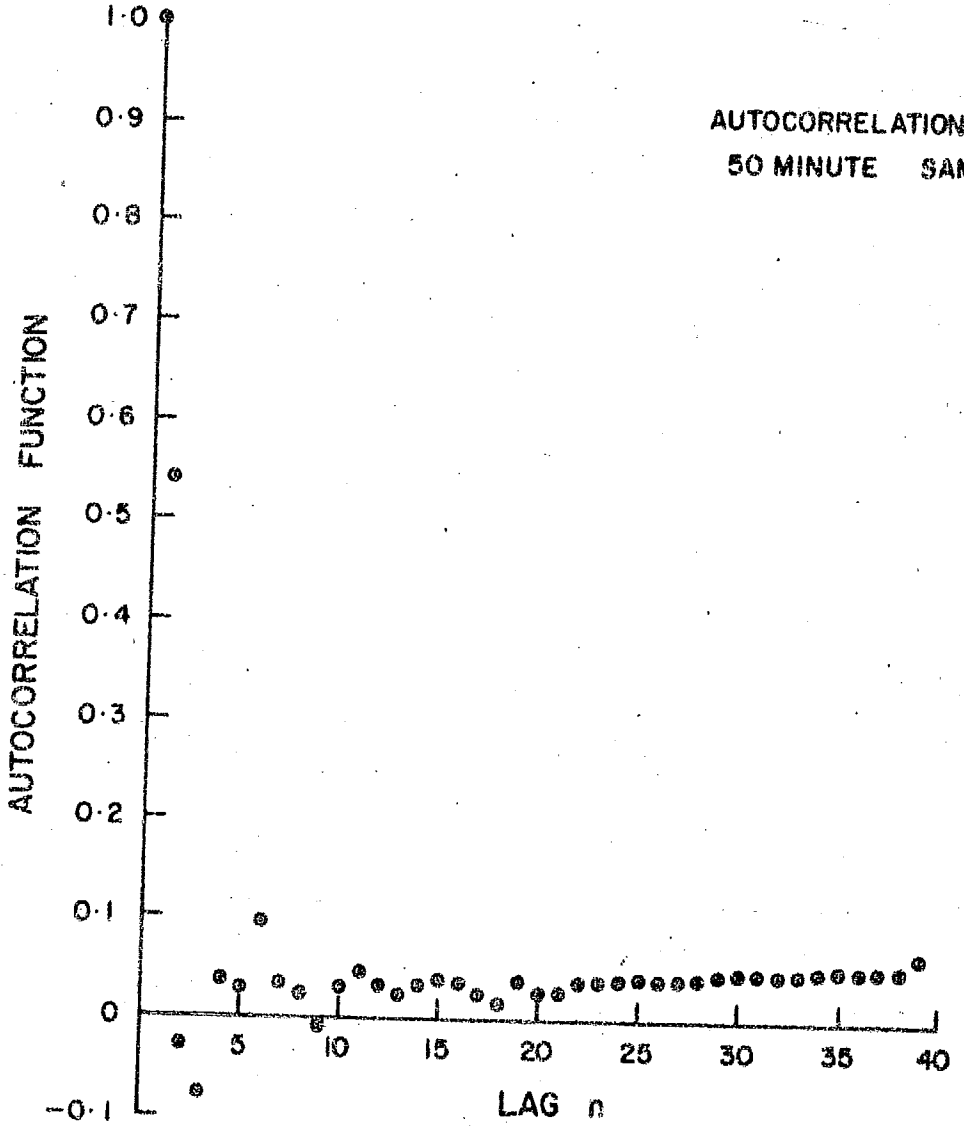

AUTOCORRELATION FUNCTION
50 MINUTE SAMPLE
AUTOCORRELATION FUNCTION
1·0
0·9
0·8
0·7
0·6
0·5
0·4
0·3
0·2
0·1
0
-0·1
5
10
15
20
25
30
35
40
LAG n

Fig. 13(b)

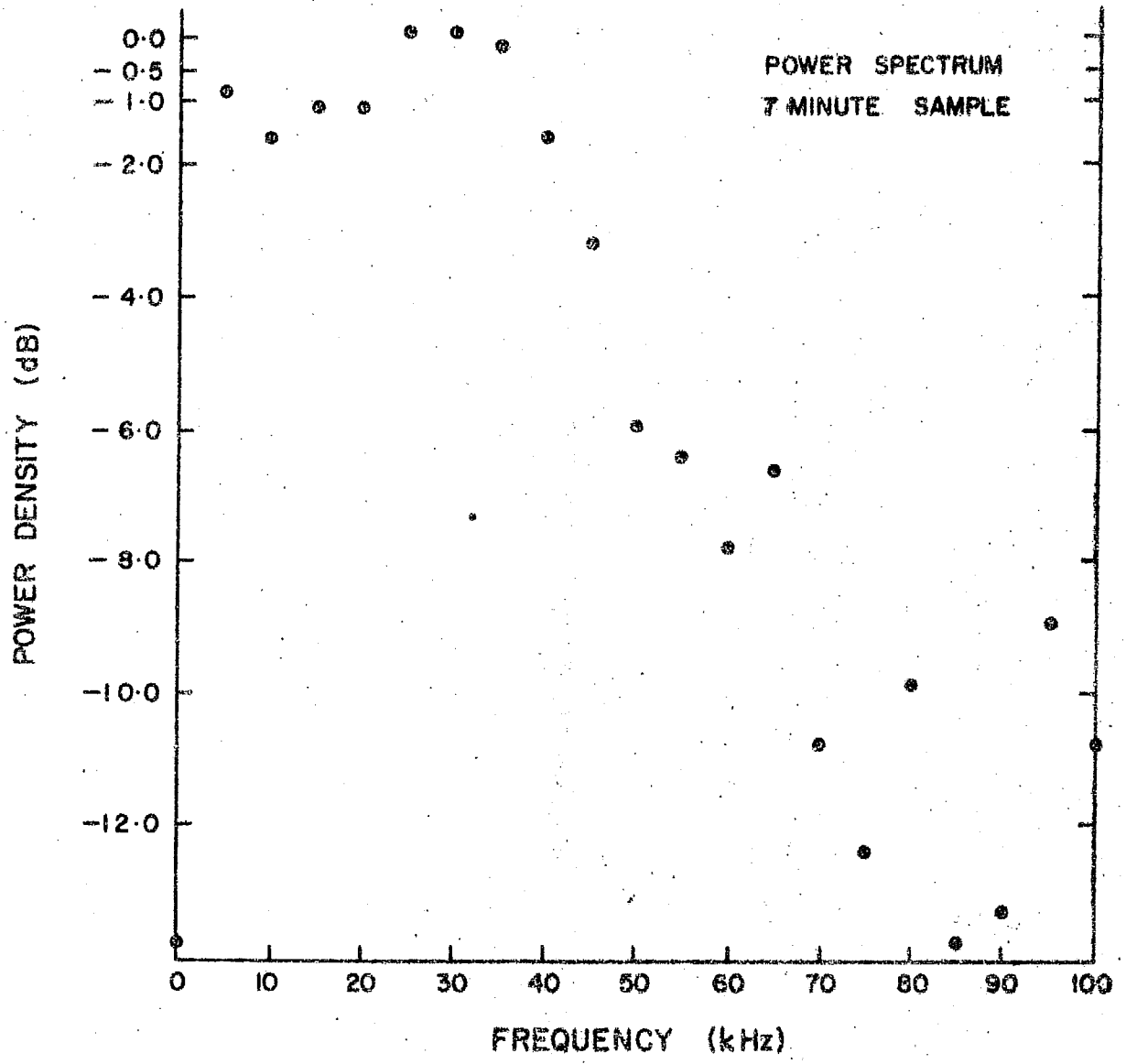
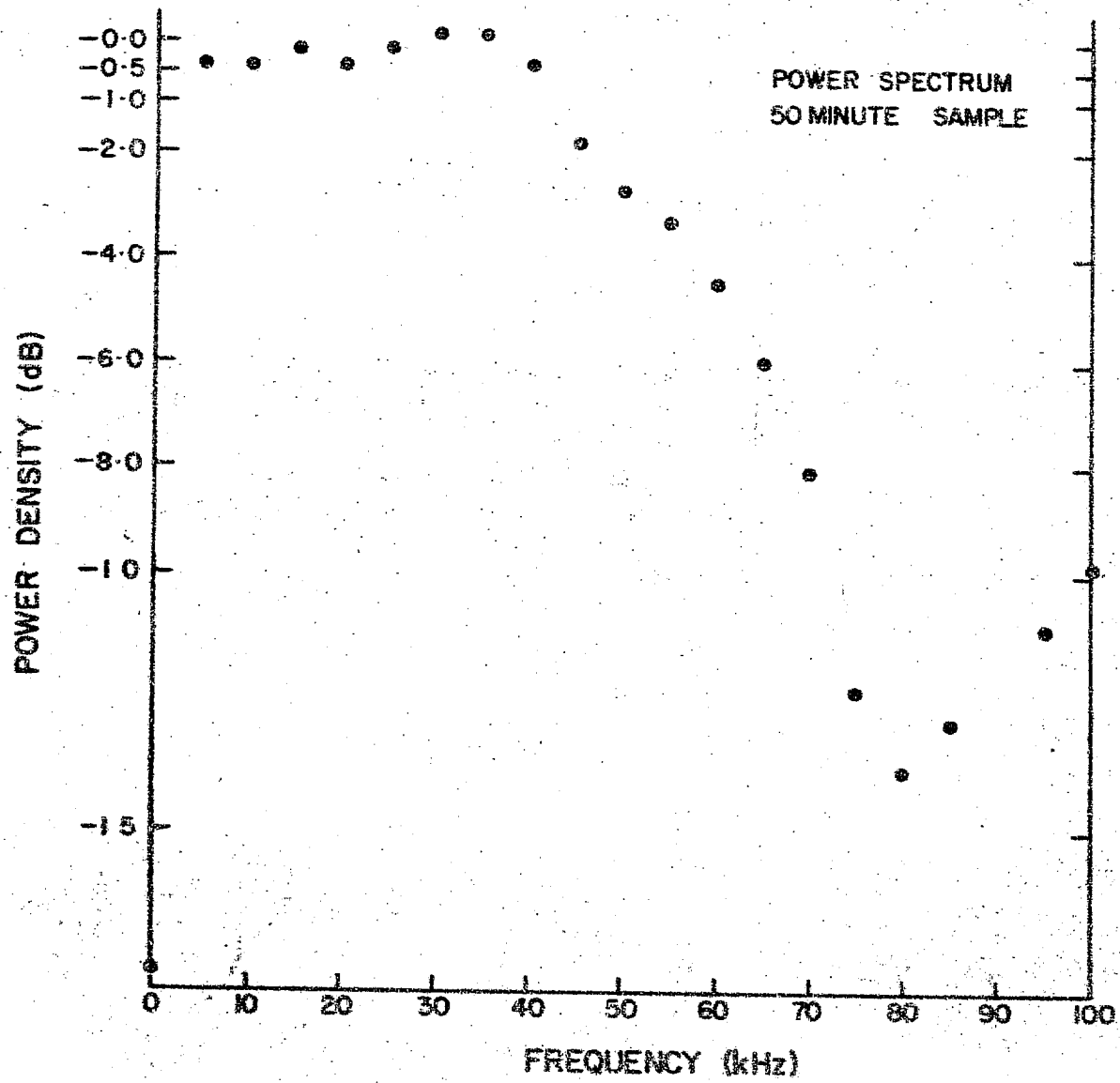

POWER SPECTRUM
7 MINUTE SAMPLE
POWER DENSITY (dB)
0·0
- 0·5
- 1·0
- 2·0
- 4·0
- 6·0
- 8·0
-10·0
-12·0
0
10
20
30
40
50
60
70
80
90
100
FREQUENCY (kHz)

Fig. 14(a)


POWER SPECTRUM
50 MINUTE SAMPLE
POWER DENSITY (dB)
-0·0
-0·5
-1·0
-2·0
-4·0
-6·0
-8·0
-10
-15
0
10
20
30
40
50
60
70
80
90
100
FREQUENCY (kHz)