A novel approach to radiation detector readout system for space borne instrumentation

A Thesis submitted by

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(Enrolment No. 17PH21**)**

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Under the guidance of

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CERTIFICATE

This is to certify that the content of this thesis titled “A novel approach to radiation detector readout system for space borne instrumentation” is the original work of Mr. Arpit Patel (17PH21) carried out under my supervision. I further certify with best of my knowledge that the work has not been submitted either partly or fully to any other university or body – in quest of a degree, diploma and/or any other kind of academic award.

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CANDIDATE'S DECLARATION

The work described in this thesis entitled "A novel approach to radiation detector readout system for space borne instrumentation" is carried out solely by me under the guidance of Prof. Himanshu Mazumdar, except for those colleagues and other workers referred/acknowledged in the text. I hereby declare that no part of this thesis has been previously submitted to this or any other university as part of the requirement for a higher degree.

Arpit Patel Date:

(17PH21) Place: Nadiad

DEDICATION

To my caring Mother & Father,

loving wife & cute daughter

and

To all my well wishers

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Words fail us to express my gratitude to my guide, **Prof. Himanshu Mazumdar**. I owe my deep sense of appreciation to him for his constant vigilance with the right amount of freedom, not only as a guide but as a guardian too. His efforts and encouragement will never be forgotten.

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ABSTRACT

This thesis focuses on the new signal readout technique from the radiation detector which can be used for future space missions ensuring to have better in terms of resolution, mass, and power compared to available signal readout techniques. In radiation detector signal processing usually, the charge-sensitive pre-amplifier converts the small charge signal coming from the semiconductor-based detector into voltage form and then the signal is further amplified to measure the energy of the incoming radiation. The voltage pulse from a charge-sensitive pre-amplifier (CSPA) is amplified with the use of a shaping amplifier which reduces the signal bandwidth. To have better energy resolution, precise measurement of the peak amplitude of shaping amplifier output is required. For multiple detector systems, currently available peak height analysis (PHA) methods are quite power consuming and difficult to implement in Field Programmable Gate Arrays (FPGA). In this direction, the research is carried out and a technique is developed that uses low sampling analog to digital converter and interpolation technique to precisely measure the peak of the analog pulse. The main topics of interest are, the development of a novel signal readout technique using the interpolation method, the selection of appropriate interpolation technique and performance comparison with existing readout techniques. The silicon drift detector (SDD) based soft X-ray spectrometer instrument is developed and used to compare the PHA techniques. Chapter 1 gives a brief objective of the research goal, and chapter 2 includes the literature review and background of various radiation detectors and their readout techniques. Chapter 3 discuss the design details of various pulse height analysis methods. The methods are implemented on hardware and various parameters are obtained to compare with the proposed method. Chapter 4 discusses the implementation of a new method with the use of the interpolation technique and contains results for the proposed method and a comparison with other methods. The energy resolution is considered the main performance criteria. To select the most suitable interpolation method for the proposed method, various interpolation methods are compared by implementing them on hardware. Chapter 5 gives a summary of the research work and future plans.

TABLE OF CONTENTS

LIST OF FIGURES

LIST OF TABLES

LIST OF ABBREVIATIONS

Abbreviation	Full form
ADC	Analog to Digital Converter
ALICE	A Large Ion Collider Experiment
AM	Amplitude Modulation
ASIC	Application Specific Integrated Circuit
BGO	Bismuth Germanate
CCE	Charge Collection Efficiency
CdTe	Cadmium Telluride
CdZnTe	Cadmium Zinc Telluride
CME	Coronal Mass Ejections
CRO	Cathode ray oscilloscope
Csl (Tl)	Cesium Iodide (Thallium)
CSPA	Charge Sensitive Pre-Amplifier
DAC	Digital to Analog converter
DSSD	Double Sided Silicon strip Detector
DPP	Digital Pulse Processing
E	Incident Photon Energy
ELF	Extremely Low Frequency
ESA	European Space Agency
eV	electron Volts
FEE	Front-End Electronics
FM	Frequency Modulation
FPGA	Field Programmable Gate Array

FWHM	Full Width Half Maximum
Ge	Germanium
GCR	Galactic Cosmic Rays
GM	Geiger-Muller
GRS	Gamma Ray Spectrometer
KV	Kilo Volts
KeV	Kilo electron Volts
$LaBr_3$	Lanthanum Bromide (cerium)
LAD	Large Area silicon Detectors
LN_2	Liquid Nitrogen
LOFT	Large Observatory for X-ray Timing
MAD	Mean Absolute error
MCA	Multi-Channel Analyzer
MER	Mars Exploration Rover
MOS	Metal Oxide Semiconductor
MSE	Mean square error
NaI (Tl)	Sodium Iodide (Thallium)
PHA	Pulse Height Analysis
PMT	Photomultiplier Tube
PWM	Pulse width modulation
RE	Relative error
SDD	Silicon Drift Detector
Si	Silicon
Si (Li)	Silicon Lithium
SPE	Solar Particle Events

SiPM	Silicon Photomultiplier
SSD	Silicon Strip Detector
UV	Ultra Violate
XRF	X-Ray Fluorescence
Z	Atomic Number

C H A P T E R – 1

1 INTRODUCTION

Developing a space-borne instrument is a challenging task, as the instrument has to survive very hostile space environment. The cost of launch is determined by the payload's weight. In that regard, it is necessary to have the least amount of mass, power, and size instrument onboard in order to complete tasks with the best possible performance. Any instrument onboard a spacecraft is likely to be exposed to harsh radiation, extreme temperature swings, and high vacuum conditions. The instrument should also be able to withstand launch vehicle vibration. At various levels of the instrument design, such as selecting components/devices with space qualification, desired radiation testing, design, and packaging of the instrument, care must be taken for the above-mentioned aspects. Instruments built with Commercial-Off-The-Shelf (COTS) components will not withstand the harsh space environment and satellite launch loads. For these reasons, "space instruments are custom-designed one-of-a-kind instruments, and the construction of such a one-of-a-kind instrument is dependent on the mission and the instrument configuration required for the scientific application".

Radiation detectors are widely used for measuring radiation emitted by various space objects in the X-ray, Gamma-ray, or high-energy particle regions of the spectrum. Ionizing and non-ionizing radiation are the two main types of radiation. Non-ionizing radiation from ultraviolet is less energetic. The atoms and molecules that interact with UV light particles receive energy from them but do remove their electrons. There are several types of ionizing radiation, including galactic cosmic radiation, trapped radiation, and solar energetic particles. The Galactic cosmic radiation is emitted as massive clouds of high-energy charged particles believed to be emitted by supernovas. The earth’s magnetic field is strong enough to catch the charge particles and, in the field, these particles travel in a spiral pattern. Solar particle events involve the Sun releasing energetic solar particles. Sudden, powerful storms may develop as a result of this.

Radiation detector instruments usually have a similar kind of readout method which contains CSPA, Shaping amplifier and pulse height analyzer. A suitable pulse

height analyzer is required based on instrument specifications such as energy resolution, count rate, mass, etc.

1.1 Research objectives and result

Currently, astronomers are attempting to answer fundamental questions about the motion of matter orbiting close to a black hole's event horizon, the state of matter in neutron stars, and other solar studies. High-resolution Gamma-ray and X-ray timing will be used to achieve these scientific objectives, which entails monitoring X-ray photometric time series and energy spectra from a range of astrophysical compact objects (Galactic black holes, neutron stars, and extra-Galactic black holes in AGNs). For these tests, wide imaging capacity and superior spectral resolution are required. The Large Area Silicon Detectors (LAD) of size 108.5 mm x 70 mm, which uses the same technology and are based on the heritage of the detectors used in the Inner Tracking System of the ALICE experiment at the Large Hadron Collider at CERN, have recently been developed to measure the X-ray energy and timings [1]. In this experiment, the number of detector's anode readout required are 224 channels [1]. Similarly, there are many instruments where multi-channel readout is required to carry out measurements in different directions or to carry out large area readout.

There are currently no commercially available back-end electronics to read these many channels. The reading approaches that are currently available demand more mass, power, and processing. The development of a new pulse height analysis technique for spaceborne instruments is required in this direction. The technique should provide comparable or better performance while using less instrument mass, power, and size. The primary research goal is to create a novel pulse height measurement technique for radiation detector readout that performs similarly to existing PHA techniques. Because the technique employs interpolation, selecting the appropriate 1-D interpolation method is also an important goal.

It is demonstrated that the LaGrange's interpolation technique is best suited for the proposed method due to its low relative and mean square error. Lagrange's interpolation methods also consume fewer resources than other interpolation methods with comparable relative error and mean square error.

For the new method, the SDD based X-ray spectrometer is designed. The other known PHA methods are developed and compared with new designed method. The interpolation method gives 165 eV energy resolution at 5.9 keV by illumination ^{55}Fe

source in front of detector. The archived resolution may be enough for many of the radiation detector systems like Gamma-ray detector, particle detector or large area X-ray detector (which has many discrete X-ray detectors) etc.

1.2 Plan of thesis chapters

The first chapter provides a brief overview of space instruments and the challenges involved in their development for use in space. Following that, the research objectives and short results of each activity are provided.

The second chapter discusses the various types of radiation and radiation detectors. In addition, the radiation detector technologies that have been developed over the last few years are being studied in terms of their working principle and possible readout techniques. The suitability of these detectors for the desired energy range is described by comparing their performances and highlighting their advantages and disadvantages.

The working principle of the Silicon drift detector based on the sideward depletion concept is discussed in Chapter 3. This chapter also discusses the concept and design details of the SDD-based X-ray spectrometer's subsystems. The CSPA concept, shaping amplifier, and HV bias are all thoroughly explained. The SDD-based X-ray spectrometer was built with commercially available qualified components and various backend electronics. The various pulse height analysis techniques were thoroughly discussed. To compare their performance, the techniques were developed and interfaced with the front-end electronics. The FWHM at 5.9 keV for each technique is calculated by illuminating the ^{55}Fe X-ray source in front of the detector.

The proposed methods and their implementation using an SDD detector and FPGA-based backend electronics are described in Chapter 4. This chapter also discusses the importance of researching various interpolation algorithms. The interpolation techniques were thoroughly examined and implemented on hardware in order to compare their performance in terms of relative error, mean square error, mean absolute deviation, and FPGA resource utilization. Based on the comparative study, the appropriate interpolation method was chosen to be implemented in the proposed method.

The results of the proposed method for pulse height analysis are obtained for various shaping time and interpolation points. The performance of ^{55}Fe and ^{241}Am X-

ray sources is also investigated. The proposed method's performance is assessed by measuring the FWHM, shaping time requirement, pile-up, and processing time.

Chapter 5 presents the research activity's conclusions as well as its future scope. We intend to expand our research into pileup correction for high-count rate applications. In addition, we are considering developing a hybrid / ASIC chip for the proposed method, which would incorporate a large number of readout channels with higher resolution in a small package.

C H A P T E R – 2

2 THEORETICAL BACKGROUND

In this chapter basic idea about radiation and its types are discussed. Various radiation detectors and their working principles are explained in detail. The methodology for various detector readouts are explained in detail.

2.1 Types of radiation relevant to space

Before creating any instrument for radiation detection, it is necessary to understand the type of radiation. A type of energy called radiation is released or transferred as rays, electromagnetic waves, or particles. Some forms of radiation, like visible light and infrared radiation, may be seen or felt, while others, like X-rays and gamma-rays, are invisible and can only be viewed directly or indirectly with the use of special equipment. Non-ionizing radiation and ionizing radiation are the two main categories of radiation.

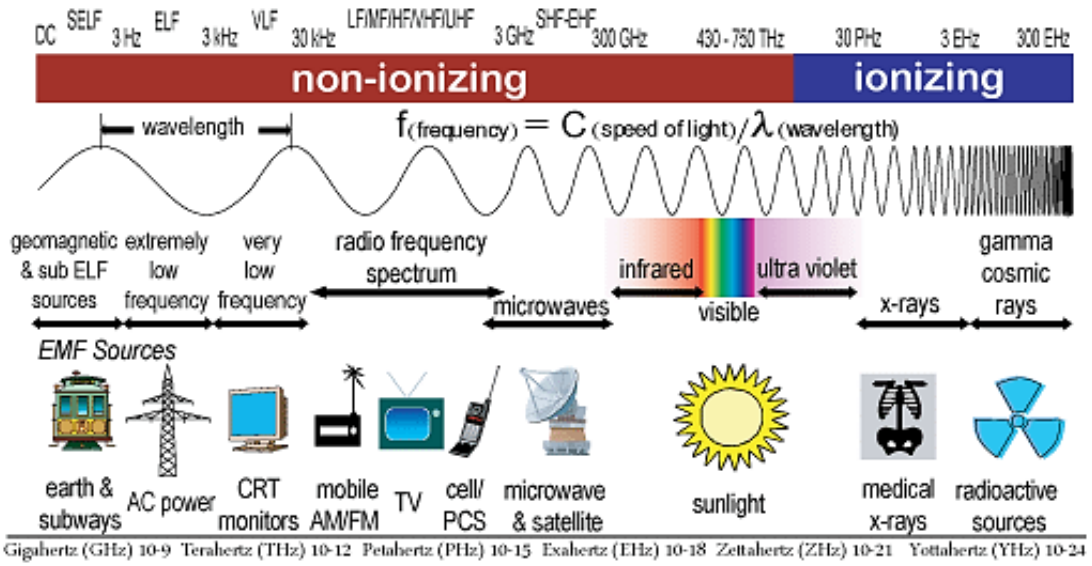


Figure 2.1: Types of radiation on the electromagnetic spectrum [2].

2.1.1 Non-ionizing radiation

Non-ionizing radiation sources are used by and exposed to people every day. The energy contained in this type of radiation is insufficient to ionize atoms or molecules. Non-ionizing radiation is used by GPS units, microwave ovens, FM and AM

radios, televisions, mobile phones, cordless phones and in many other instruments. Other types of radiation include exposure to the magnetic field caused by being close to electrical equipment, earth's magnetic field, wiring in homes, and transmission lines. These are defined as extremely low frequency (ELF) waves.

2.1.2 Ionizing radiation

Some forms of radiation are powerful enough to dislodge electrons from their atomic orbits, causing a shift in the electron/proton balance and a positive charge on the atom. Ions are the name for molecules and atoms that are electrically charged [3]. Ionizing radiation is the name for radiation that can create ions.

Ionizing radiation comes in many different forms, mostly as a result of charged particles, neutral particles, and photons. These are a few of the relevant ones:

Alpha radiation:

Two protons and two neutrons make up alpha radiation; as they lack electrons, they have a positive charge. Alpha particles can scarcely penetrate skin due to their size and charge, and can be fully blocked by a piece of paper. [4].

Beta radiation:

Fast-moving electrons that have been expelled from an atom's nucleus make up beta radiation. Beta radiation is more invasive since it has a negative charge and is roughly $1/7000^{th}$ the size of an alpha particle [4]. A modest amount of shielding, such as a sheet of plastic, can block beta radiation.

Gamma radiation:

Gamma radiation has a high penetration level. It often occurs soon after an atom's nucleus releases an alpha or beta particle. It may travel through the human body since it has no mass or charge, but denser things like concrete or lead absorb it [4].

X-rays:

While X-rays are a kind of radiation similar to gamma radiation, they are mostly created by artificial techniques as opposed to radioactive materials [4]. In contrast to light, X-rays have a higher energy and can penetrate most materials, including the human body. Images of inside organs and tissues are created using medical X-rays.

Neutron radiation:

When nuclear fission and other processes cause neutrons to be released from the nucleus, neutron radiation results. Nuclear fission is exemplified by the nuclear chain reaction, in which the release of a neutron from one fissioned atom triggers the fission of another, releasing more neutrons. Neutron radiation, unlike other types of radiation, is absorbed by substances like plastics and paraffin wax which contains a lot of hydrogen atoms. Figure 2.2 displays the various radiations' decay types.

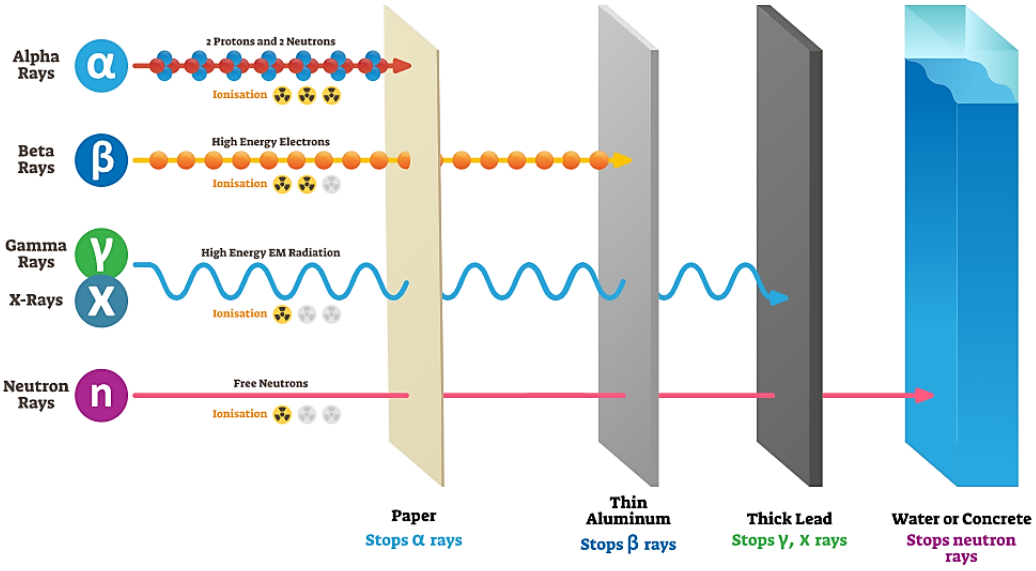


Figure 2.2: Types of decay for various radiation [3].

People are regularly exposed to electromagnetic radiation in their daily lives thanks to devices like microwaves, mobile phones, and X-rays for medical diagnosis. There are various naturally occurring sources of electromagnetic and ionizing radiation in addition to technology made by humans, such as radio transmitters, light bulbs, heaters, and gamma-ray sterilizers (machines that destroy microorganisms in fresh or packaged food). These comprise stars, other astronomical phenomena like quasars or galactic centers, as well as radioactive substances in the Earth's crust and radiation trapped in the planet's magnetic field. [3].

The Sun is the principal radiation source for Earth. All electromagnetic spectrum wavelengths are emitted by the Sun. Visible, infrared, and ultraviolet radiation (UV) make up the bulk. On occasion, the Sun's surface experiences enormous explosions known as solar flares and coronal mass ejections (CME), which release enormous quantities of energy into space in the form of X-rays, gamma-rays, and streams of protons and electrons known as solar particle events (SPE).

Galactic Cosmic Radiation, or GCR, is a kind of radiation that originates largely from inside our Milky Way galaxy but also from sources beyond the solar system. GCR are massive, high-energy ions of elements that have had all of their electrons removed during their almost light-speed passage through the galaxy. They may ionize atoms as they move through matter and essentially unhindered through the skin of an astronaut or a normal spaceship. Current spacecraft and upcoming space missions must contend with the GCR, which is a prominent source of radiation in our solar system [3]. The average strength of these particles, which are influenced by the Sun's magnetic field, is highest during the minimal sunspot period when the Sun's magnetic field is least strong and least able to deflect them.

2.2 Systems used for radiation measurement

A sensor or detector is a device or part of a system that monitors several factors, including physical, chemical, biological, and others [5]. Radiation is defined as the energy emitted by a source via a medium in the electromagnetic spectrum, ranging from radio waves with the smallest wavelength to gamma radiation with the largest energy.

Radiation detectors operate on the principle of ionization to identify radiation particles such as alpha, beta, gamma, X-ray, protons, neutrons, etc. [6]. A highly energetic nuclear particle that enters a material medium ionizes the medium, which may be detected using various sensor techniques.

Direct or indirect methods are used to convert the photon energy emitted by the detector material during the encounter into an electrical signal; the conversion factor varies depending on the detector [7]. Consequently, radiation detectors may be generically divided into two categories.

1. Direct conversion type

2. Indirect conversion type

A direct conversion type detector is the one in which the incoming photon is directly converted into an electrical signal, whereas in an indirect conversion type detector, the conversion takes place in two steps. The first step involves conversion of photon into visible light and the second step involves the conversion of visible light into electrical pulse. The schematic representation of production of charge carriers in direct and indirect conversion type detector is shown in Figure 2.3.

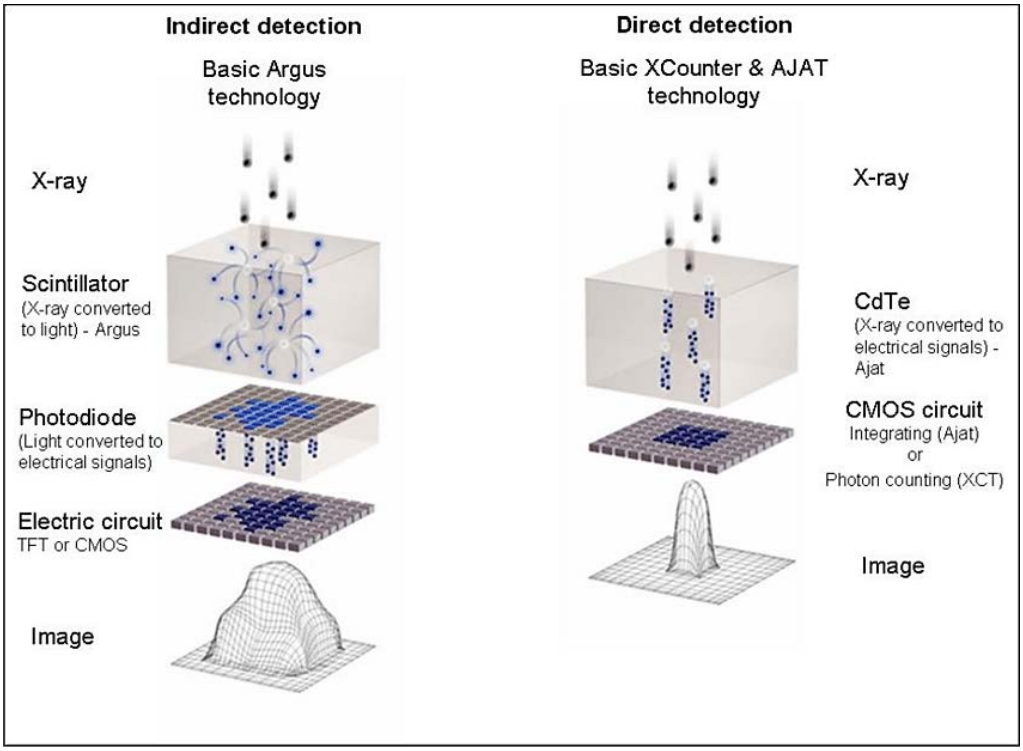


Figure 2.3: Schematic representation of the production of charge carriers in direct and indirect conversion type X-ray detectors [8].

The indirect conversion approach induces loss of information in the process particularly at very low radiation inputs. Direct conversion detectors are those that directly convert input photon energy into a certain quantity of charge, which is subsequently collected at the output electrode of the device. These include semiconductor detectors and gas-filled detectors. Since there is no charge loss in the direct conversion type, it offers superior energy resolution. The energy required to create one electron-hole (e-h) pair in gas-filled detectors varies from 25 - 35 eV and in the case of a semiconductor detector, it is of the order of few eVs (for silicon, 3.6 eV and for germanium, 2.9 eV).

Scintillation detectors are indirect conversion types, wherein the incident radiation is converted into a shower of optical photons (visible and near visible region). Using photodetectors, these photons are subsequently captured and transformed into electrical charge. The photodetector may be a silicon photo detector, a photomultiplier tube (PMT), or a fairly recent technological innovation called a silicon photomultiplier (SiPM). Due to two-step conversion mechanism in the indirect conversion process, there is loss of signal due to light coupling, resulting in poor energy resolution. The average energy required to create one e-h pair in scintillators is of the order of 25 eV.

Biological, chemical, and physical parameters are measured by sensors, which play a key role in monitoring, measuring, and controlling systems [9]. Radiation is the energy that comes from a source and travels through a medium as waves or particles in the electromagnetic spectrum. Gamma radiation is the hottest and most potent type of radiation, whereas radio waves are the newest and have the shortest wavelengths.

Based on the ionization principle, a nuclear detector is a device that can identify several types of particles, including protons, neutrons, beta particles, gamma rays, X-rays, and alpha particles [10]. When a very energetic nuclear particle interacts with a material medium and ionizes it, radiation can be detected. Different types of sensors, broadly categorized in Figure 2.4, are needed to detect this energy.

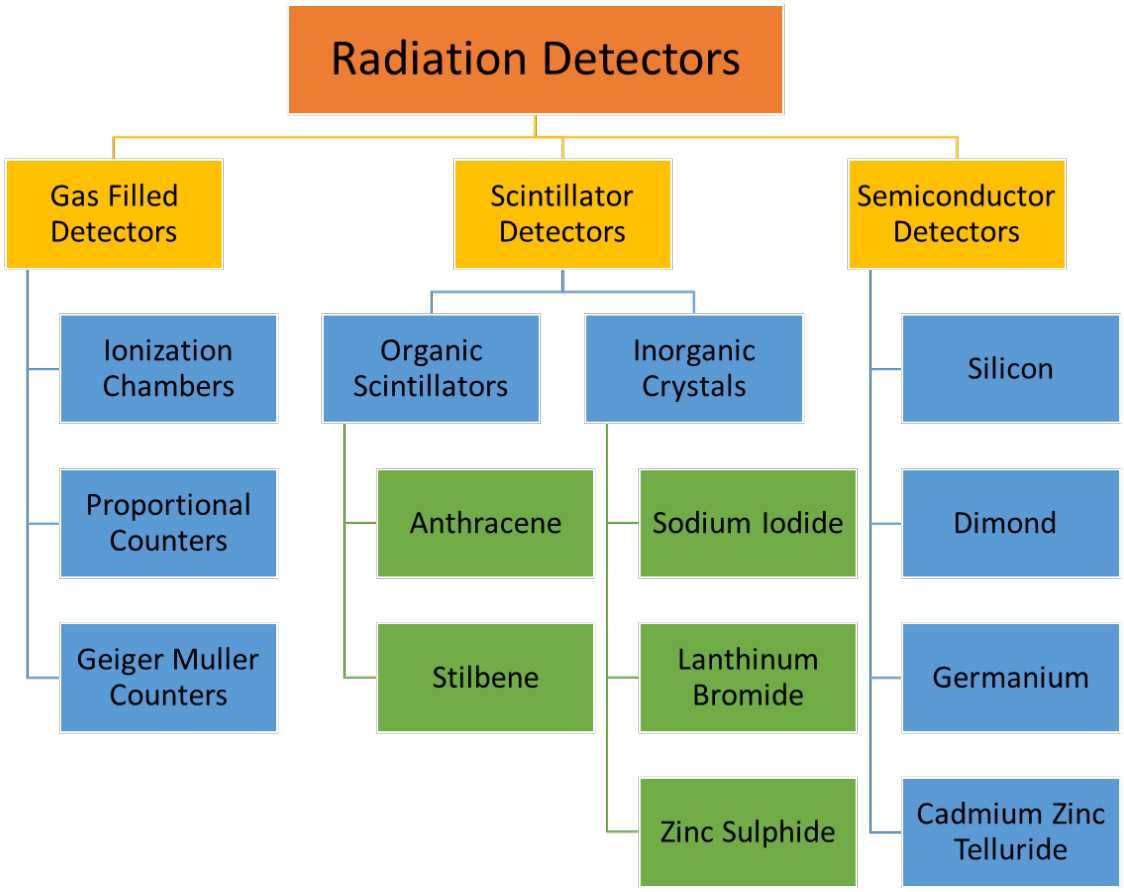


Figure 2.4: Classification of radiation detectors.

In order to correctly extract the energy or temporal information involved with radiation interactions, the majority of radiation detectors require pulse (or signal) processing circuitry. The general block diagram for the readout of the radiation detector is shown in Figure 2.5. The radiation detector generates the charge cloud, which will be converted into an electrical form by a pre-amplifier. The pre-amplifier signal will be

used in a subsequent step to calculate the incident energy. The voltage pulse produced from the pre-amplifier has an amplitude that is directly proportional to the incident energy. The pre-amplifier's output pulse generally has an amplitude of a few tens to hundreds of millivolts and is too small to directly measure. Consequently, the pulse is often processed through a linear amplifier as the following step where the voltage gain of ten or more can be given. The shaped linear pulse at this location will cover a range of 0 to 10V or ADC reference voltage. In a simple counting system, the shaping requirements are often not harsh; it is only when the counting rate is rather high that one needs pay great attention to the particular type of shaping chosen. The pulse height analyzer will receive the amplified signal from the shaping amplifier.

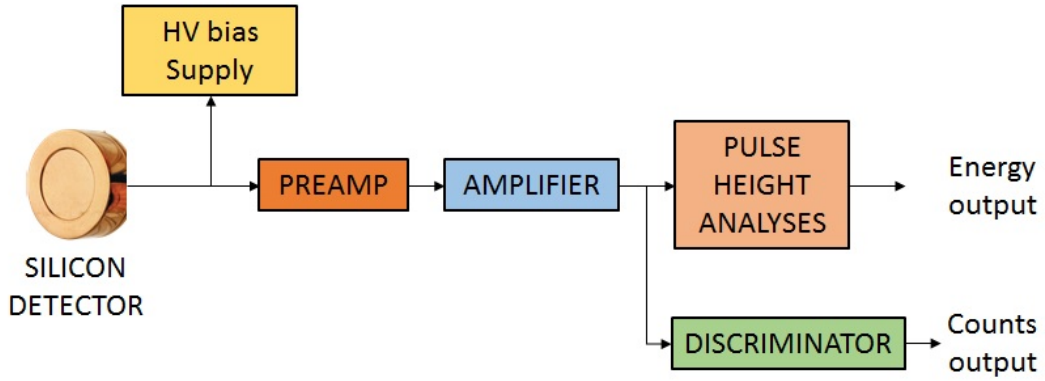


Figure 2.5: Radiation detector readout block schematic.

The process of determining the amplitude of the voltage or current pulse is called pulse height analysis. The shaped linear pulse must be transformed into a logic pulse in order to accurately count the pulse. The integral discriminator, which consists of a device that produces a logic output pulse only if the shaped input pulse amplitude exceeds a predetermined discriminating level, is the simplest way to detect the particle interaction. The process of pulse height analysis can be started using the logic pulse. There are multiple radiation detectors available which can be used to make instruments and derive various methods of PHA.

Sections 2.3, 2.4, and 2.5 of Chapter 2 will cover various types of detectors used in X-ray, Gamma-ray, and particle detection, with a focus on semiconductor detectors, specifically silicon detectors. A gamma-ray or X-ray detector is a transducer that converts photon energy into voltage pulses. The interaction of an X-ray photon within the active volume of the detector produces charge carriers (electron-hole pairs) through photoionization process. The current pulse produced by these charge carriers is

converted to a voltage pulse, by a charge to voltage conversion amplifier known as charge sensitive pre-amplifier. The incoming X-ray photon's energy is directly proportional to the voltage amplitude of the pulse. The signal is then processed by a suitable low-noise electronics chain to obtain the energy and other required parameters such as arrival time, the angle of arrival, position of interaction etc. X-ray detectors are also used to detect other types of electromagnetic radiations such as electrons, protons and alphas etc.

2.3 Summary

The working principle and various types of radiation detectors are discussed in this chapter. This chapter also discusses technologies used in X-ray studies over the last several decades, including their operating principles, charge formation, and readout techniques. The suitability of these detectors for the desired energy range is described by comparing their performances and highlighting their advantages and disadvantages. Because of advancements in silicon detector technology, it is possible to design X-ray spectrometer instruments with energy resolution close to the Fano limit. The application of silicon detectors in various applications is also covered.

C H A P T E R – 3

3 EXPERIMENTAL METHODS

The various components required to develop radiation detection instruments like a detector, various types of CSPA, shaping amplifier, high voltage bias and pulse height analysis techniques are discussed in this chapter.

3.1 Detector and Pre-amplifier

One of the crucial aspects of an experiment is the choice of an appropriate detector. The detector must be a radiation detector and be simple to operate in a lab setting without the need for special shielding or vacuum. In this opinion, the silicon drift detector (SDD) is a practical choice since it is frequently offered as modules with a built-in Peltier, which removes the need for liquid nitrogen (LN) cooling, and a temperature sensor for accurate temperature control [63]. The SDD detector supports throughput count rates of up to 100 Kcps and can tolerate significantly greater input count rates. The SDD provides better resolution in the 1–15 keV range.

3.1.1 Silicon Drift Detector (SDD)

Silicon Drift Detector (SDD) is a new technology silicon photodetector with a unique electrode structure and offers low detector capacitance compared to planar Si PIN detector of the same area. This yields low noise even at shorter shaping times and hence, SDDs can be used at much higher count rates with desired energy resolution. The concept of SDD was introduced in 1984 by Gatti and Rehak, who presented the concept and the experimental results [64]. The concept was based on sideward depletion. SDD was initially proposed for position measurement and considered as a replacement for gas chambers in the form of a solid-state device. In his work, it was observed that detector capacitance is independent of detector area. In 1985, Rehak and Gatti [65] showed the use of SDDs for energy measurements rather than position measurement with SDD in circular form. In these SDDs, the drift electrodes are made on both sides to form the radial electric field. The planar electrode concept in SDD was introduced in 1987 by Kemmer [66] with planar contact on one side and drift electrodes on the opposite side. As discussed in the earlier chapter, the fabrications of planar

contacts are easier to manufacture. This technique also provides a very thin dead layer in the entrance window where only X-ray photons are allowed to enter into the detector, which is important for X-ray spectroscopy. The first good-quality SDD for laboratory application was produced in 1995 for EDS and XRF measurements [67]. In the last two decades, SDDs have been optimized to achieve very good spectral energy resolution in various types and sizes [68, 69, 70, 71]. Significant research work has been carried out on the SDD readout techniques [72, 73, 74], aiming at improving the energy resolution by reducing the contribution of electronics noise. In recent times, it has been shown that SDDs with advanced readout electronics can provide energy resolution close to the Fano limit.

3.1.1.1 Working principle of SDD

In the conventional PIN photodetector, the ohmic n+ contact extends to the full area of the silicon bulk on one side, and the potential distribution is shown in Figure 3.1 (a). In Figure 3.1 (b), n+ contact is introduced with p+ electrodes on both the sides to achieve the depletion of the bulk and when the bias at n+ contact is increased, creating a potential minimum at center of the bulk with a small undepleted zone near the n+ region as shown in Figure 3.1 (c).

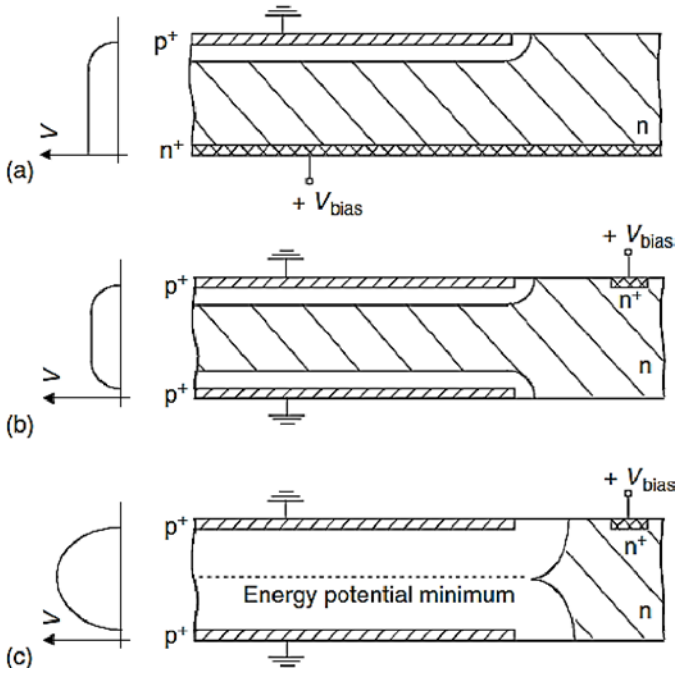


Figure 3.1: Schematic representation of sideward depletion concept [64].

The working principle of the drift detector is understood from the sideward depletion concept. In the case of SDD, an additional electric potential is applied on both

sides to force the electrons to drift towards the n+ electrode for the signal readout, as shown in Figure 3.2.

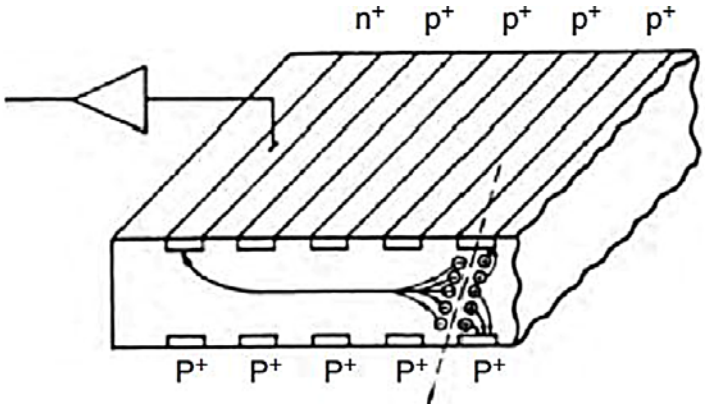


Figure 3.2: Schematic representation of the working principle of silicon microstrip detector [64].

This is achieved by implanting the p+ electrode on both sides. These electrodes are suitably biased such that an electric field line is created, as shown in Figure 3.4. When a photon interacts in the active volume of the detector, the electrons are guided towards the anode and the holes are collected by the nearest p+ electrodes as the p+ electrodes are applied with negative bias. By appropriately biasing the opposing electrodes, the bottom of the potential channel is pushed away from the area near the collecting anode and towards the surface where the anode is located. The electron cloud gives an electric pulse in the anode and the drift time of the electron cloud along with the signal due to holes can be used to derive the measure of the position of the photon interaction [65].

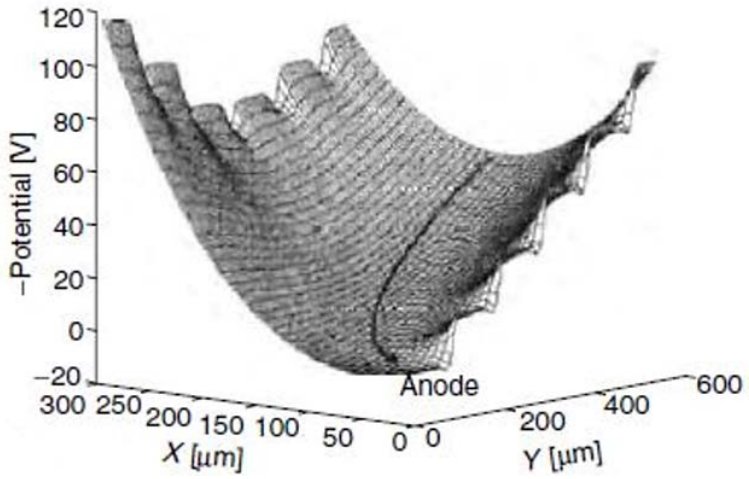


Figure 3.3: The electron guiding potential distribution in the drift region of the SDD pointing towards the anode [64].

The signal due to electron charge will give the energy of the photon. The important finding of this sideward depletion concept is that the detector capacitance is the anode capacitance whose value is independent of the detector area. The anode capacitance is of the order of a few hundred femtofarad. The low detector capacitance provides low noise at shaping times near to 1μs. Thereby the system can be used for high count rate applications.

3.1.1.2 SDD for X-ray measurements

SDDs are ideally suited for X-ray spectrometry due to their low detector capacitance along with the low noise readout system enables them to achieve an energy resolution close to the Fano limit. In the sideward depletion SDD concept, the areas between the p+ strips on the surface are covered with SiO_2 layer. Since the SiO_2 layer contains fixed positive charges, potential minima are created by the spread of potential energy away from the detector surface. The signal electrons produced during photon interaction in the low energy range, <5 keV, might be collected at these locations. [75]. To overcome this limitation at lower X-ray energies, a suitable design topology has been implemented with a thin continuous entrance window without oxide layer gaps [76]. Also, the point anode is kept in the center forming a circular detector that minimizes any signal loss due to the travel length of the signal electrons. The circular SDD optimized for energy measurement is shown in Figure 3.4. Circular SDDs have concentric rings around the point anode, which are applied with progressively higher reverse bias voltages, which guide the photoelectrons into a "point" anode. The drift field with respect to the point anode at the center is shown in Figure 3.5.

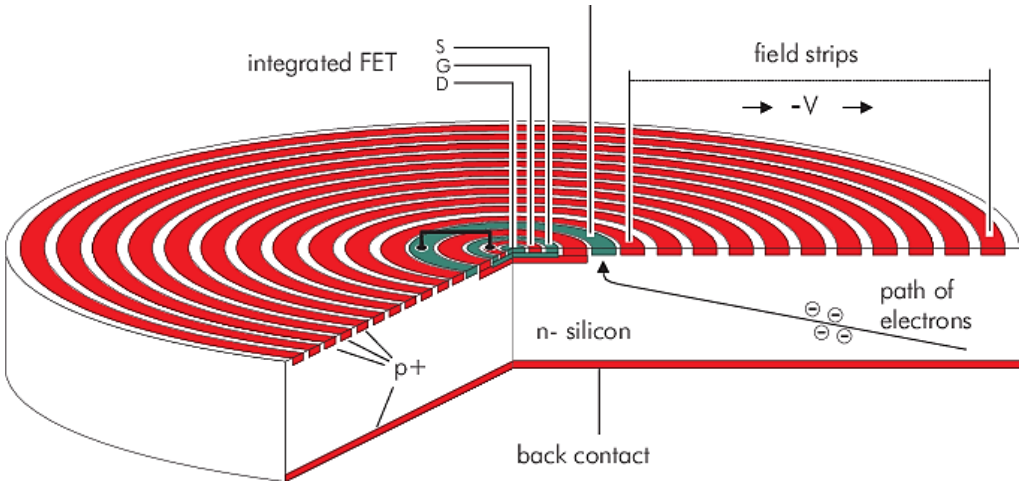


Figure 3.4: Schematic representation of a circular SDD with anode at the center (courtesy: KETEK, GmbH) [77].

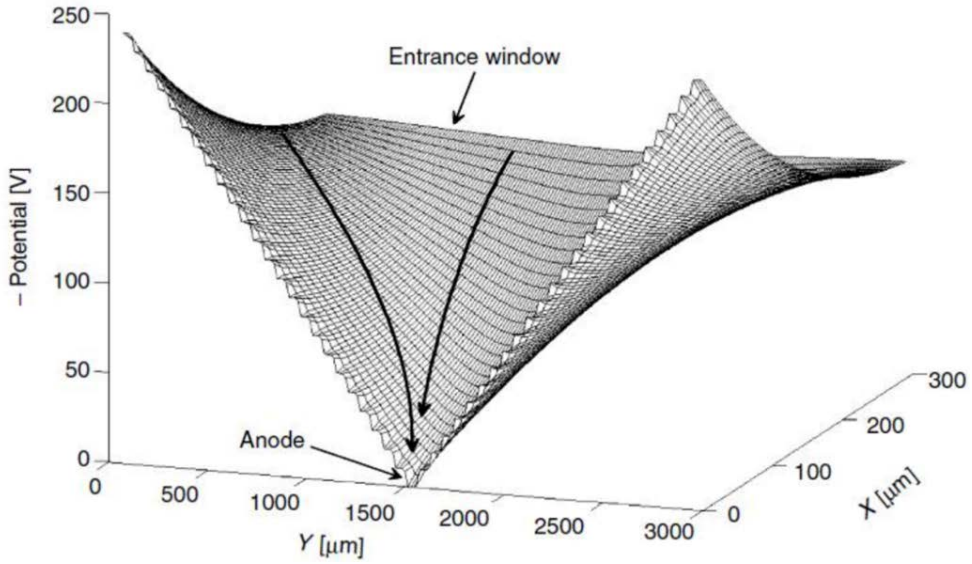


Figure 3.5: The possible electron path (field line) inside the SDD with 300-micron thickness [77].

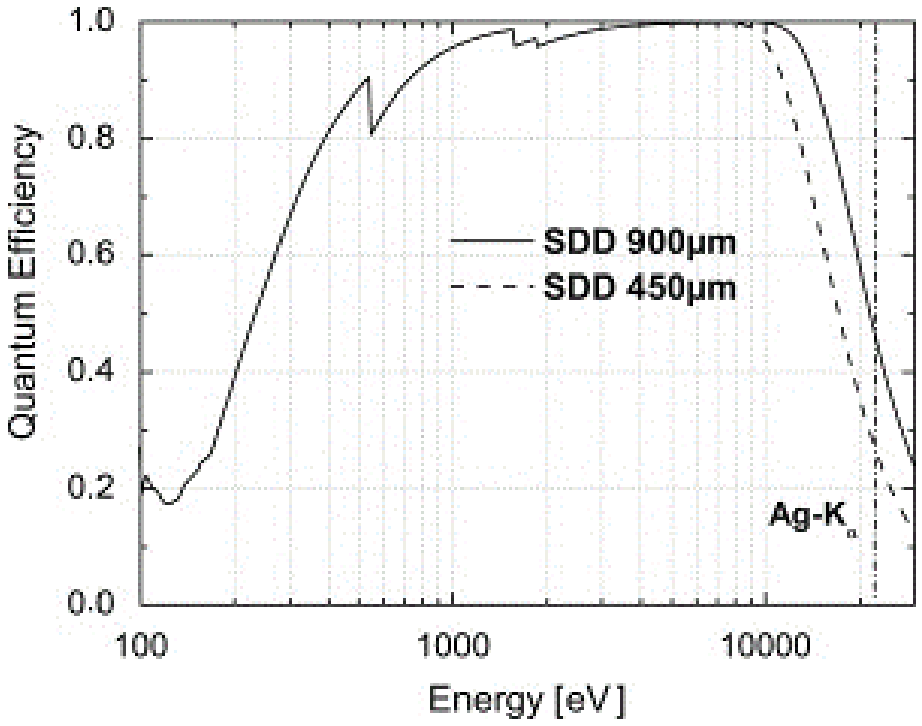


Figure 3.6: Quantum efficiency of 450 and 900-micron thick SDDs with thin dead layer [78].

The bias voltages required for the successive p+ electrodes are derived from a single high voltage applied at the outer electrode by using a resistive divider, which is part of the SDD chip. The inner ring close to the anode and the back contacts are applied with separate bias voltages. The capacitance of the point anode is ~200 fF. The p+ back

contact acts as an entrance window for the radiation to be detected and is made of a shallow p+ implantation with a thickness of the order of a few tens of nanometers [79] which allows to achieve the low energy threshold of a few hundred eV. The quantum efficiency of such SDD with few tens of nm of dead layer for 450 and 900-micron thick detector is reported in [78]. It is shown that quantum efficiency of > 40% could be achieved for incident energies of more than 200 eV as shown in Figure 3.6.

3.1.1.3 SDDs in space missions

Due to its better spectroscopic performance, X-ray spectrometers based on Silicon Drift Detectors (SDD) have been flown on several space missions during the past ten years for a variety of scientific experiments. Earlier space investigations, such as the MinXSS experiment to measure the solar X-ray spectrum on a CubeSat [63], and the solar X-ray monitor (XSM) on the Chandrayaan-2 [80], The APXS instrument on Mars rovers Curiosity, Spirit, and Opportunity [81, 82], The PIXL instrument on mars rover Perseverance [83], and neutron star interior composition explorer (NICER) for soft X-ray timing and spectroscopy of astrophysical sources [84] employed silicon drift detectors. The comet mission Rosetta also carried SDD based X-ray spectrometer onboard PHILAE lander for the comet 67P/Churyumov-Gerasimenko to carry out in-situ elemental composition measurements. Recent lunar mission from China, Change'3 also carried SDD for in-situ elemental composition measurements on the lunar surface.

There are planetary/space missions in the near future plan to use scientific instruments having SDD as a sensor. Chandrayaan-3, the Third Indian mission to Moon is slated for launch in the year 2023 uses SDD detector in one X-ray spectrometer instruments. The space mission, Large Observatory for X-ray Timing (LOFT) is being developed by European Space Agency (ESA) with large number of large area SDDs with total effective area of 10 m^2 for astronomical observations. This mission is slated for launch in the coming years.

3.1.1.4 SDD detector module used for an experiment

The main advancement of SDD devices is the application of concentric rings in the detector region. These rings are used with increasingly higher bias voltages to direct the photo-electrons created to a point anode when an X-ray is absorbed. The anode's minimal surface area maintains an extremely low capacitance. This is significant

because total input capacitance, which is proportional to voltage noise, is the primary noise source in silicon X-ray spectroscopy. The SDD has less noise because to its low capacitance, especially during extremely fast shaping periods. The field-effect transistor (FET), which makes up the first stage of the charge-sensitive pre-amplifier (CSPA), and the feedback capacitor, which integrates charge from the detector anode, are both present in the silicon drift detector (SDD) module because they are essential to the SDD's performance [63]. Because of its space heritage and compatibility with the in-house built charge-sensitive pre-amplifier (CSPA), the silicon drift detector (SDD) module was purchased from KETEK for the experiment.

Figure 3.7: Silicon drift detector (SDD) module with lid, KETEK VITUS H80 (left). Views of the TEC and on-chip collimator from an unencapsulated silicon drift detector (SDD) module (right). [24] (Image courtesy of KETEK GmbH.)

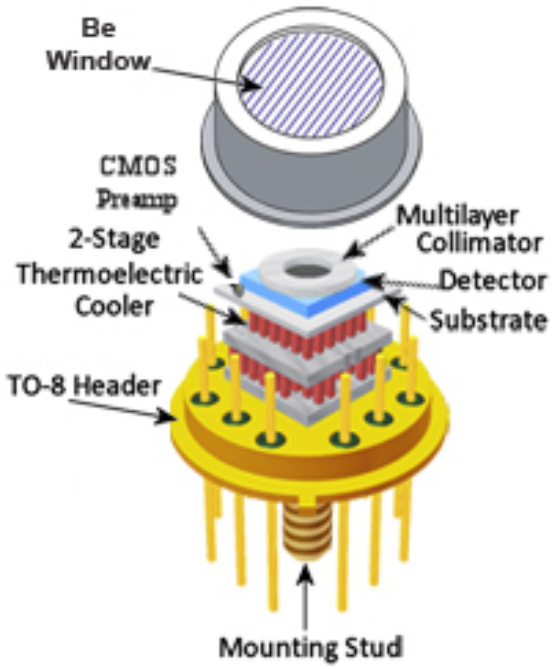


Figure 3.8: SDD module schematic view [85] (courtesy: KETEK, GmbH - H80).

The KETEK SDD detector used in the experiment has the component number VITUS H80. The detector is housed in a typical TO-8 package and has a wide collimated area of 80 mm^2, a diameter of 21 mm, a height of 19.5 mm. Figure 3.7 shows the KETEK SDD module in detail. The module has a 25 μm thick filter window which is made up of Be (Beryllium) with DuraCoat and it is installed on the TO-8 package cap that is visible in a detector's explored view (Figure 3.8). This Be filter will restrict the ambient light to saturate the detector. The detector's chip has a thickness of 450 μm. The silicon bulk of the SDD must be completely depleted by applying a negative voltage to the detector's back contact in order to make the sensor sensitive to incoming photons.

An NTC thermistor with a resistance of 10 kΩ at 25 °C is used to measure the temperature within the detector. To operate the detector at negative temperatures, a Peltier cooler is attached to it within a container. The inside schematic view of the detector made by KETEK is shown in Figure 3.9.

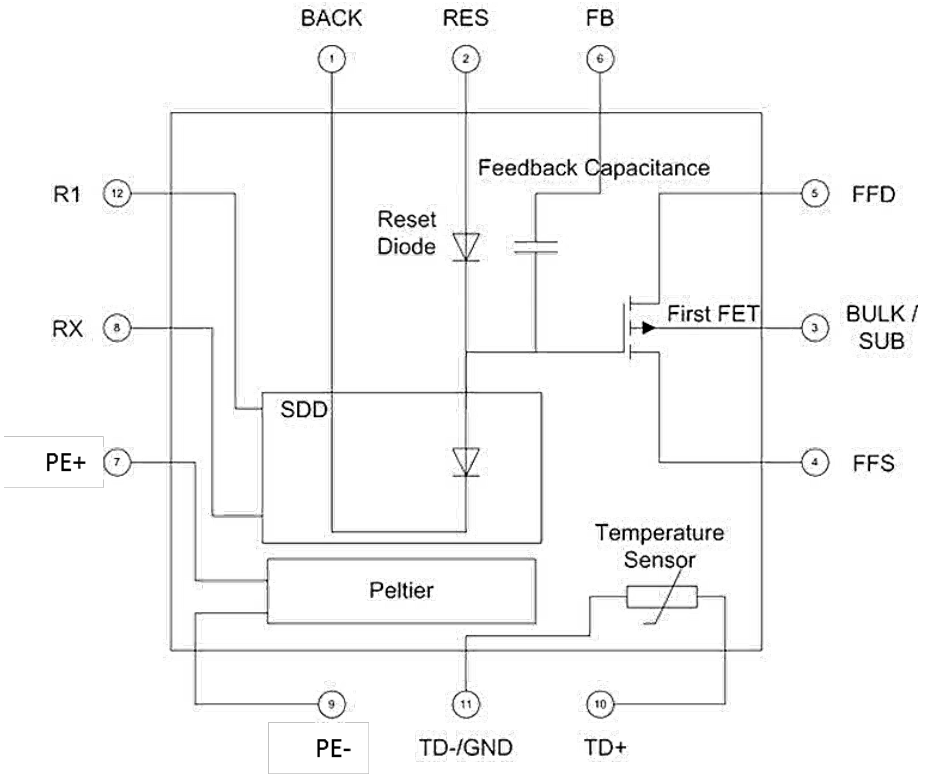


Figure 3.9: Internal electrical interconnection diagram of SDD module [86] (courtesy: KETEK, GmbH).

High voltage biases of -20 V, -130 V, and -60 V are supplied to the SDD's Inner Ring (R1), Outer Ring (RX), and Back Contact (RBACK) electrodes in order to

produce an electric field that directs electrons to the anode through the SDD detector. Similar to this, the drain, source, and bulk of a FET have corresponding bias voltages of 3V ± 0.5 V @ 3 mA, 0 V, and -5 V ± 1 V. The maximum rating for the peltier element is 4.5 V and 1 A with a maximum differential temperature of 75 °C. Table 3.1 is a list of the SDD detector's specifications..

Table 3.1: Specifications of the SDD module planned for the experiment

Sr. No.	Parameter	Values/ Components
1	Area	80 mm^2
2	Absorption depth	450 μm
3	Windows	8 μm Be (with 1-micron thick Dura Coat)
4	Cooling performance	~T > 75 K
5	HV (R_1, R_X, R_{BACK})	-20 V, -130 V and -60 V
6	Peltier Element	4.5 V, 1 A
7	Temperature monitor	Thermistor, 10 KΩ at 20°C

3.1.1.5 Design of Charge Sensitive Pre-Amplifier (CSPA):

The block schematic of the developed charge-sensitive pre-amplifier along with SDD is shown in Figure 3.16. The first stage of the charge-sensitive pre-amplifier is the charge to voltage conversion amplifier, where the internal FET is operated in a common source configuration. The internal charge storing capacitor is connected to the feedback path that determines the gain of the charge to voltage conversion amplifier. The output of the charge to voltage conversion amplifier is connected to the gain amplifier to provide additional gain to the feeble signal that is of the order of < 1 mV/ keV.

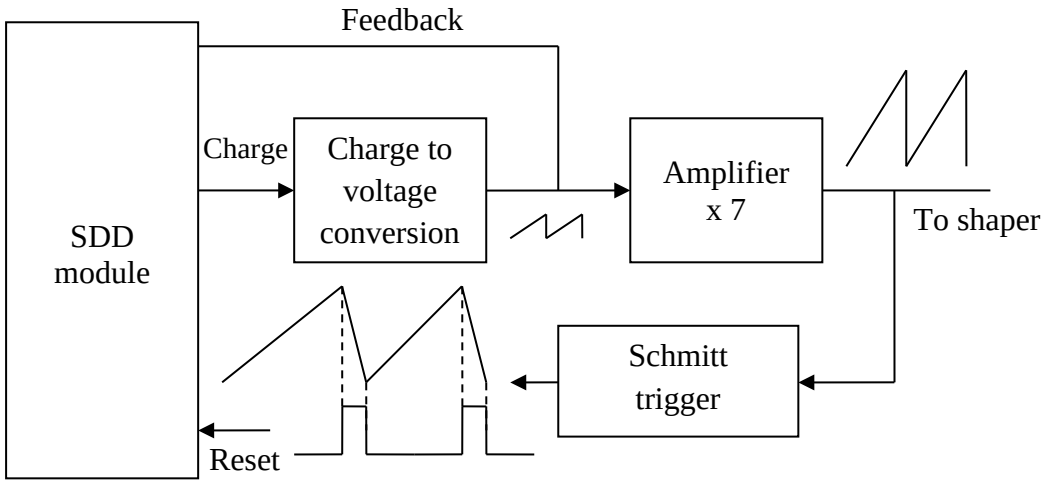


Figure 3.10: Block schematic of pulse reset type Charge Sensitive Pre-Amplifier (CSPA) design [105].

The feedback capacitor integrates the leakage current and also the current pulses due to photon interaction. The charge is integrated into the form of a ramp signal and the charge should be removed before the amplifier attains the saturation limits. To generate the reset pulses to remove the charge in the feedback capacitor, the output of the gain amplifier is fed to Schmitt trigger-based reset pulse generator, which gives reset pulses when the ramp signal amplitude crosses the set threshold limit. The duration of the reset pulse is set ~ 1 μs which is fed to the reset diode to discharge the charge stored in the feedback capacitor. The selected operational amplifier device for the CSPA design is AD829 which has a wide bandwidth of 28 MHz, low input noise of 4 nV/√Hz and a high slew rate of 230 V/μs. The Schmitt trigger is made using comparator LM311.

The amount of the leakage current produced by the SDD in the absence of any photons interacting with the detector will determine the ramp signal frequency at the CSPA's output. Figure 3.17 displays one such ramp signal that was recorded in the cathode ray oscilloscope (CRO) (left). The ramp signal frequency fluctuates with the energy and rate of a photon interacting with the detector when there are photon interactions present. Each photon interaction appears as a step voltage pulse on the ramp and the magnitude of the step pulse is proportional to the incident photon energy as shown in Figure 3.17 (right).

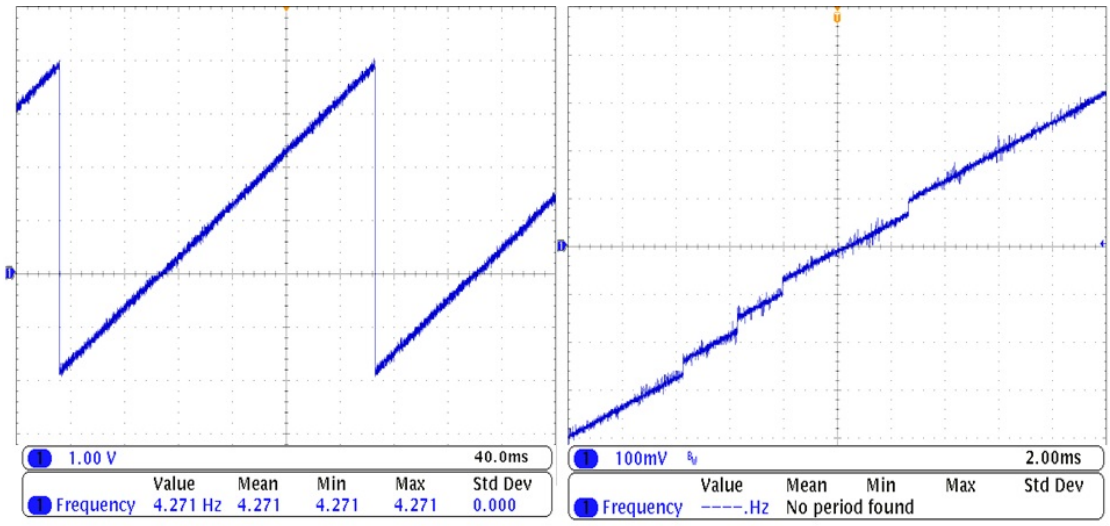


Figure 3.11: CRO screenshot for ramp signal output from CSPA (left), Step on the ramp signal indicating X-ray interaction with the SDD detector (right).

The amplitude of a step pulse at the output of charge to voltage conversion amplifier of CSPA (first stage of CSPA) is ~ 0.74 mV/keV (assuming the value of C_f is ~ 60 fF) and at the final output of CSPA is ~ 5 mV/keV. Application Specific Integrated Circuit (ASIC) based charge readout ICs have been developed in recent times [99, 100, 101] and shown to provide the energy resolution of ~140 eV at 5.9 keV for small area SDD modules. Recently, a CMOS-based ASIC has been developed [102] that is integrated along with the small area SDD module and has shown to provide an energy resolution of ~ 125 eV at 5.9 keV.

The step pulses must be turned into a semi-gaussian pulse after being converted from charge to voltage, or they can be supplied directly to an FPGA or digital signal processor (DSP) for pulse processing after being digitized.

3.1.2 Shaping Amplifier

A shaping amplifier is generally used following the CSPA stage that performs three functions. First, the shaping amplifier provides an output pulse with a faster return to the baseline than the CSPA, which has a peak to baseline return time of a few tens of microseconds. This is crucial at high count rates because successive event pulses have a tendency to "pile up." Other than that, by narrowing the signal bandwidth as needed for the application, the shaping amplifier removes noise from the pre-amplifier output signal. Finally, the shaping amplifiers also provide the necessary gain to amplify the signal from CSPA, which is very small (few mV/keV). A shaping amplifier is a

combination of high pass and low pass filter amplifiers, which reduces the signal bandwidth and thereby improves the signal-to-noise ratio and provides the necessary gain to match the analog to digital converter (ADC) range. The output of the shaping amplifier will be in the form of a semi-gaussian pulse and one can get close to a gaussian pulse shape by increasing the number of low pass filter amplifiers in the design. The shaping amplifier is designed with three stage amplifier, first stage is the CR high pass filter amplifier which defines the desired fall time of the signal with the C_1R_1 time constant. It is represented by the equation (3.9)

$$V_d = V_{in} e^{-\frac{t}{\tau_d}} \tag{3.1}$$

Where, V_d is the signal amplitude at the output of the C_1R_1 differentiator and τ_d is the differentiator time constant. The amplifier after the CR stage is known as CR amplifier, providing suitable gain to an output signal having a fast rise time. The output of the CR filter amplifier is given to two-stage RC low pass filter amplifiers with time constants of R_2C_2 and R_3C_3 respectively. The two-stage RC filter amplifier defines the rise time or peaking time of the pulse. The equation for a one-stage RC filter is given in equation (3.10).

$$V_i = V_d \left(1 - e^{-\frac{t}{\tau_i}}\right) \tag{3.2}$$

Assuming the CR differentiator and RC integrator time constants are equal i.e., $\tau_d = \tau_i = \tau$, then the equation becomes (3.11).

$$V_o = V_{in} \left(\frac{t}{\tau}\right) e^{-\frac{t}{\tau}} \tag{3.3}$$

The output of the *CR-RC* type shaping amplifier with step input for $\tau_d = \tau_i$ is shown in Figure 3.18.

To get the shaping amplifier output close to Gaussian, the number of RC stages has to be increased and the equation becomes (3.12).

$$V_o = V_{in} \left(\frac{t}{\tau}\right)^n e^{-\frac{t}{\tau}} \tag{3.4}$$

Where, n is the order of RC integrator stages and the shaping amplifier output for one stage CR filter and a number of RC filters is shown in Figure 3.19. The shaping amplifier has been designed using AD829 op-amp with three-stage CR-(RC) 2 type (5 poles) shaping.

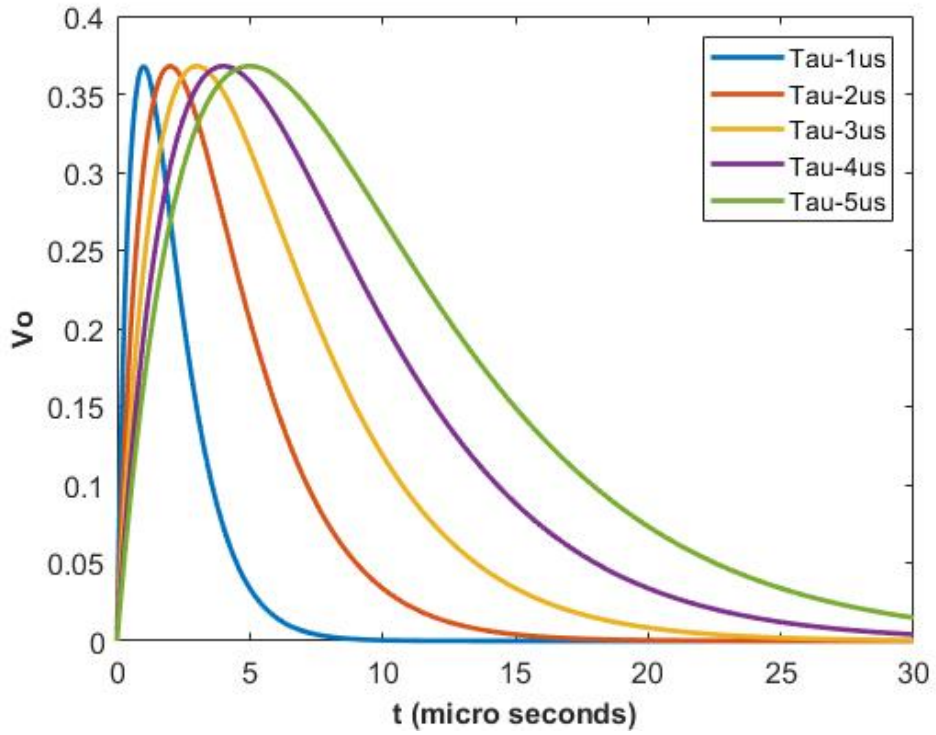


Figure 3.12: Simulated shaping amplifier output for equal CR-RC time constants.

Increasing the number of RC stages will increase the hardware complexity substantially and hence limit to two-stage RC filters. The block schematic is shown in Figure 3.20. The shaping amplifier gain is decided based on the energy range covered by the spectrometer.

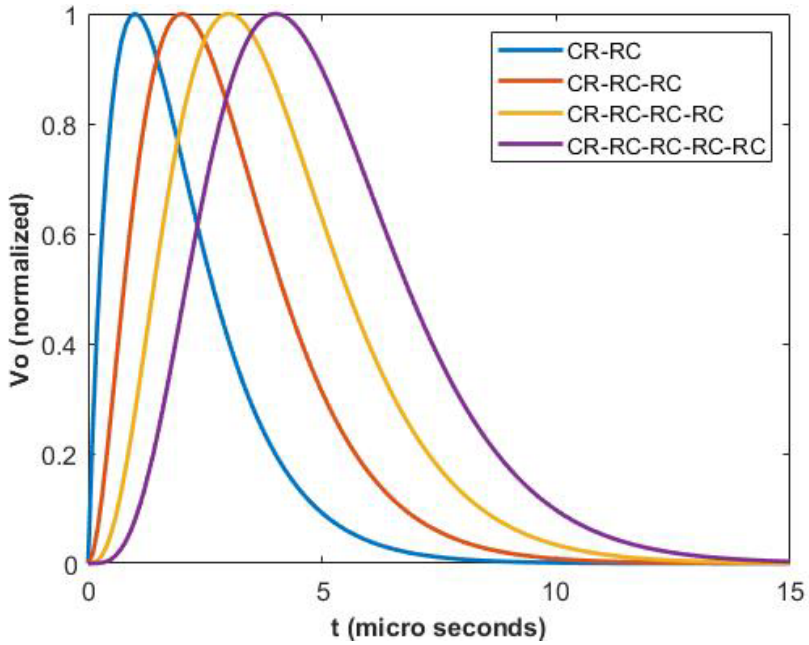


Figure 3.13: Simulated shaping amplifier output with one CR and multiple RC stages.

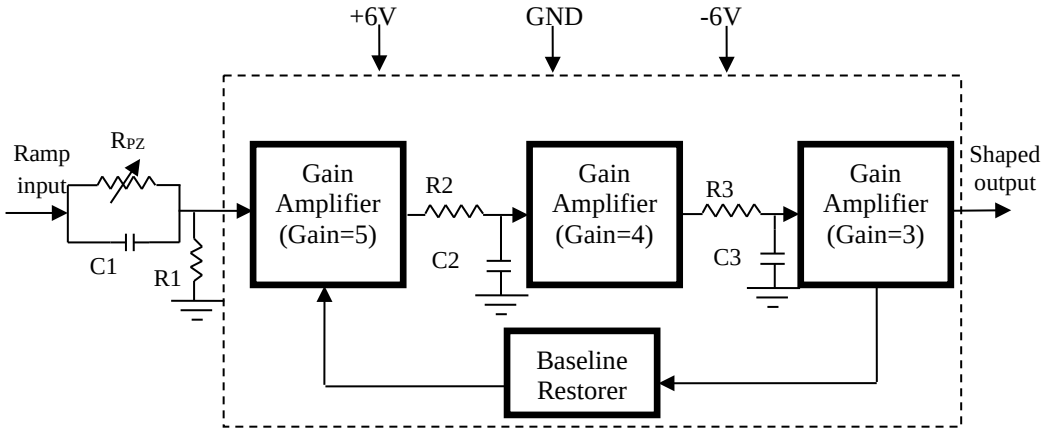


Figure 3.14: Block schematic of CR-$(RC)^2$ type shaping amplifier.

3.1.3 High Voltage Bias Generation for SDD

SDD requires three high voltages for its operation on the terminals namely outer ring R18 (R_x), inner ring adjacent to anode R_1 and back contact R_{BACK}. The schematic representation of the high voltage bias pin locations on the SDD module and the filter connections are shown in Figure 3.21.

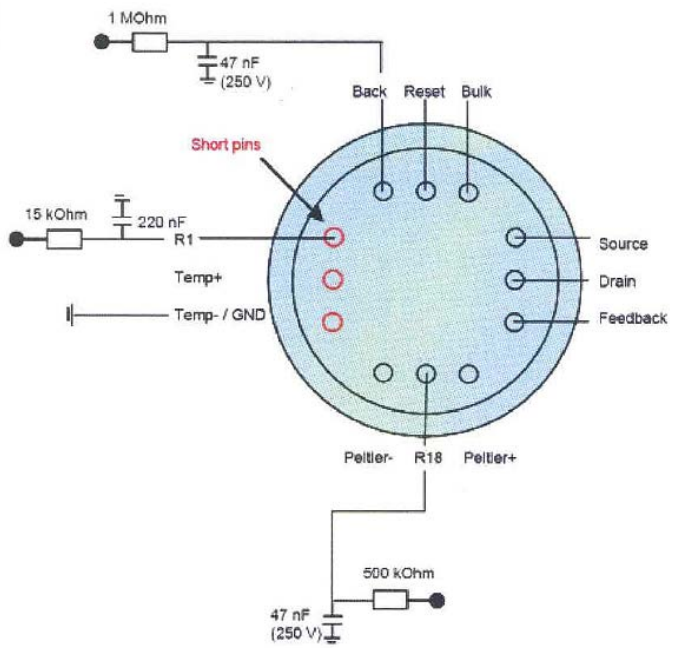


Figure 3.15: Schematic representation of SDD with HV bias filtering requirement (courtesy: KETEK GmbH).

These high voltage biases are generated using a voltage multiplier-based circuit having eleven stages of voltage multiplication with the first stage being an RC oscillator with a frequency of about 100 kHz.

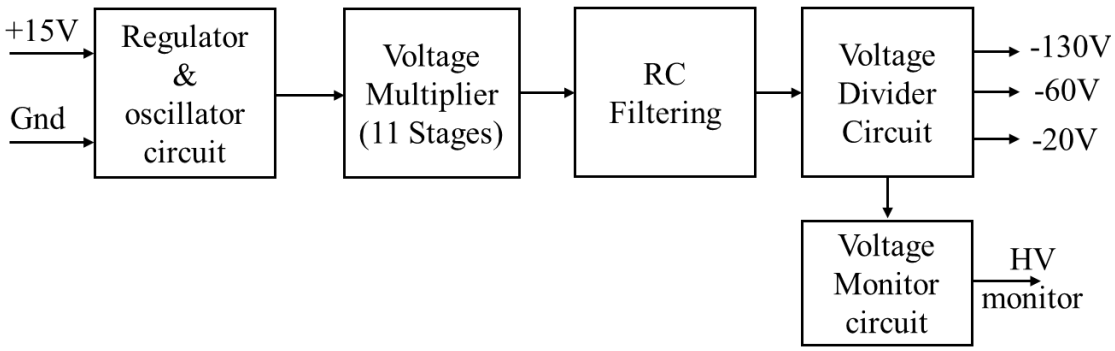


Figure 3.16: The block schematic of the high voltage generation circuit.

Each stage of the voltage multiplier uses a Schmitt trigger buffer with a diode capacitance combination for voltage multiplication. Hex Schmitt trigger inverter HC40106 IC is used for this purpose and the voltage multiplication is carried out with 15 V bias input. Three different voltages required for SDD operation are derived using a resistive voltage divider. The high voltage bias and the filtering requirement are listed in Table 3.2.

Table 3.2: SDD HV bias voltage, current and filtering on each HV line.

SDD Ring	Typical voltage	Filter requirement
R1 Voltage, Current	-20V ± 1V, 10 μA	15 kΩ, 220 nF
R_{18} (Rx) Voltage, Current	-130V ± 5V, 10 μA	500 kΩ, 47 nF (250 V)
R_{BACK} Voltage, Current	-60V ± 2V, < 1 nA	1 MΩ, 47 nF (250 V)

3.2 Pulse height measurement techniques

A Pulse-Height Analyzer (PHA) is a device that counts the pulses and measures their amplitude coming from a radiation detector. There are several methods for measuring pulse height. The peak hold detector-based approach, which keeps the peak of the semi-gaussian-shaped pulse form shaping amplifier output on hold until the ADC conversion time, is one of the conventional techniques. Digital pulse processing (DPP), a well-known method, samples the CSPA output using a high-speed ADC and processes it using an FPGA or DSP. The shaping amplifier output can be discharged linearly to measure the height of the pulse using the linear discharge technique (Amplitude of the Pulse is proportional to the discharge time). The pulse width modulation method, in which the pulse width is directly proportional to the input pulse amplitude, is also used to quantify pulse amplitude.

The identical front-end hardware, which comprises an SDD detector, CSPA, high voltage (HV) bias, and Peltier cooling circuit, is utilized to evaluate the performance of developed approaches. Using a Schmitt trigger-based multiplier circuit, the high voltages are produced. The thermistor value is monitored in order to keep the detector temperature at -35 °C at ambient temperature. Most of the time, the performance of the front-end component is unaffected by the back-end. For all the peak height measuring methods back-end hardware and FPGA algorithm is designed. In the next sections, all peak height measuring methods are thoroughly examined before being compared to the suggested approach. One of the primary factors used for technique comparison is spectral resolution. The spectra are measured by the full width at half maximum (FWHM) of the line at 5.9 keV and are obtained using a ^{55}Fe radioactive source available at lab.

3.2.1 The conventional peak detection technique

Usually, Soft X-ray spectrometer is designed in two parts front-end electronics and back-end electronics (processing electronics) package. The detector, CSPA, shaping amplifier, controller for the Peltier cooler, and high voltage supply to bias the detector make up the front-end electronics package. Back-end electronics will contain the semi-gaussian peak detection method and other processing.

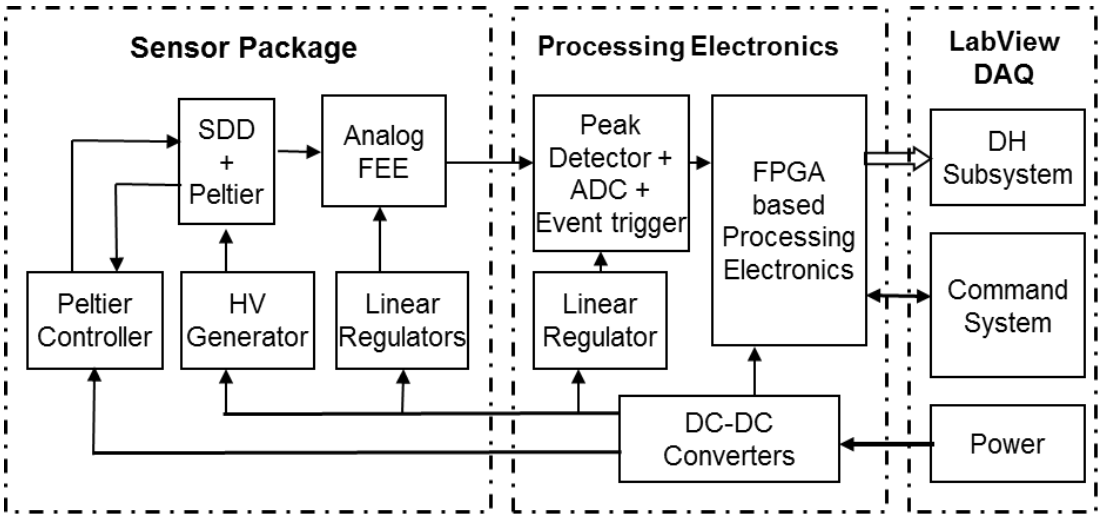


Figure 3.17: Block diagram of the peak detector-based spectrometer's front-end and back-end circuits.

The step pulse will be transformed into a semi-gaussian pulse with a 5μs peaking period by the CR-RC-RC filter. Figure 3.24 displays the spectrometer's block diagram. The peak detection, analogue to digital conversion, and further event processing are all started by the event trigger generator when an X-ray interacts with the detector.

3.2.1.1 Peak hold detector

A peak detector circuit receives the output of the shaping amplifier and holds the peak amplitude value of the pulses until the analogue to digital process time. The design makes use of the hybrid peak detector PH300 module manufactured from AMPTEK. This is a hybrid module that is directly interfaced with the FPGA to initiate the peak detection and hold the peak value until the A/D conversion. Peak detector PH300 is having the following features

1. Low droop rate (10 n V /ms)
2. High speed (250 ns rise time)

3. Low power consumption (36 mW)
4. Fast discharge

The peak detection and holding of peak value for one semi-gaussian signal are shown in Figure 3.25. The peak detector PH300 operation is controlled through FPGA. FPGA allows the input signal into the peak detector as and when event trigger occurs by activating the GATE input. PH300 provides active low digital output PKDT indicating that the peak detector has detected the peak value of the input signal. On detecting the active low PKDT, FPGA closes the GATE and starts the analog to digital conversion process and data readout from the analog to digital converter (ADC). Once the conversion is over, the peak signal amplitude is discharged by making RAMP and DUMP signals active low and this is called fast discharge mode. PH300 takes 1 μs for the discharge. This process repeats for every event and the dead time for each event conversion is the sum of pulse shaping time (peaking time), analog to digital conversion time, signal readout time from the ADC to FPGA (serial or parallel) and the peak detector discharge time (Figure 3.27).

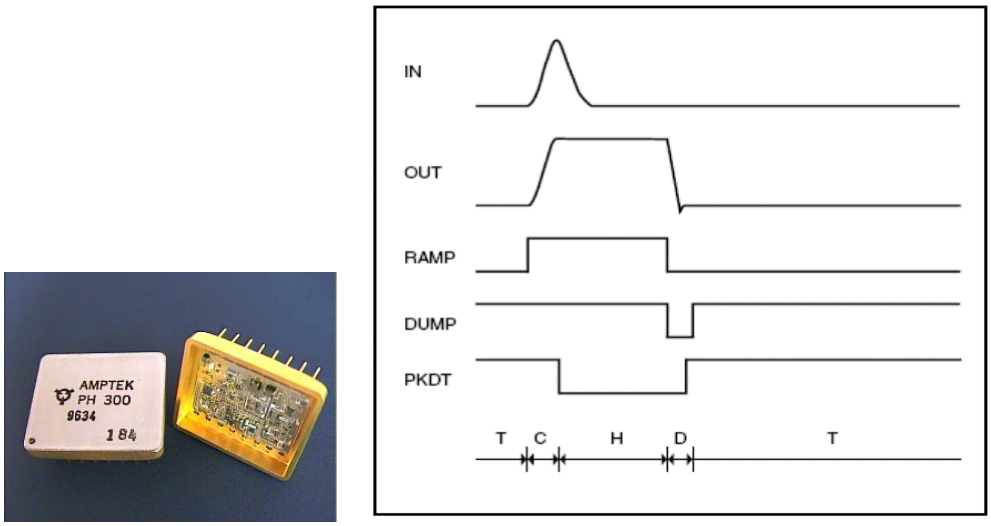


Figure 3.18: AMPTEK make PH300 Hybrid peak detector module(left), Peak detector operational timing diagram for peak hold and discharge (right) [47].

3.2.1.2 Analog to digital converter (ADC)

The analog to digital conversion is performed using a 12-bit serial ADC called ADC128S102, which takes conversion time of 1 μs. This ADC accepts input signal voltage up to 5V. The reference voltage required for this ADC is supplied externally through regulator AD584. The 12-bit digital output is readout using 10 MHz clock. On

the occurrence of the X-ray event, FPGA initiates the analog to digital conversion by generating required control signals for ADC, after 880 ns, 12-bit data is read out and the spectra is made using 12-bit data.

3.2.1.3 Experimental setup and result

Figure 3.26 shows the designed spectrometer test setup, which consists of a sensor package and processing electronics package. A data acquisition system built on LabVIEW is used to collect the data. This pulse height analyzer (PHA) technique uses a ^{55}Fe radioactive source to illumine the detector and obtains a resolution of ~157 eV at 5.9 keV. Figure 3.27 displays the histogram for the radioactive source ^{55}Fe (bottom).

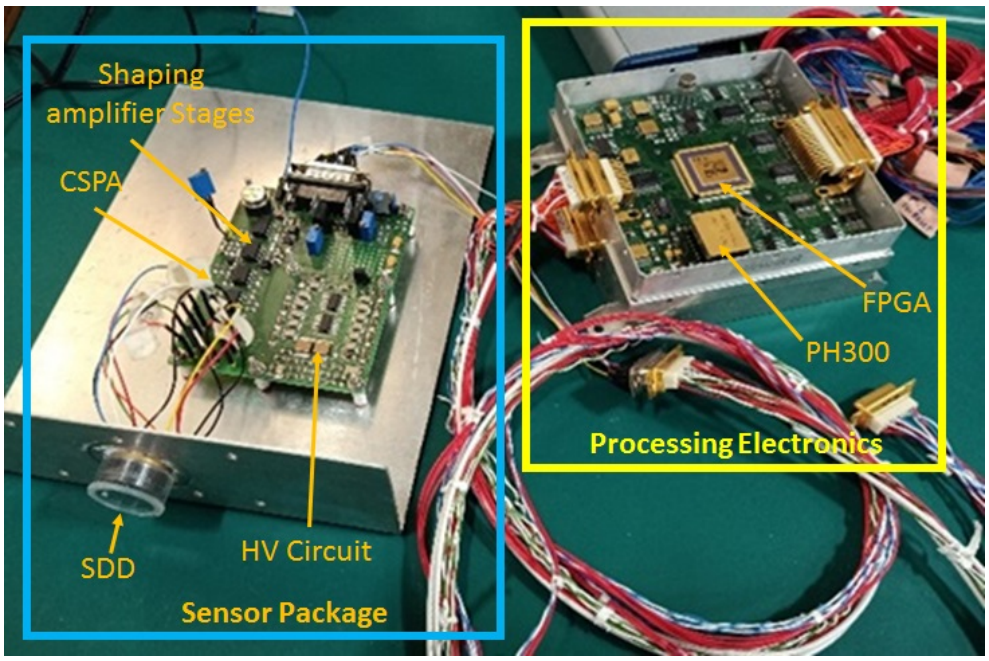


Figure 3.19: X-ray spectrometer set up utilizing peak detector-based processing circuitry and a front end compatible with silicon drift detectors (SDDs).

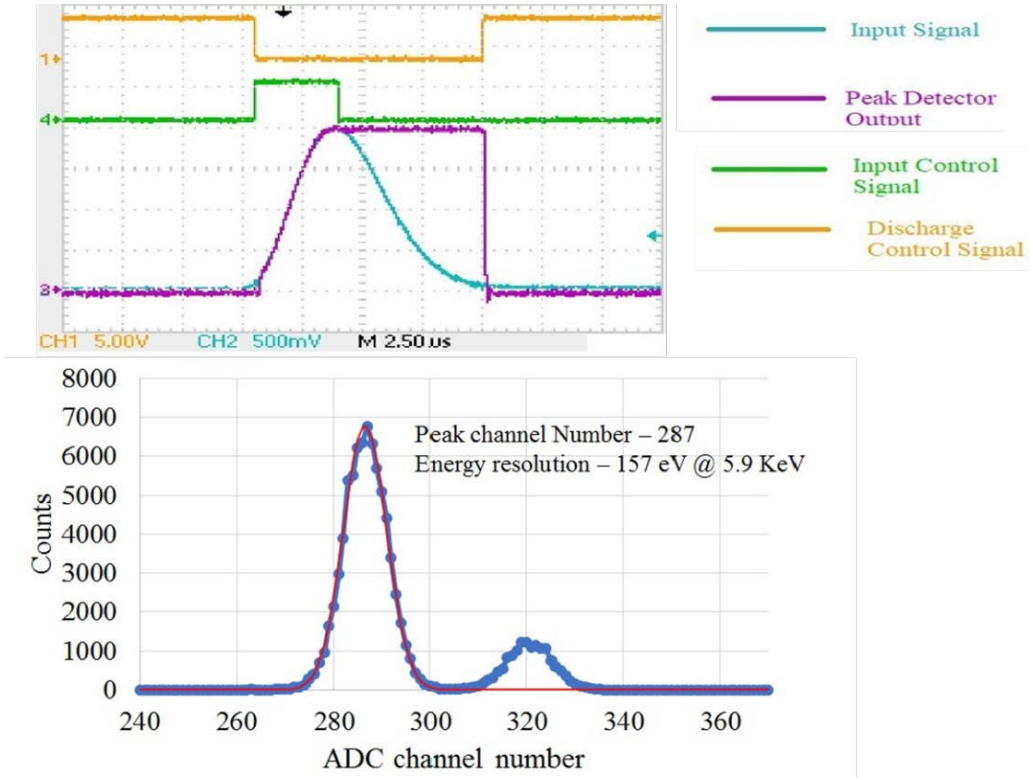


Figure 3.20: Operation signals for a peak hold detector in operation (top), spectra from a ^{55}Fe source produced using a traditional peak detection method. (bottom).

Using a red line as an overlay, Figure 3.27's first peak of spectral data is fitted using a Gaussian function. The fitted peak's FWHM is ~157 eV at 5.9 keV. The peak ADC channel of first gaussian fitted peak is 287. During experiment, The SDD detector is cooled at -40°C. The peaking time or pulse shaping time of semi-gaussian pulse is 5 µs.

3.2.2 Real-time pulse shaping via digital pulse processing

Signal filtering operations that are not achievable with conventional analogue signal processing can be implemented using digital pulse processing. The typical peak detection approach described in the previous section has the drawback of performing poorly at higher count rates, which is an issue that is addressed by this methodology. As demonstrated in Figure 3.28, the shaping amplifier and peak detector components are replaced in digital pulse processing by the faster digitizer with greater sampling rates.

Figure 3.21: Block diagram of the digital pulse processing.

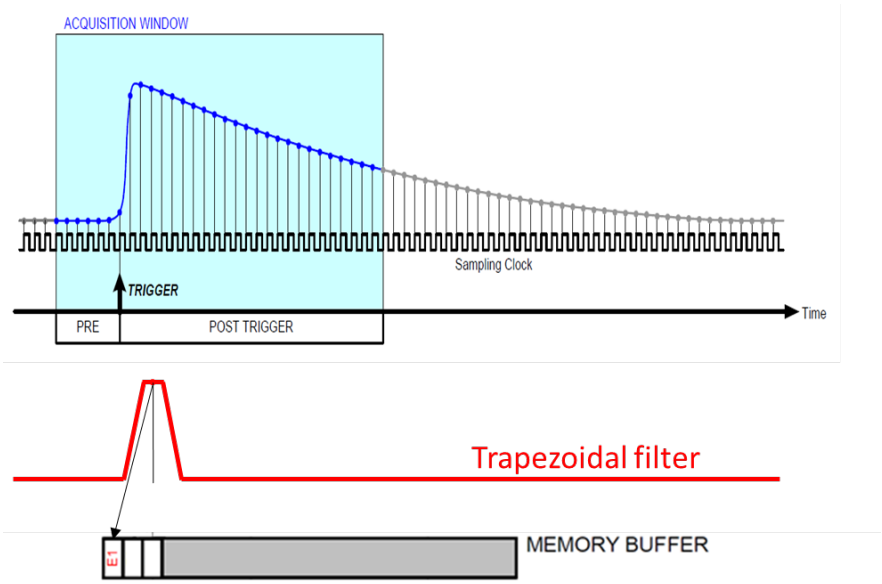


Figure 3.22: Fast ADC is used to digitize the input signal from the CSPA (blue), and samples are then saved in internal memory of the FPGA. (top), Red represents the output of a trapezoidal wave with a flat top. The height of the output pulse is inversely proportional to the height of the input pulse [103] .

Moving average filters are the most basic digital filters, however they only partially reduce noise, making them inadequate for pulse height analysis when compared to analogue pulse shaping. The low-frequency noise components of the shaped pulse have a lengthy tail and have not yet been reduced. The trapezoidal filter is a more widely used kind of digital filter for detector pulse processing. On reaching its full width, the trapezoidal filter output pulse exhibits a sudden termination. When the peaking time is less than the collecting duration of a portion of the charge carriers, the flat top area of the trapezoidal pulse is useful for improving the detector charge carrier collection. As illustrated in Figure 3.30, a block schematic may be used to construct the equations for the trapezoidal filter.

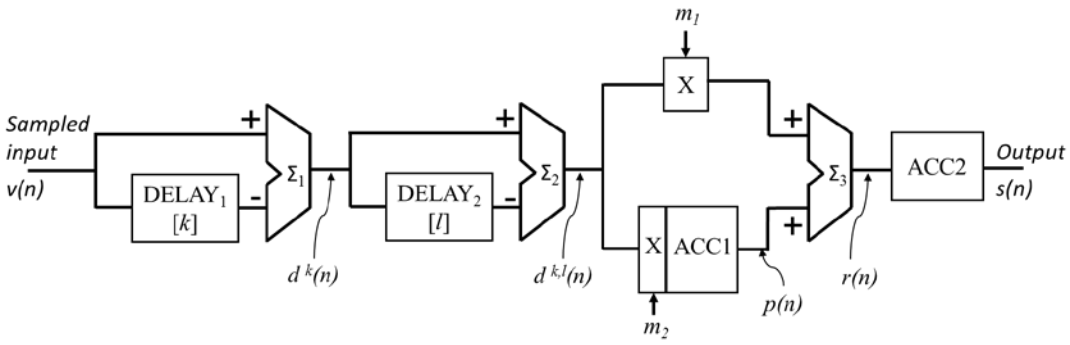


Figure 3.23: Digital trapezoidal shaper block diagram. [104].

In Figure 3.30 The elements are Σ -an adder/ subtractor, DELAY*n* - a delay pipeline, X*n* -a multiplie, ACC*n* - an accumulator. The equations to convert digitized exponential pulse v(n) into a symmetrical trapezoidal pulse *s(n)* are given as [104]

$$d^{k,l}(n) = v(n) - v(n-k) - v(n-l) - v(n-k-l) \quad (3.5)$$

$$p(n) = p(n-1) + d^{k,l}(n), \quad n \geq 0 \quad (3.6)$$

$$r(n) = p(n) + M\, d^{k,l}(n), \quad (3.7)$$

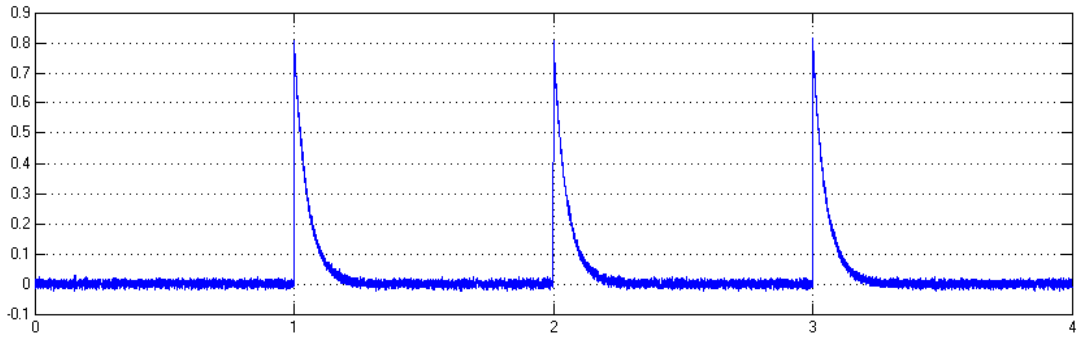
$$s(n) = s(n-1) + r(n)^{k,l}, \quad n \geq 0 \quad (3.8)$$

Where, for n < 0, *v(n), p(n),* and *s(n)* are equal to zero. The parameter *M* is provided by and solely depends on the exponential pulse's decay time constant and the digitizer's sample period T_{clk}.

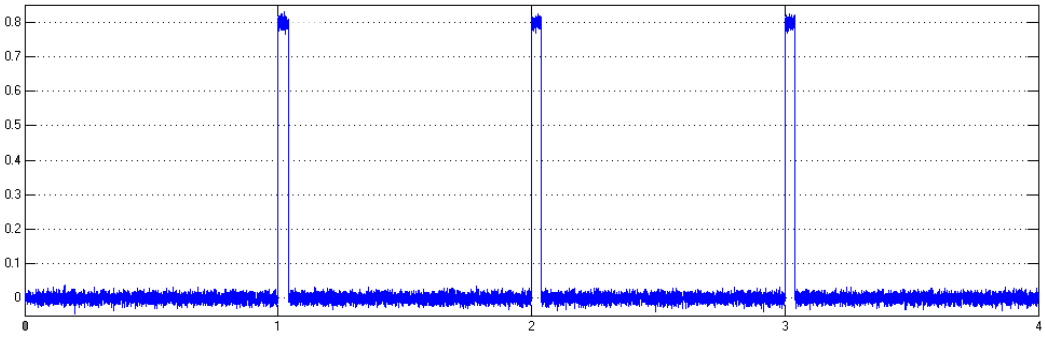
$$M = \frac{1}{e^{(T_{clk}/\tau)} - 1} \quad (3.9)$$

It is simple that by wiring two Delay subtract units in series, the method described by Eq. (3.16), may be implemented. One of the units' delay pipelines has a depth of *k*, whereas the depth of the pipeline in the other unit is *l*. The sequence of connection between the units is irrelevant since each of these units forms a linear time-invariant system. Under such circumstances, the duration of the rising (falling) edge of the trapezoidal shape is given by the smaller value of *k* and *1*(min(k, 1)) and the duration of the flat part of the trapezoid is given by the absolute value of the difference between *k* and *1* (*abs(1- k)*) [104].

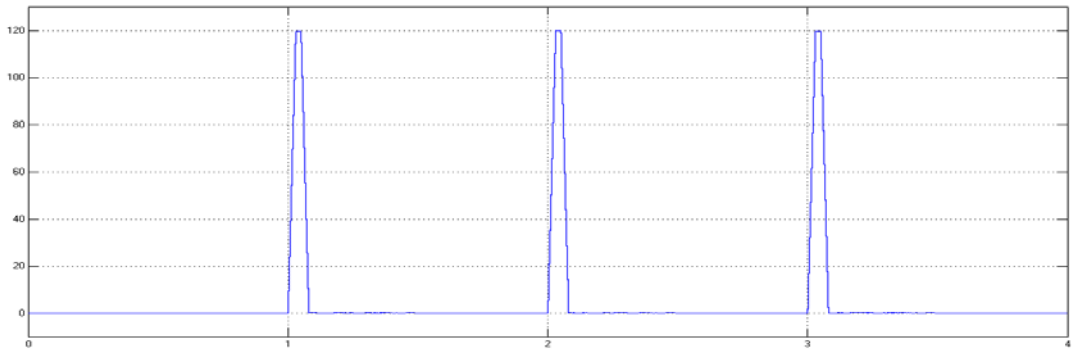
The MATLAB simulation is carried out to study the digital pulse processing equations. The equations (3.16) to (3.19) are implemented in stages suing Simulink environment of MATLAB and output were observed with scope. The simulation output of Simulink simulation is shown in Figure 3.31.



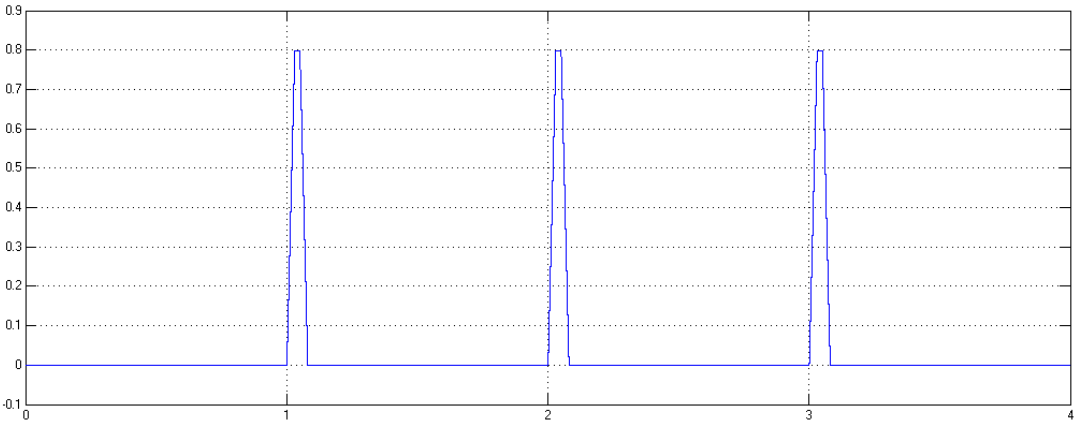
(a) Exponential function –input for the simulation



(b) Stage-1 output $d^k(n)$



(c) Output r(n) - Shape is a trapezoid with significantly increased SNR comparing to the input



(d) Stage-4 Output s(n) – Noise removed

Figure 3.24: The MATLAB simulation results for the digital trapezoidal shaper.

The calibrated and better-resolution optimized version of the digital pulse processor is offered on the commercial sector. The investigation compared the outcomes of all created methods with a reference system utilizing a commercially available multichannel analyzer (MCA). Although the hardware was created for digital pulse processing, as illustrated in Figure 3.32, other factors including FPGA use, mass, power, and size were also taken into consideration.

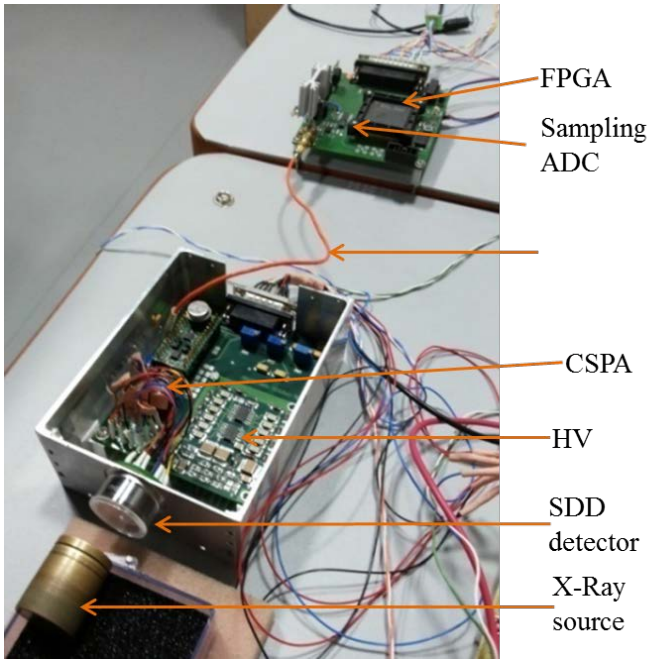


Figure 3.25: FPGA board with digital pulse processing interfaced with setup for SDD detector front-end.

The CSPA output which is a ramp signal is passed through CR stage and given to the FPGA card for further processing which has an algorithm for trapezoidal pulse filtering. The 12-bit sampling ADC AD9235 is used which has 1V internal reference. The AD9235 is operated at 20MHz sampling rate to sample the input exponential pulse. In FPGA, the equation for a trapezoidal filter is implemented as shown in block schematic Figure 3.30.

To visualize the trapezoidal filter output in analog form the digital output data from FPGA is given to DAC. The DAC output is shown in Figure 3.33. The FPGA implementation for pulse processing is shown in Figure 3.34 which has many sub-modules like moving average, baseline restorer, peak find, clock divider, ADC control, DAC control generator, DSP logic, and internal SRAM blocks.

Figure 3.26: CRO screenshot for CSPA output (blue) and Trapezoidal filter output through DAC (orange).

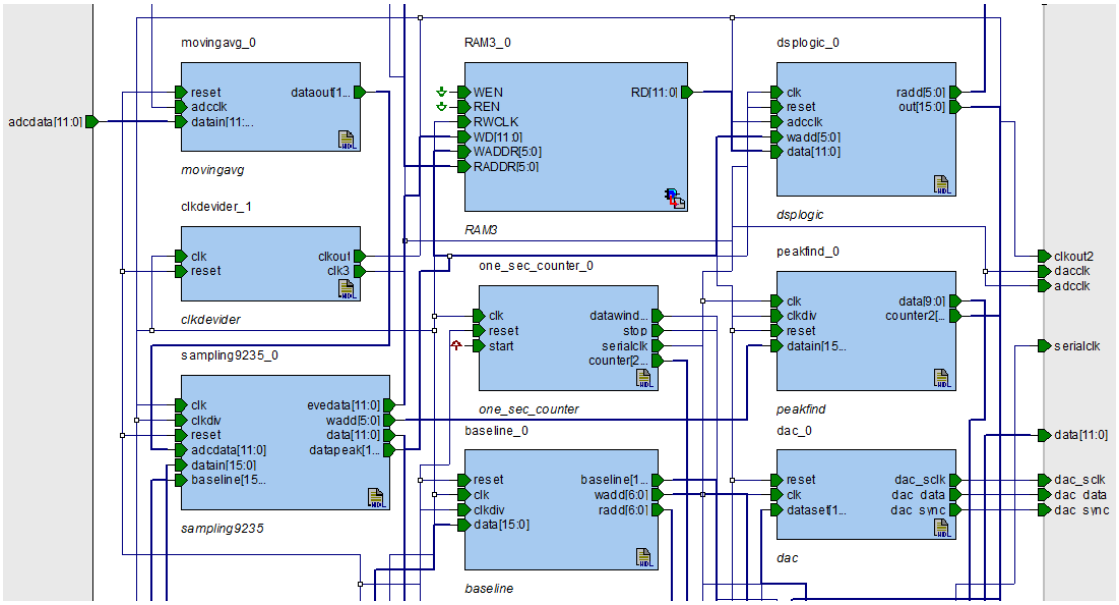


Figure 3.27: FPGA implementation for digital pulse processing using libero smart design tool (For Microsemi make FPGAs).

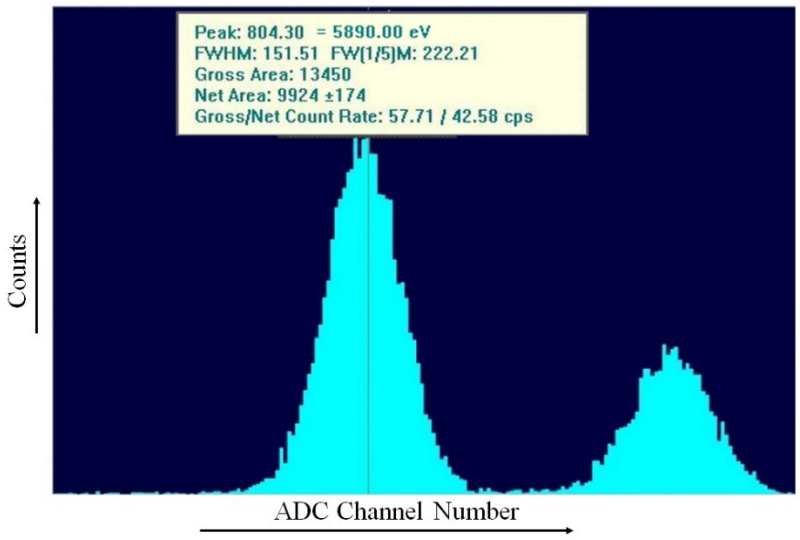


Figure 3.28: The ^{55}Fe spectral data was collected utilizing the digital pulse processing method of the ORTEK MCA.

The experiment uses the commercially available ORTAC make MCA, which relies on digital pulse processing and has its own software for data visualization. Figure 3.35 displays the data collected using a multichannel analyzer (MCA). The data is collected by back-end ORTEC make MCA illumination of the ^{55}Fe source using the same front-end as described in Section 3.3.1.3. The data collected indicates an energy resolution of ~152 eV at 5.9 keV. Additionally, data is collected using a digital pulse processing system that has been created in lab, with an energy resolution of around ~200 eV at 5.9 keV. The CSPA output, which has a very low amplitude, is sent to another card for further processing, which degrades performance and adds noise. Additionally, the system's performance is constrained by the ADC's sampling rate. The processing speed of the trapezoidal filter is further constrained by the 40 MHz working clock frequency of the FPGA. The 13-bit ADC, DSP processor, and 80 MHz FPGA clock frequency are features of the commercially available MCA. These factors contribute to the commercially available MCA's superior performance over the designed DPP.

3.2.3 Linear Discharge technique

The Wilkinson ADC concept underlies the linear discharge method for measuring the pulse height of radiation detectors [105]. A capacitor and an analogue switch that is utilized for charging and discharging are the two main components of the design. The discharge period is proportional to the analogue voltage at the operational

amplifier's input (op-amp). By comparing the shaping amplifier output with a set reference value of 50 mV, the comparator creates the trigger pulse. After a given amount of time, which corresponds to the signal peaking time, the FPGA will change the switch position. A longer discharge time is desirable to provide a wider energy range and higher resolution.

Figure 3.36 illustrates the concept of the analogue switch and capacitor charging. In default mode, the switch will be connected to shaping amplifier output. When the shaping amplifier output gives the pulse, the comparator will generate the trigger. As the switch is connected to an analog output signal from the shaping amplifier, the capacitor (C) is will remain in charging mode as shown in Figure 3.36 (a). The analog switch will allow the charging of the capacitor till the peak amplitude. After completion of charging mode which is fixed duration based on the pulse peaking time, the FPGA will change the switch position to the constant current source as shown in Figure 3.36 (b). In this case, the capacitor (C) will be in discharge mode with a constant current path which will linearly discharge the capacitor.

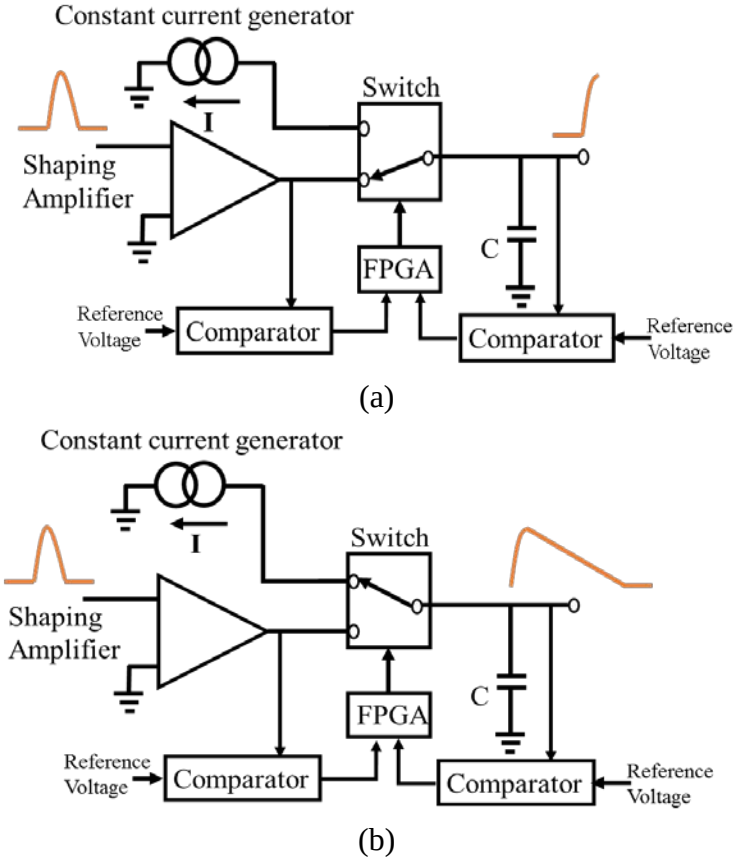


Figure 3.29: Peak detection and linear discharge circuit concept. (a) Capacitor (C) is in charging mode with analog input signal coming from shaping amplifier. (b) Capacitor (C) in discharge mode with constant current path (bottom).

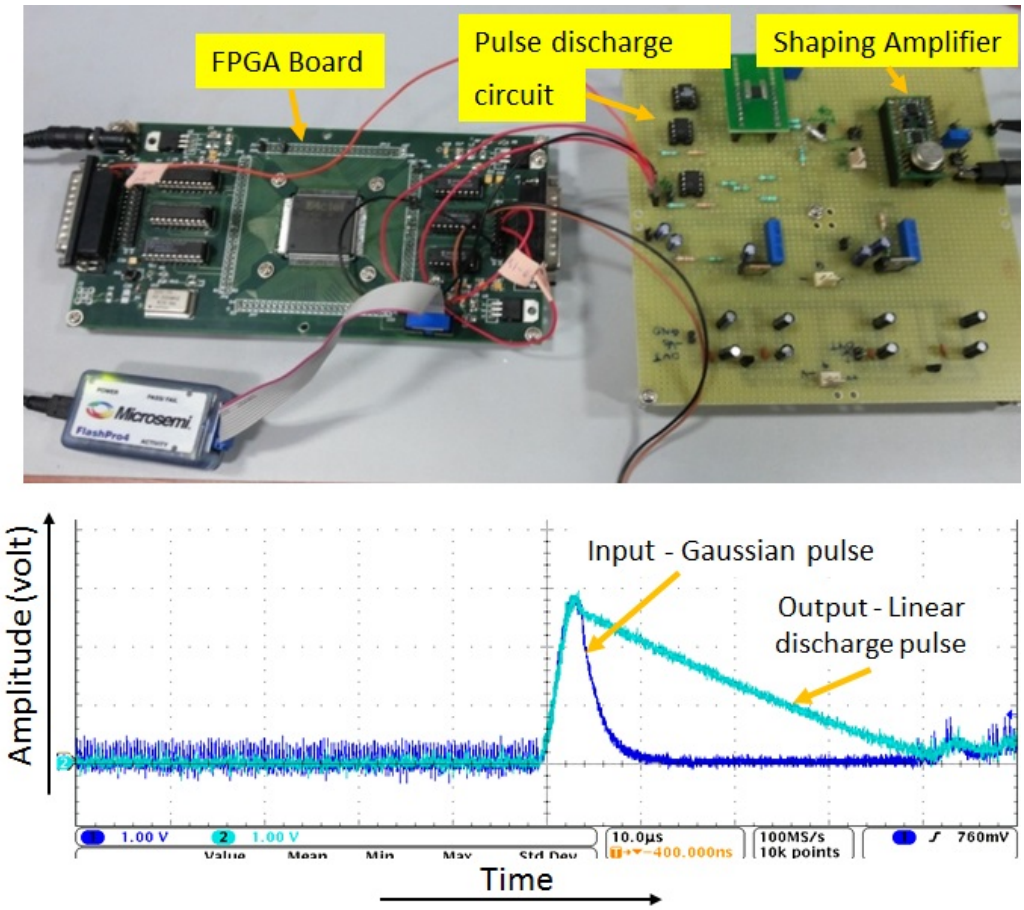


Figure 3.30: Hardware setup for a pulse linear discharge circuit (top), oscilloscope waveform displaying the output of a shaping amplifier (dark blue) and a linear discharge pulse (light blue). The Y-axis has a 1 V grid size, whereas the X-axis has a 10 s grid (bottom).

As seen in the top panel of Figure 3.37, the peak detection and linear discharge circuit were developed. The lower portion of Figure 3.37 displays the discharge output coupled with the shaping amplifier output. Up until the peak is reached (dark blue), the light blue output follows the shaping amplifier input. After that, the output is discharged linearly using the current source to control the decay constant. The implementation of another comparator circuit uses reference and discharge output voltages as inputs. The FPGA receives the pulse from the comparator and uses it to calculate the discharge time, which is directly proportional to the length of the pulse. Using PLL, a counter with a 320 MHz clock frequency is constructed in the FPGA and has a resolution of 3.125 ns for measuring pulse width. The experiment was run with the same front-end as described in section 3.3.1.3 and a ^{55}Fe source, yielding an energy resolution of about ~300 eV at 5.9 keV.

3.2.4 Pulse width modulation (PWM) technique

One well-known and often used technique for converting a DC signal to digital is pulse width modulation (PWM). Here, the pulse height is measured using the same method. The peak detector and analogue to digital (A/D) converter can be swapped out using this technique [106]. This approach will be useful if a lot of detectors are utilized since the analogue to digital converter and peak detector take more space and power. Figure 3.38 depicts the basic block diagram for PWM operation.

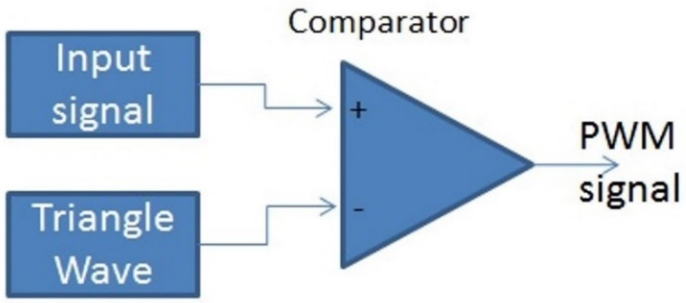


Figure 3.31: Pulse width modulation basic concept.

PWM is usually generated by comparing the input signal with a higher frequency triangle wave signal. The peak height resolution of the system is mostly depends upon the frequency and linearity of the triangle wave. As shown in Figure 3.39 To produce the triangle output, an integrator configuration of the op-amp is used. This strategy is based on the obvious fact that linear ramps are produced when a constant voltage is integrated. A Schmitt trigger feeds the integrator's output back into the inverting input. The Schmitt trigger's input threshold voltages are intended to alter the state according to the required peak voltages of the output triangle wave.

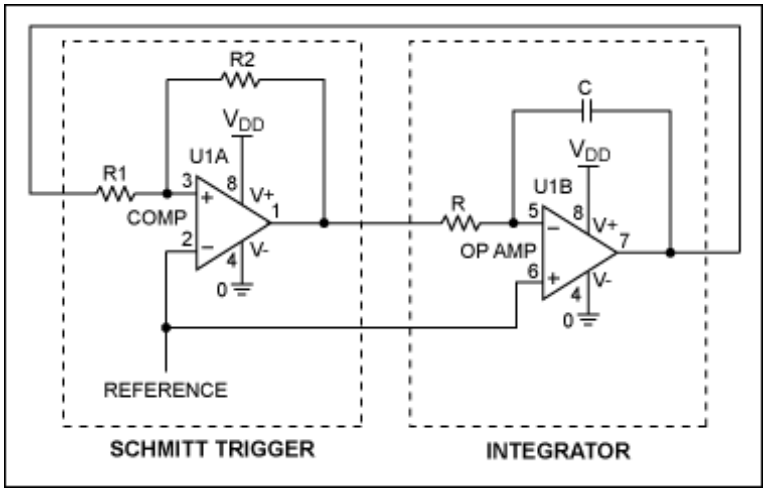


Figure 3.32: Design concept for a basic triangular-wave generator [107].

Hardware for producing the 500 kHz triangle waveform is created as illustrated in Figure 3.40 and uses the op-amp integration circuit LM6172, which has a 3000 V/µs slew rate. Due to the limitation of op-amp operation, above 500 kHz frequency the triangle wave is non-stable and has more non-linearity. The triangle wave output from the integrator is compared with a shaping amplifier output which is a semi-gaussian pulse. The AD8561 comparator is used because it has 7 ns propagation delay. The output pulse from the comparator is shown in Figure 3.42.

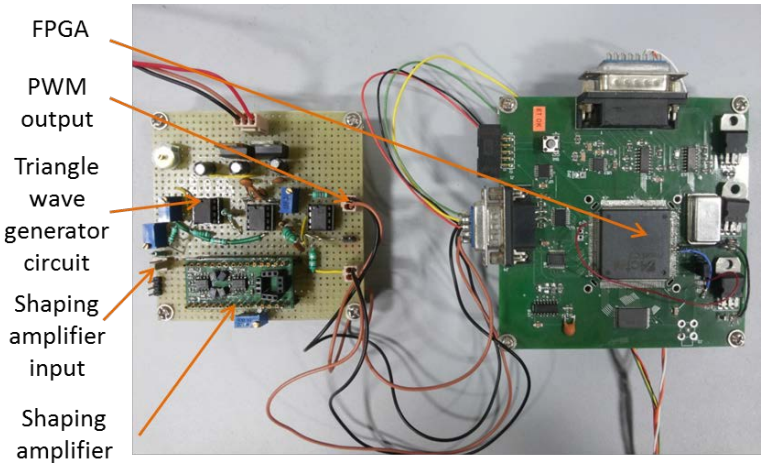


Figure 3.33: PWM hardware and FPGA interface.

The hardware is developed for PWM generation and interfaced with the FPGA card. The CSPA output is given to the PWM hardware, which contains the shaping circuit, triangle wave circuit and comparator circuit. The FPGA implementation for PWM is shown in Figure 3.41.

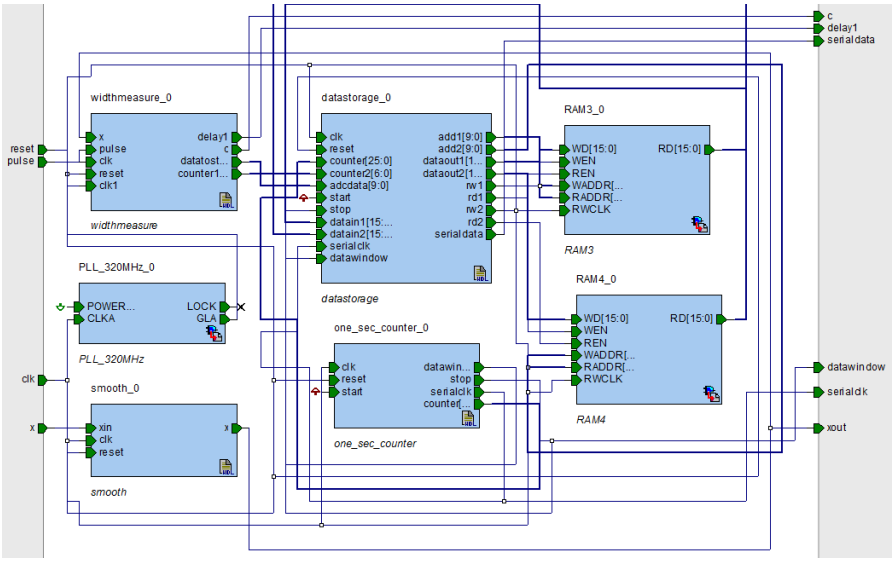


Figure 3.34: FPGA implementation of PWM algorithm, data storage and transfer using Libero smart design flow.

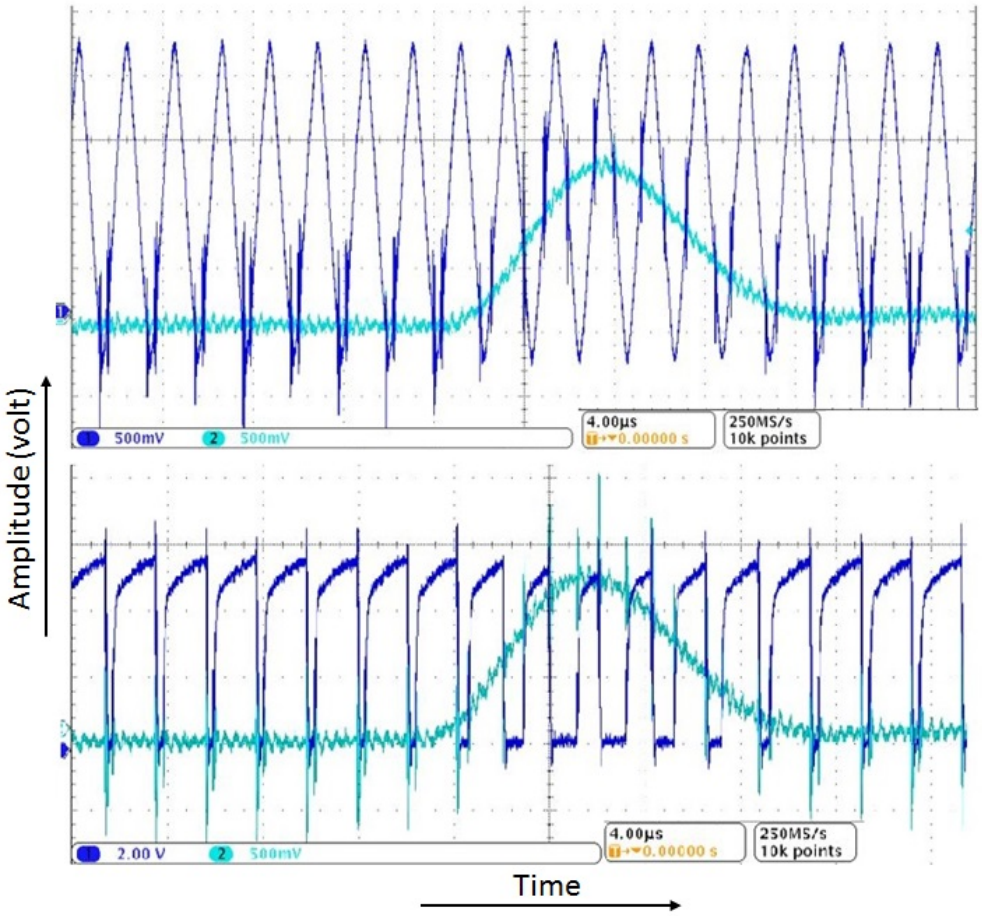


Figure 3.35: Triangle signal compared with input semi-gaussian pulse (top), PWM output with semi-gaussian input pulse (bottom).

Information about peak height in terms of pulse width is sent to the FPGA through the PWM output from the comparator. FPGA calculates the lowest pulse width, which corresponds to the semi-gaussian pulse's peak. Resolution for the pulse width measurements is 3.125 ns. The recorded pulse width data is transformed into a 256-bin histogram. The energy resolution ~300 eV at 5.9 keV is made possible by the silicon drift detector (SDD) and pulse width modulation circuit architecture. This approach can only be utilized for higher shaping time semi-gaussian pulses due to the instability and non-linearity issue of triangle wave at a higher frequency.

3.3 Summary

In this chapter, various parts of the radiation detector readout are explained in detail. The CSPA and shaping amplifier parameter derivations are shown. The front-end and various back-ends for SDD based X-ray spectrometer have been developed

using the commercial equivalent of space-qualified components. When the silicon drift detector (SDD) is cooled to -40°C with other subsystems at ambient temperature and the pulse peaking time of the shaping amplifier is 3 μs, it is demonstrated that the constructed front-end portion of the spectrometer delivers an energy resolution of 152 eV at 5.9 keV with the conventional digital pulse processing system. Different Pulse height measurement techniques were developed and tested with the same front-end electronics. By illumination ^{55}Fe X-ray source, the conventional peak detector technique shows ~157 eV energy resolution with 5 μs peaking time, Linear discharge methods shows ~300 eV energy resolution with 4 μs peaking time and PWM method shows ~300 eV energy resolution with 8 μs peaking time.

C H A P T E R – 4

4 IMPLEMENTATION AND RESULTS OF THE PROPOSED PULSE HEIGHT ANALYSIS METHOD

A novel approach is suggested as a replacement for the various peak height measuring approaches covered in the preceding chapter, in which the shaping amplifier output is sampled using a low sampling ADC. A comparison study and hardware implementation of several interpolation methods are done in order to interpolate the intermediate data. Based on error performance and resource use for the suggested approach, Lagrange's interpolation method is determined to be the most suited method. To determine the peak value of the analogue pulse, the peak search algorithm and Lagrange's interpolation method are implemented in the FPGA. Based on the experimental findings mentioned in this chapter, parameters like the shaping duration of the input pulse and the interpolation polynomial are evaluated and optimized.

4.1 Proposed pulse height analysis method

In the proposed method, the input analog signal is sampled using low sampling ADC and the interpolation is carried out on the ADC sample data. After interpolation, the maximum digital number corresponding to the analog pulse is the derived height of the analog pulse. A visual illustration of the interpolation performed for the semi-gaussian pulse, which is the shaping amplifier's anticipated output, is shown in Figure 4.1. In the left panel of subfigure (a) of Figure 4.1, the first five points (blue dots), including the two points that are just below the threshold limit and the three points that are over it, are shown. For points that are beyond the threshold limit, as indicated in the right panel of Figure 4.1's (a) panel, the 3-point interpolation (yellow dots) is applied. As indicated in (b) of Figure 4.1, the FPGA will move the array for the next real point after the first interpolation is finished and then apply interpolation for the second point. The subfigure (c) of Figure 4.1 depicts the continuous procedure for all of the spots. The interpolated points are spaced from the real positions by a set, evenly split gap.

The resulting points are not employed in the equation to find new points because they are not genuine values. As soon as it discovers the threshold value again, the FPGA will terminate the operation. However, to detect the pile-up events, the procedure is prolonged up to the threshold sample value. The process can also be terminated when the FPGA identifies the decreasing side of pulse sample values. Combining the entire interpolated data and determining the array's highest value are the following FPGA operations. This maximum sample value is used to create the histogram, which is known as an interpolated data histogram.

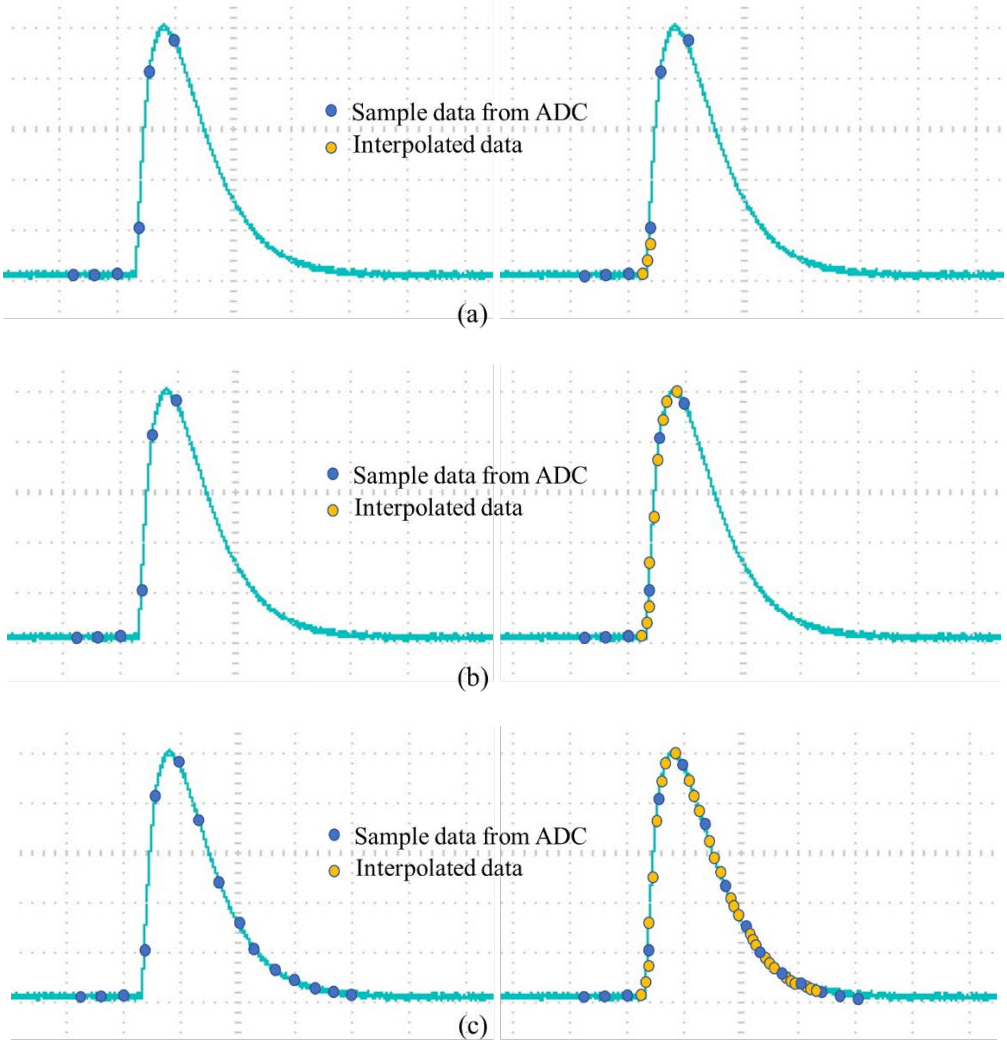


Figure 4.1: Illustration of the suggested interpolation method using a semi-gaussian pulse sampled at a low sampling rate (left part of a, b, c). after sample data interpolation (right part of a, b, c).

To achieve a better resolution few parameters are required to be optimized like the minimum required shaping time and minimum required interpolation points. These parameters are derived by experiments explained in upcoming sections.

4.2 Interpolation methods

The purpose of this section is to introduce interpolation and to evaluate the suitability of interpolation methods for the proposed method. In the proposed method, a low sampling ADC with 1 MHz is used to sample the shaping amplifier output. To interpolate the intermediate samples, an interpolation method must be implemented in FPGA. Between each pair of sample data, three additional points are interpolated. For instance, the ADC will deliver 10 samples for the pulse profile if the shaping time is 10μs. The peak height of the pulse cannot be determined accurately with only 10 samples. After interpolation, the sample size is raised to 40 in order to more precisely determine peak height. After interpolation, the sample with the highest peak value is identified, providing precise peak information.

Interpolation is used to calculate the unknown values of a non-linear or linear function based on a few accurate sample data points. Theoretically, more data points are needed for more accurate fitting. However, it is not feasible to develop a system that employs big data set points owing to the difficulties of hardware computation. The first task of the problem at hand is to sample the input pulse into equally spaced data points and then find the interpolated values. The following interpolation methods are designed and tried to determine the unknown peak value of the analog semi-gaussian pulse.

4.2.1 Nearest neighbor Interpolation

The simplest interpolation technique is nearest neighbor interpolation. This interpolation technique simply determines the closest data value at an integer position by rounding the expected position's value. The value of the interpolated function f at point *x* is given by below equation for the samples F(k).

$$f(x) = F\left(\lfloor x + \frac{1}{2} \rfloor\right) \tag{4.1}$$

The closest sample point to *x* is simply chosen. The greatest integer number that is less than or equal to *x* in this case is called the floor function, or ⌊x⌋. This results in an interpolated function that looks like a staircase. The function *f(x)* is defined on the entire real axis, but it is neither continuous (since it contains jumps) nor differentiable. Take a look at Figure 4.2's interpolated closest neighbor representation of the function f(x)=sin(x) as an example.

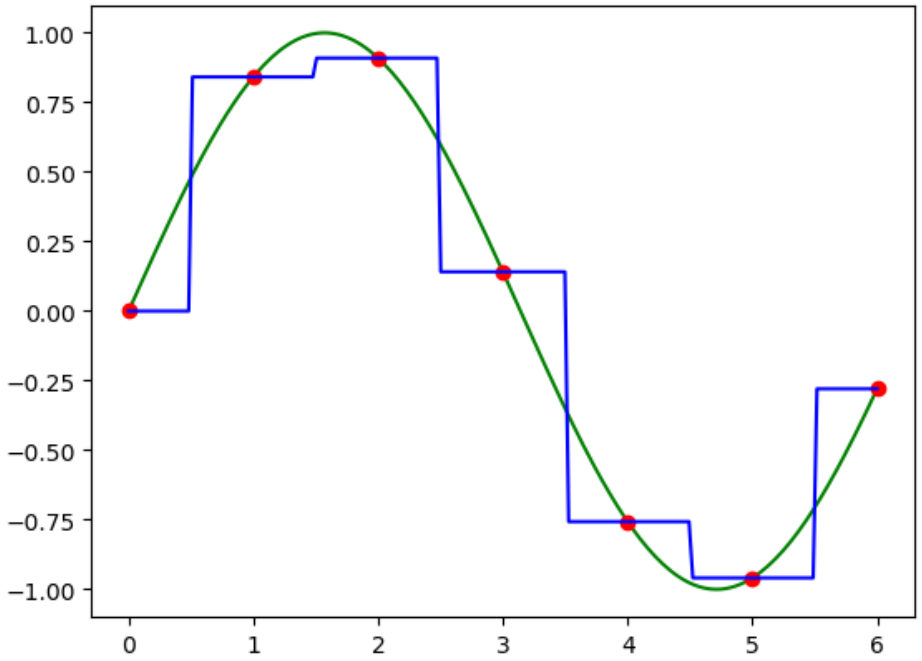


Figure 4.2: The continuous function f(x) = sin(x) in green, the sampled function in red and the nearest interpolated function in blue.

4.2.2 Linear Interpolations

The simplest interpolation technique for determining the value of a function between any two known values is the linear interpolation. A technique for fitting curves with linear polynomials is the linear interpolation formula. In essence, the interpolation method uses the collection of values to discover new values for any function. The linear interpolation formula is used to determine the unknown values in the table. Data forecasting, data prediction, mathematical and scientific applications, market research, etc. all employ the linear interpolation algorithm. The unknown values in the table can be found using the linear interpolation formula given by:

$$y = y_1 + (x - x_1)\frac{(y_2 - y_1)}{(x_2 - x_1)} \tag{4.2}$$

where,

- x_1 and y_1 are the first coordinates
- x_2 and y_2 are the second coordinates
- x is the point to perform the interpolation
- y is the interpolated value

Figure 4.3 shows the linear interpolation carried out for the function f(x)=sin(x) as an example.

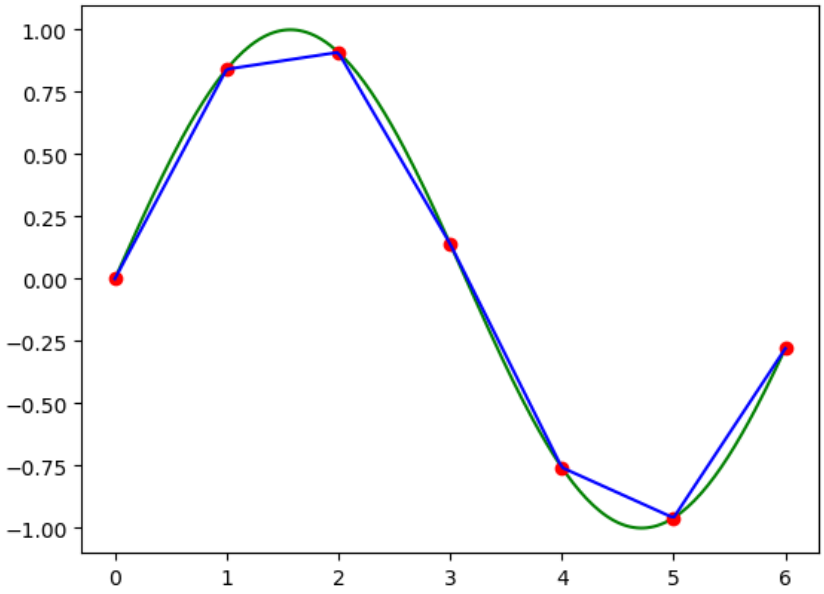


Figure 4.3: The continuous function f(x) = sin (x) in green, the sampled function in red, and the linear interpolated function in blue.

Despite being a straightforward interpolation technique, linear interpolation is frequently employed in practice. It is quick and easy to put into practice.

4.2.3 Lagrange's interpolation

The Lagrange interpolation formula may be used to locate a polynomial known as a Lagrange polynomial that assumes certain values at every location. Lagrange's interpolation is an approximation to f(x) using a N^{th} degree polynomial. Given n distinct real values X_1, X_2, … ,X_n and n real values Y_1, Y_2, … ,Y_n (not necessarily separate), there is a unique polynomial P with real coefficients satisfying $P(X_i) = Y_i$ for $i \in \{1, 2, \ldots, n\}$, such that deg(P) < n. The following is the Lagrange interpolation formula for a different order of polynomials:

$$y = f(x) = \frac{(x-x_1)(x-x_2)\ldots(x-x_n)}{(x_0-x_1)(x_0-x_2)\ldots(x_0-x_n)} y_0 + \frac{(x-x_0)(x-x_2)\ldots(x-x_n)}{(x_1-x_0)(x_1-x_2)\ldots(x_1-x_n)} y_1 + \cdots + \frac{(x-x_0)(x-x_1)\ldots(x-x_{n-1})}{(x_n-x_0)(x_n-x_1)\ldots(x_n-x_{n-1})} y_n \quad (4.3)$$

The equation (4.3) is simulated using MATLAB for the sinewave input data. The Figure 4.4 shows the 3^{rd} order LaGrange's interpolation carried out for a sample data taken for sinewave. For the other higher order interpolation methods explained in upcoming sections, the interpolation will look similar to Lagrange's interpolation as shown in Figure 4.4 but they have different error statistics.

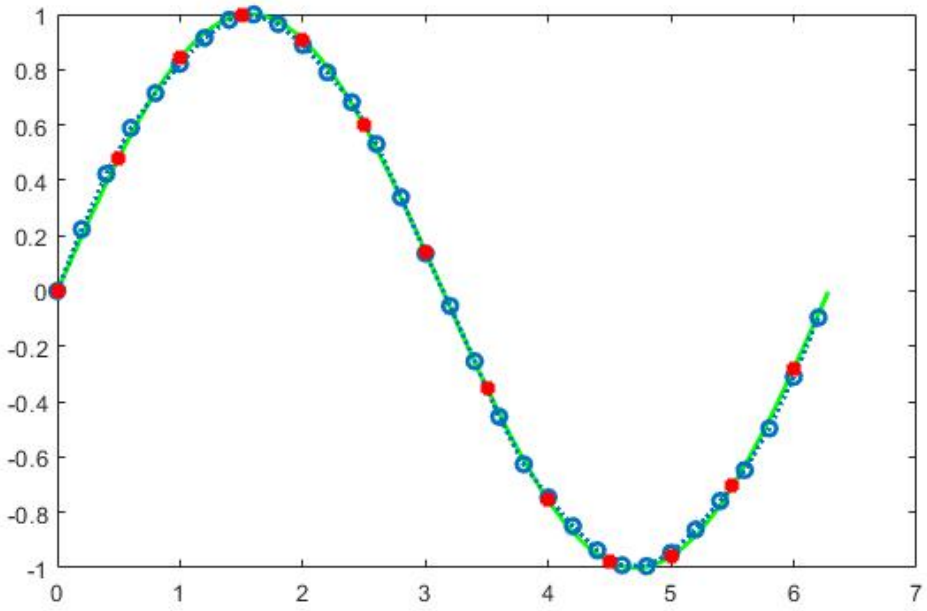


Figure 4.4: The continuous function f(x) = sin (x) in green, the sampled function in red, and the Lagrange's interpolated function in blue doted.

4.2.4 Newton Raphson Interpolation

The Newton-Raphson technique, commonly referred to as Newton's method, is a rapid approach to approximate the real-valued function f(x) = 0's root. It makes advantage of the idea that a straight line parallel to a continuous, differentiable function can serve as a rough approximation. A continuous, differentiable function f(x) needs to have a root, and you know the root you're seeking for is close to the point $x = x_0$. Then, according to Newton's approach, a more accurate approximation for the root is

$$x_1 = x_0 - \frac{f(x_0)}{f'(x_0)} \tag{4.4}$$

To get the requisite precision, this procedure may be done as many as necessary. In general, for every x-value x_n, the next value is provided by below equation.

$$x_{(n+1)} = x_n - \frac{f(x_n)}{f\prime(x_n)} \tag{4.5}$$

4.2.5 Cubic interpolation

Finding a curve that connects data points with a degree of three or less is possible through the use of cubic spline interpolation. The closest samples are utilized to determine the interpolated value in nearest neighbor and linear interpolation [108].

While in cubic interpolation we examine two data points on the left and two on the right in order to increase the accuracy of the fitting. We fit a cubic polynomial over the range of *x=k* to *x=k+1* to interpolate [109].

$$k \leq x \leq k+1:$$

$f(x) = a(x)^3 + b(x)^2 + c(x) + d$ to the 4-sample points *k−1, k, k+1*, and *k+2*.

For the 4 points, we have:

$$F(k-1) = a(-1)^3 + b(-1)^2 + c(-1) + d$$

$$F(k) = d$$

$$F(k+1) = a(1)^3 + b(1)^2 + c(1) + d$$

$$F(k+2) = a(2)^3 + b(2)^2 + c(2) + d \qquad (4.6)$$

Solving these equations for *a, b, c,* and *d* we get:

$$a = \frac{1}{6}\left(-F(k-1) + 3F(k) - 3F(k+1) + F(k+1)\right)$$

$$b = \frac{1}{2}\left(F(k-1) - 2F(k) + F(k+1)\right)$$

$$c = \frac{1}{6}\left(-2F(k-1) - 3F(k) + 6F(k+1) - F(k+2)\right)$$

$$d = F(k) \qquad (4.7)$$

4.2.6 Whittaker–Shannon interpolation

One way to create a continuous-time bandlimited function from a list of real values is to use the Whittaker-Shannon interpolation formula, often known as sinc interpolation. Similar to the Lagrange polynomial interpolation, the procedure is used. The key to polynomial interpolation is to identify a collection of component polynomials, each of which traverses a certain set of provided points. The component polynomials must also equal zero whenever there is a different point in order to be able to combine them all into a single polynomial that traverses the whole collection of

points. By doing this, it is ensured that the polynomials won't interfere with one another at the specified set of points when they are added together. Instead of using polynomials as the component, Whittaker-Shannon interpolation uses the Sinc function. The Sinc functions are periodic functions that are as below:

$$sinc(x) = \begin{cases} 1, & x = 0 \\ \frac{\sin(x)}{x}, & Otherwise \end{cases} \quad (4.8)$$

4.2.7 Neville's Algorithm for interpolation

An interpolation procedure called Neville's algorithm starts by fitting a polynomial of degree 0 across the point (X_k, Y_k) for k =1, ..., n, or $P_k(x) = Y_k$. Then, in a second iteration, pairs of points are fitted using P_i and $P_{(i+1)}$, resulting in P_{12}, P_{23}, and so on. A "pyramid" of approximations is produced by repeating the process until the desired outcome is obtained.

X_1: $Y_1 = P_1$

P_{12}

X_2: $Y_2 = P_2$ P_{123}

P_{23} P_{1234}

X_3: $Y_3 = P_3$ P_{234}

P_{34}

X_4: $Y_4 = P_4$

The result is

$$P_{i(i+1)\ldots(i+m)} = \frac{(x-x_{i+m})P_{i(i+1)\ldots(i+m-1)}}{(x_i-x_{i+m})} + \frac{(x_i-x)P_{(i+1)(i+2)\ldots(i+m)}}{(x_i-x_{i+m})} \quad (4.9)$$

4.3 Implementation of interpolation methods

All of the above-mentioned interpolation methods are simulated in this work, and hardware implementation is carried out using ADC, FPGA, and the LabVIEW environment. The initial finding from this research was that the precision of fitting rises as the number of interpolation points grows, reducing error [110]. The 3-point interpolation method is used to compare all of the above interpolation methods.

4.3.1 FPGA Implementation

FPGAs have found lots of applications in electronics engineering because of their customizable and programmable nature. In real-time mode, FPGA can perform basic mathematical operations such as addition, subtraction, multiplication, and division [111]. In order to prevent overflow and erroneous measurement, the best bit size consumption for each operation must be identified because the FPGA employed in this study uses fixed-point operations. By allowing customized bit sizes for data for different mathematical operations, fixed point operations can be speed up. However, the output may become saturated if the bit size is incorrectly specified or the high and low values are not taken into account.

In the present work, National Instruments (NI) USB6343 and A3PE1500 FPGA with 1.5 Million gates are used. Given the restricted resources available, the code for FPGA implementation should be created to use least amount resources as possible. Additionally, temporal restrictions must be taken into account. The FPGA clock frequency is set to 40MHz for the base clock. Any mathematical action must be viewed as a special instance of single-cycle timed loops with a slower clock speed if it cannot be performed inside the time bound of this clock speed. Wherever possible, a reduced clock rate was used in the algorithms mentioned above. The following sections provide a summary of resource utilization for various algorithms on FPGA.

4.3.2 Experimental Setup & Validation

This section outlines the experimental setting used to assess how well the piecewise interpolation methods utilized performed. Figure 4.5 displays the experimental setup's block schematic. The same number of samples and interpolation order were used to provide a common platform for comparing the efficiency of various interpolating methods based on fitting accuracy.

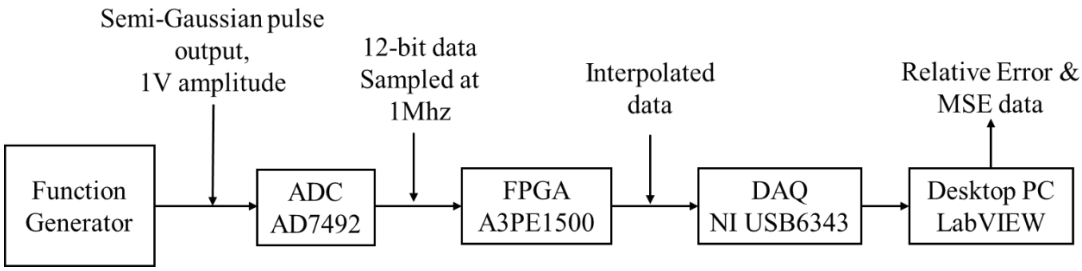


Figure 4.5: Experimental scheme for Relative error (RE) measurement

The MATLAB code is utilized to produce the semi-gaussian pulse profile data, and the same data is also used to program the function generator. While programming the function generator to have a varied duration between two semi-gaussian pulses, the data is repeated at random in a text file. Figure 4.6 displays the function generator's semi-gaussian output and the control signal (CONV) for the ADC. The semi -gaussian pulses are having 1 V peak amplitude.

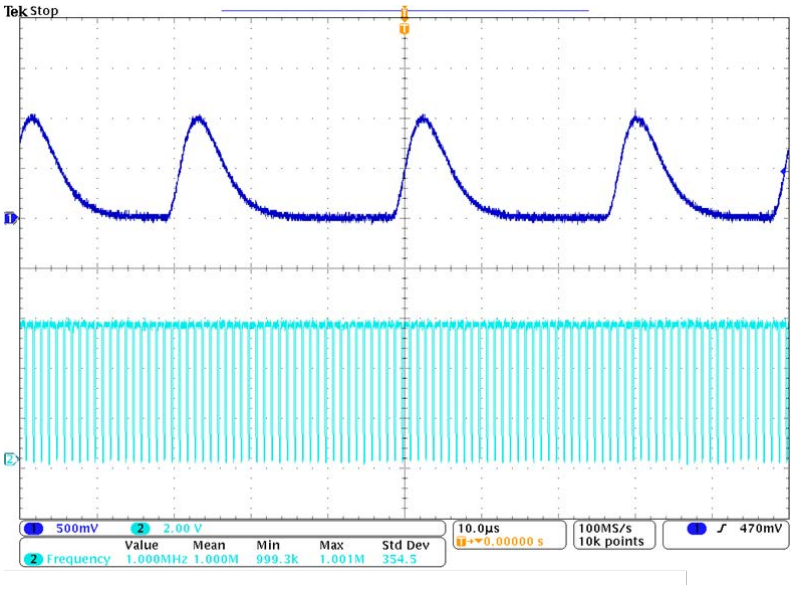


Figure 4.6: Waveform obtained using an oscilloscope showing semi-gaussian pulse from function generator output (dark blue) and convert start pulse for ADC from FPGA (light blue).

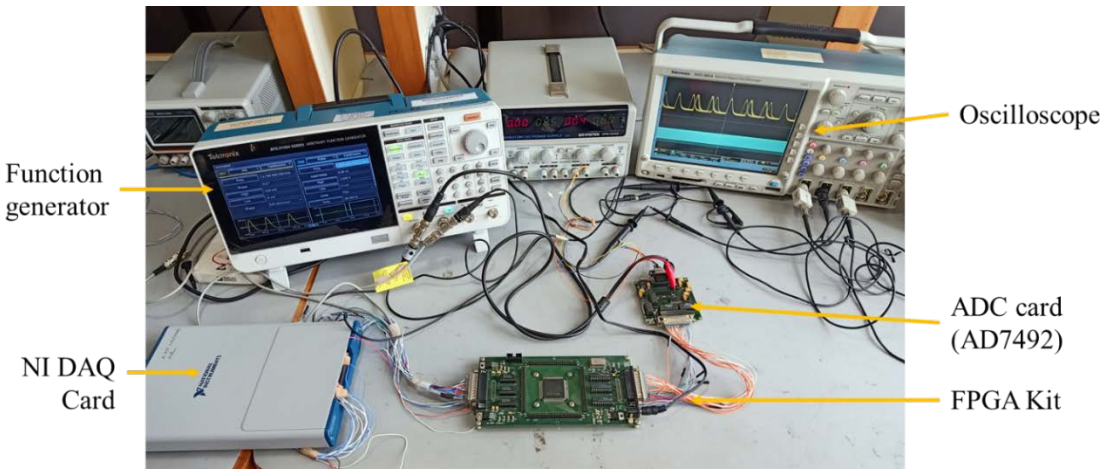


Figure 4.7: Experimental setup for Relative error (RE) measurement

Usually Flash-type ADC is required for higher sampling rates, which consume higher power. Typical flash ADC power consumption is 35 mW to 5 W depending on the sampling rate and number of bits. If the instrument has multiple X-ray channels to

read using higher sampling rate ADCs then the instrument would require very high power, which is a major constraint in space payloads. To design a very low-power instrument, successive-approximation ADCs like AD7492 (parallel ADC) and ADC128S102 (serial ADC) can be used which consume 12 mW and 3 mW power, respectively. For the current experiment, the AD7492 analog to digital converter is used which has a 2.5V internal reference voltage and maximum sampling rate of 1.25 MHz. The function generator's output pulse is sampled at 1 MHz.

The FPGA is used to implement the interpolation methods. Each technique employs three-point interpolation except near interpolation. FPGA is also finding the peak amplitude from the interpolated data. Using a National Instruments (NI) data acquisition module, the computer receives the FPGA's processed data. The LabVIEW code is written on a computer to store the data in text file. The MATLAB code is written to read the text data and estimate Relative error, Mean square error, and Mean absolute deviation. Each interpolation method covered in the previous part is implemented independently in an FPGA, and data was obtained. The setup for experiment is shown in Figure 4.7. The equation for relative error is listed below (4.11) where the peak-actual is ideal 12-bit data corresponding to 1V, and peak-measured is the peak value measured after interpolation which is taken from LabVIEW code. The dc offset in the peak-measured data is derived and deducted while computing Relative Error. The fitting accuracy is accessed by MSE (4.12) and Mean Absolute Deviation MAD (4.13) [110]. The relative error is calculated for thousand pulse data.

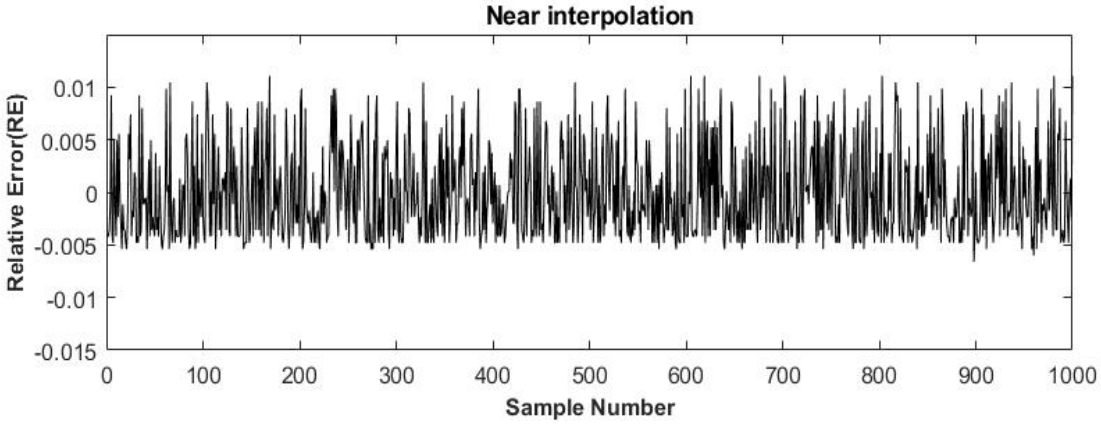
$$Peak_{actual}\ for\ 1V\ amplitude\ pulse = \frac{4096\ (12-bit)}{2500\ (2.5V\ ref)}\ x\ 1000 = 1638.4 \tag{4.10}$$

$$Relative\ error = \frac{Peak_{\ actual} - Peak_{\ Measured}}{Peak_{\ actual}} \tag{4.11}$$

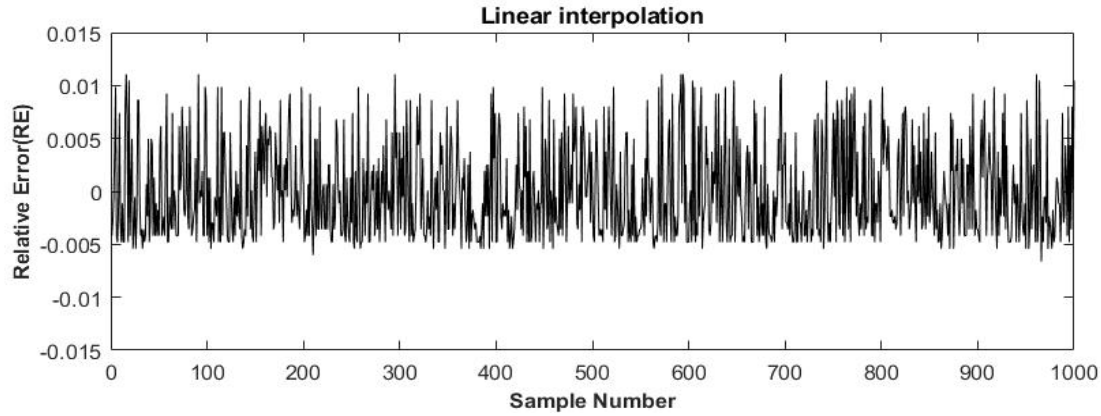
$$MSE = \frac{\sum_1^n (Relative\ Error)^2}{n} \tag{4.12}$$

$$MAD = \frac{\sum_1^n |Relative\ Error|}{n} \tag{4.13}$$

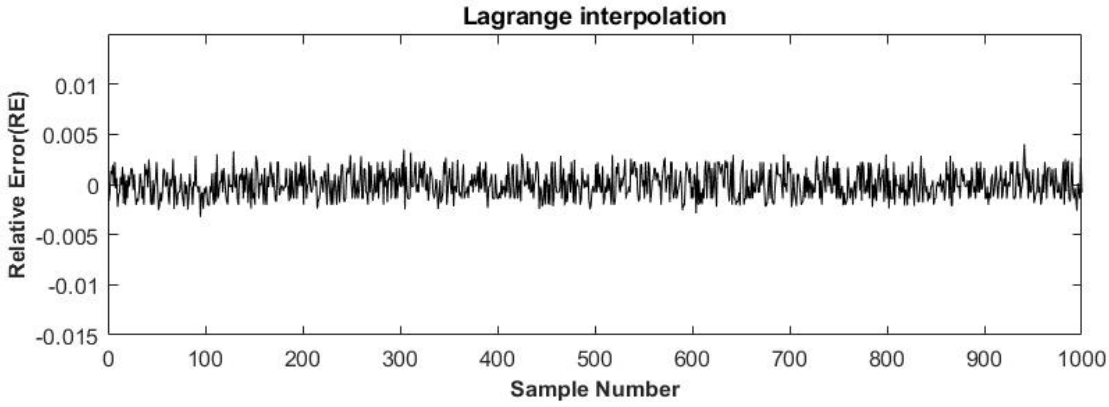
The mean square error and mean absolute deviation are calculated using relative error as shown in equations (4.12) and (4.13) [110]. Where the value of *n* is 1000. The relative error (RE) is calculated for thousand samples for various interpolation techniques and is shown in Figure 4.8.


Near interpolation
Relative Error(RE)
0.01
0.005
0
-0.005
-0.01
-0.015
0
100
200
300
400
500
600
700
800
900
1000
Sample Number

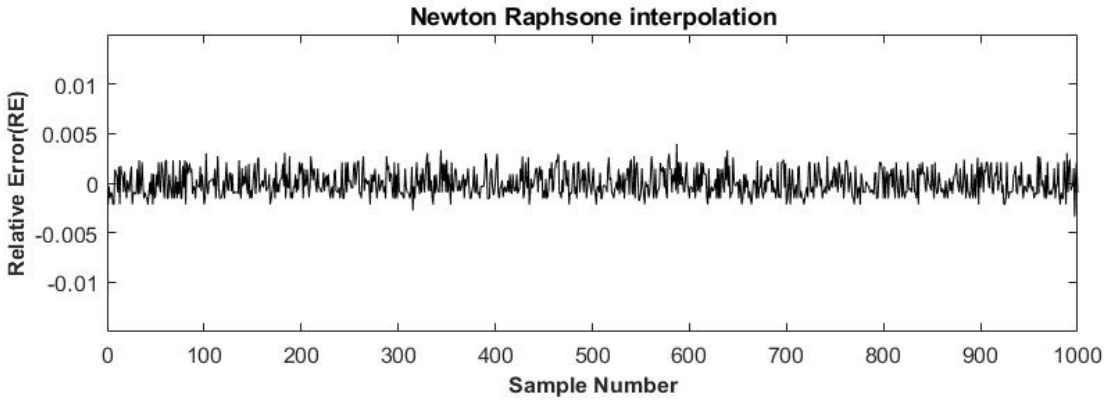
(a)


Linear interpolation
Relative Error(RE)
0.015
0.01
0.005
0
-0.005
-0.01
-0.015
0
100
200
300
400
500
600
700
800
900
1000
Sample Number

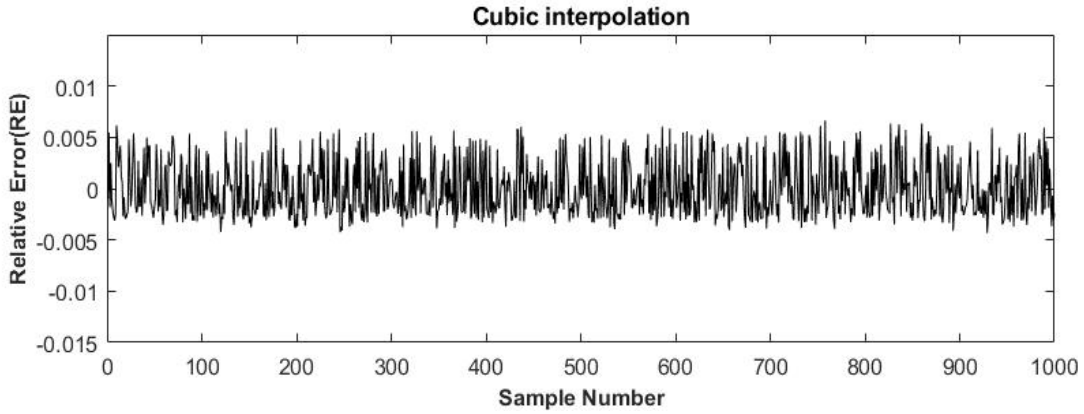
(b)


Lagrange interpolation
Relative Error(RE)
0.01
0.005
0
-0.005
-0.01
-0.015
0
100
200
300
400
500
600
700
800
900
1000
Sample Number

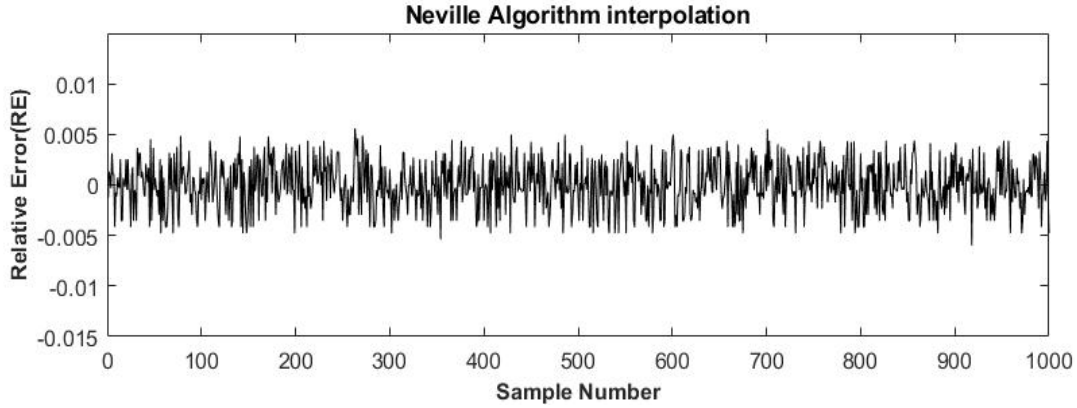
(c)


Newton Raphsone interpolation
Relative Error(RE)
0.01
0.005
0
-0.005
-0.01
0
100
200
300
400
500
600
700
800
900
1000
Sample Number

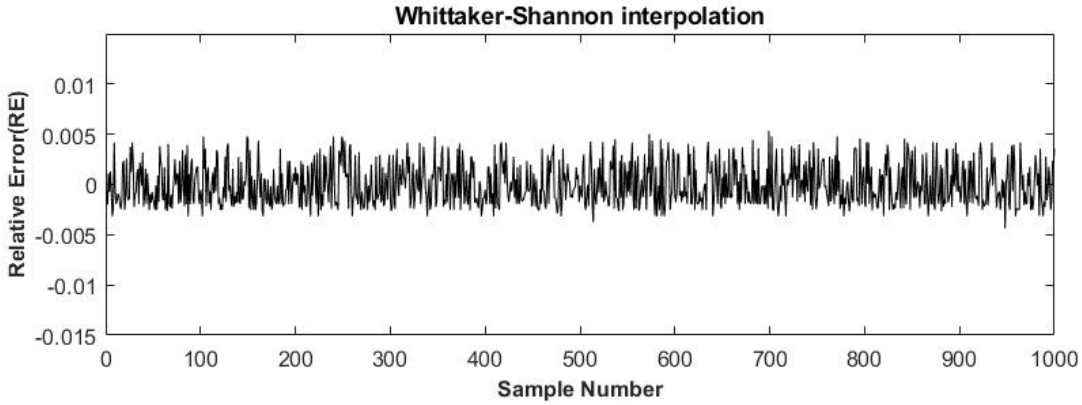
(d)



(e)



(f)



(g)

Figure 4.8: Relative error (RE) values for different interpolation methods for 1000 sample data.

The thickness of the relative error plot indicates the interpolation method's performance. The greater the interpolation error, the thicker the plot. According to Figure 4.8, the relative error is highest for near and linear interpolation and lowest for Lagrange's and Newton’s raphson interpolation. The relative error for near and linear interpolation is higher because the derived point result is more dependent on the value of nearest samples. The RE value for cubic interpolation is greater than the RE value

for Neville's and Whittaker Shannon's interpolation. The Lagrange and Newton-Raphson methods perform the best in terms of relative error.

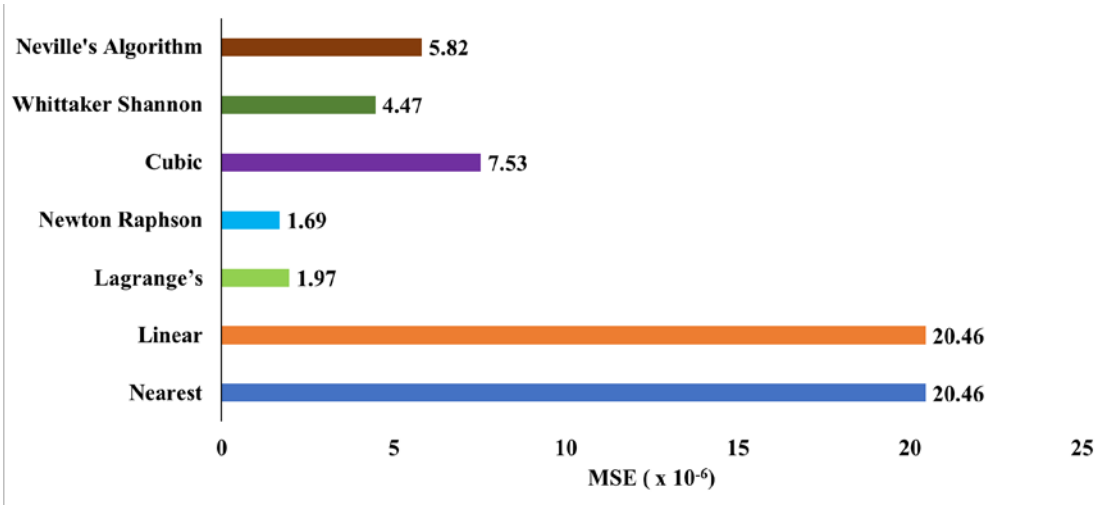


Figure 4.9: Mean square error (MSE) values for different interpolation methods for 1000 sample data

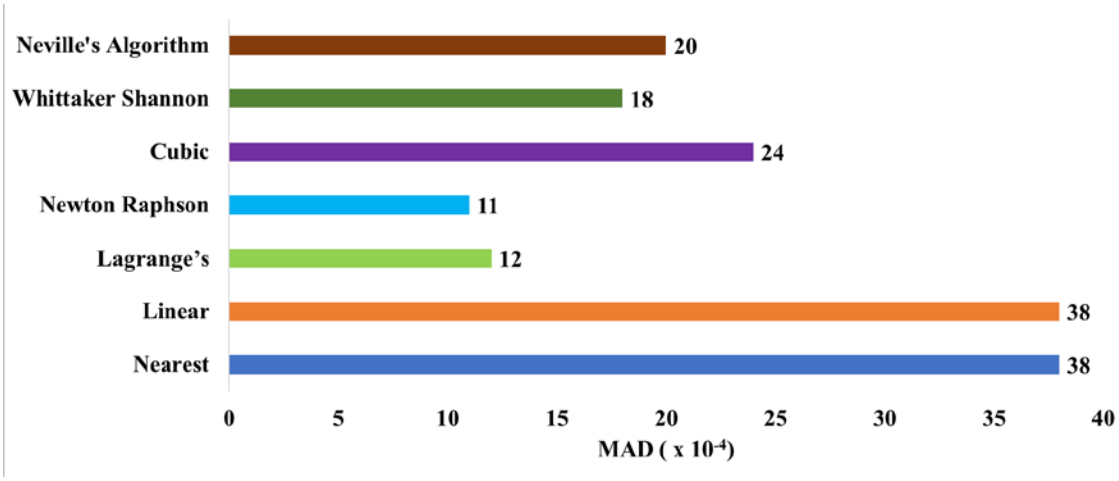


Figure 4.10: Mean absolute deviation (MAD) values for different interpolation methods for 1000 sample data

The MSE and MAD are lowest for the Lagrange's and Newton Raphson methods, according to the data in Figure 4.9 and Figure 4.10. For Lagrange's interpolation method, MSE is 1.97 x 10^{-6} and MAD is 12 x 10^{-4}. MSE for Newton Raphson interpolation method is 1.69 x 10^{-6} and MAD is 11 x 10^{-4}, which are very close to Lagrange's interpolation method.

In terms of FPGA resource utilization, as shown in Figure 4.11 and Figure 4.12, Neville's Algorithm and Newton Raphson interpolation require the most logic cells, whereas the nearest interpolation method requires the fewest logic cells due to the

function's simplicity. When compared to Lagrange's method, the Newton Raphson method uses more hardware.

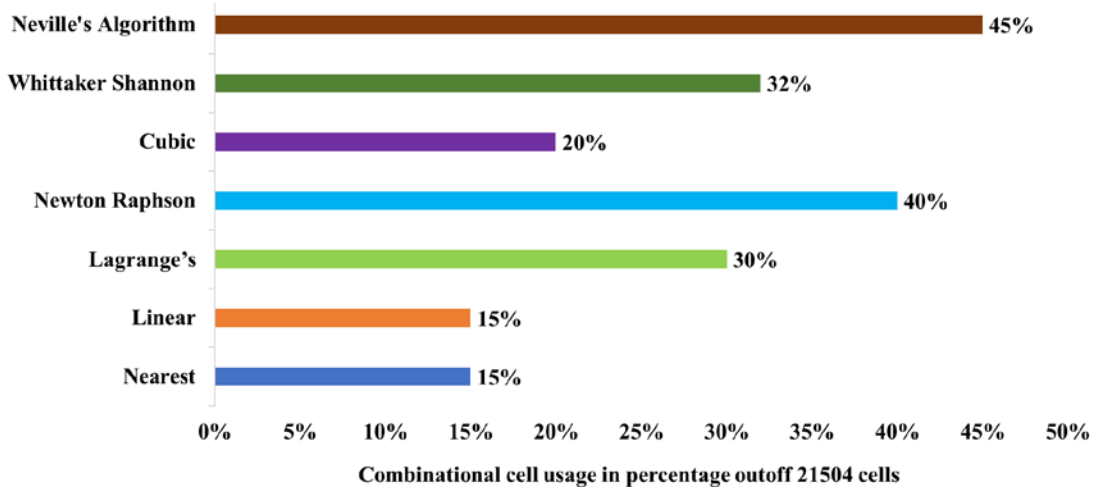


Figure 4.11: Combinational cell utilization of A3PE1500 FPGA for different interpolation methods

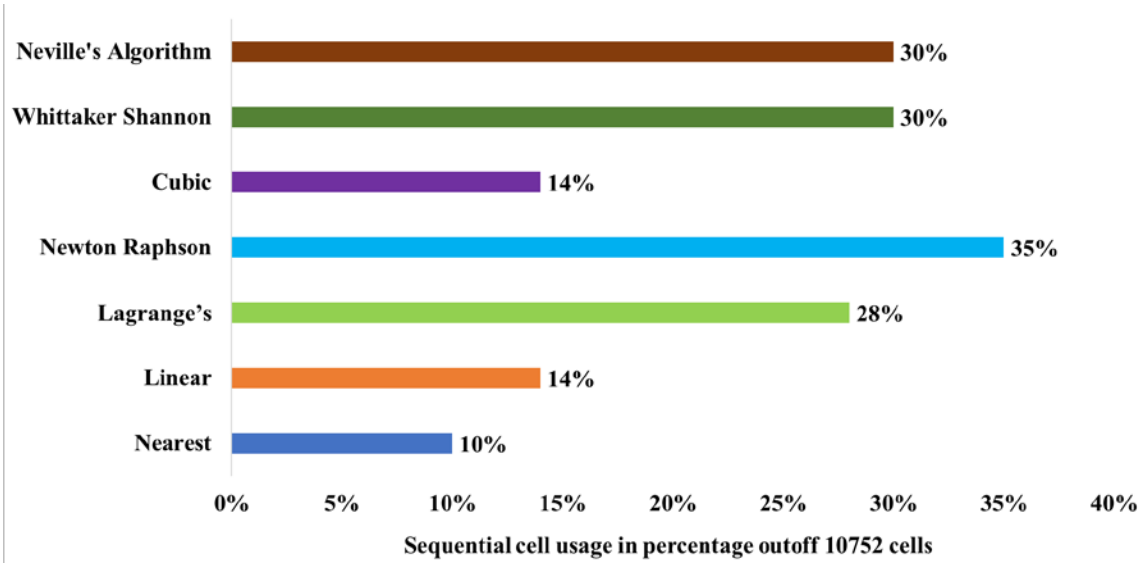


Figure 4.12: Sequential cell utilization of A3PE1500 FPGA for different interpolation methods

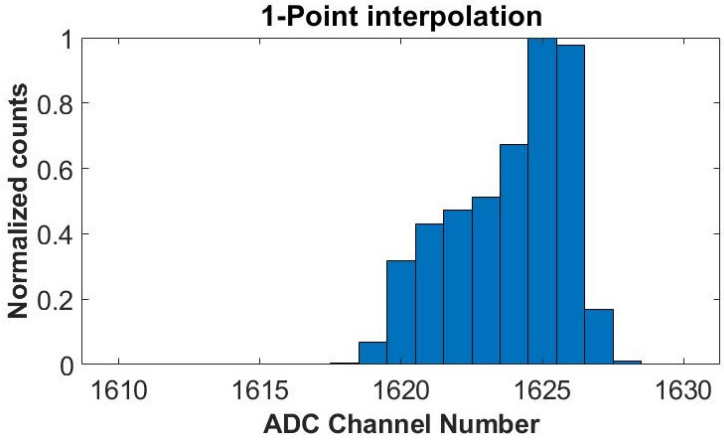
In this section, the experiments were discussed in which the semi-gaussian pulse peak height was measured using seven interpolating methods: Near, Linear, Cubic, LaGrange's, Newton Raphson, Whittaker Shannon, and Neville's. The Mean Square Error (MSE), Mean Absolute Deviation (MAD), and hardware resource utilization was used to compare performance. For thousand equal amplitude samples studied and MSE on FPGA for Near, Linear, Cubic, LaGrange's, Newton Raphson, Whittaker Shannon

and Neville's interpolation methods were found to be 20.46 x 10^{-6}, 20.46 x 10^{-6}, 1.97 x 10^{-6}, 1.69 x 10^{-6}, 7.53 x 10^{-6}, 4.47 x 10^{-6}, and 5.82 x 10^{-6}. It was observed that the nearest interpolation uses minimum hardware, Neville's Algorithm and newton Raphson interpolation uses maximum resources and Lagrange's method uses moderate hardware resources (30% combinational cell, 28% sequential cells) and gives better error performance. Based on the above study LaGrange's interpolation method is used for the proposed method.

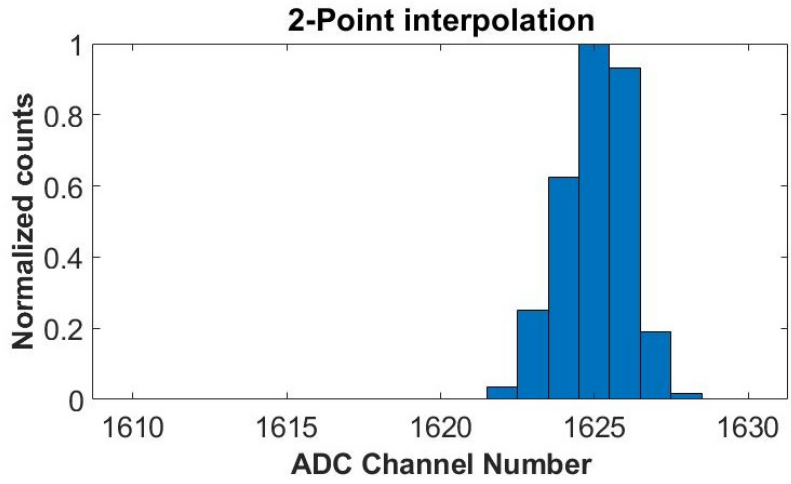
4.4 Experiment to derive optimum interpolation points

The experiment was conducted utilizing a function generator and the setup described in section 4.3.2 in order to determine the ideal number of needed interpolation points. The semi-gaussian shaped pulse as seen in Figure 4.6 from the function generator is sent to the ADC. It has a peak amplitude of 1V, and a peak time of 4 μs. A 1 MHz sampling rate is used to sample an input signal, and the data is then stored in an FPGA for interpolation. The same ADC, an AD7492 (parallel output ADC), a 1.25 MHz sampling ADC with a 2.5 V internal reference voltage, is employed. In order to provide a varied number of interpolation points between the real data points, the LaGrange's interpolation algorithm is implemented in an FPGA with a different order of interpolation.

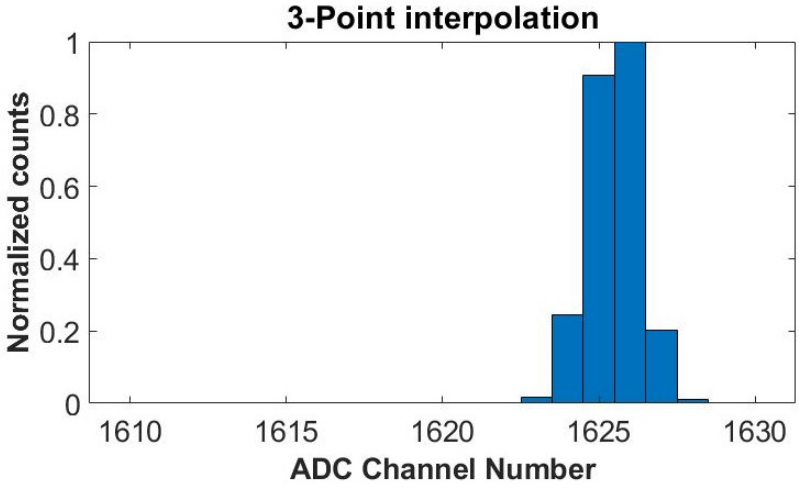
Since the shaping time in this case is 9 μs, the ADC will only provide 9 samples for the pulse profile, which is insufficient to accurately determine the peak height of the pulse. The sample size is expanded to 36 numbers after three-point interpolation, which aids in more precise peak height determination. After interpolation, the sample with the highest peak value is identified, providing precise peak information. Figure 4.13 displays the histogram data for several LaGrange's interpolation orders.



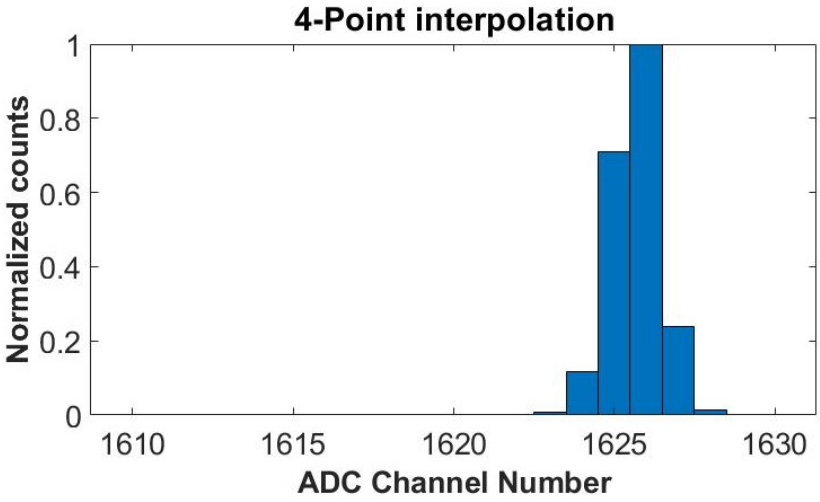
(a)



(b)



(c)



(d)

Figure 4.13: Plots of the spectrum for various interpolation points between two raw data points. (a) One-point interpolation, (b) two-point interpolation, (c) three-point interpolation, and (d) four-point interpolation are examples.

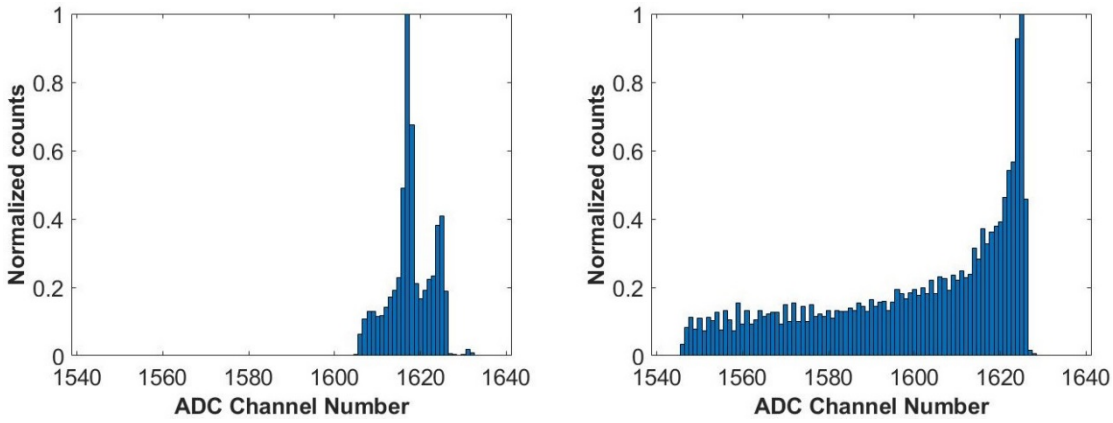
The variance is higher for lower interpolation points and almost constant after three-point interpolation. Based on these observations, a three-point interpolation was selected for the proposed method. The effect on variance is the same for shaping time pulses. It is observed that 4-channel variance is constant after 3-point interpolation.

4.5 Experiment to derive required shaping time

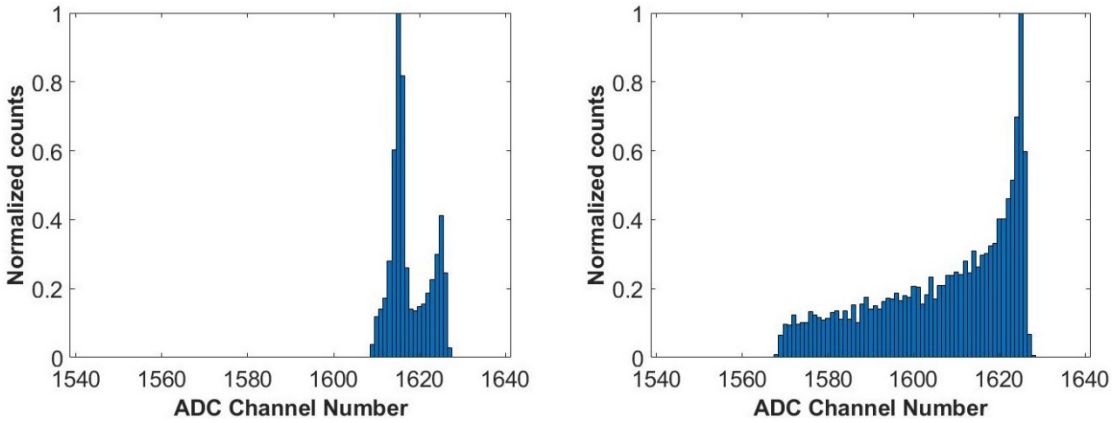
Another experiment was conducted to compare the peak height obtained from raw data and interpolated data, as well as to determine the ideal pulse shaping time for the interpolation approach. In the experiment, sampling ADC input was fed semi-gaussian shaped pulses from a function generator with varying shaping periods, fixed peak amplitude of 1 V, and frequency of 1 kHz. With the aid of an ADC, input signals are sampled at a rate of 1 MHz for all shaping time input pulses. For one set of data, the input pulse's shaping time is fixed. The FPGA is used in the first portion of the experiment to locate the peak height by looking for maximum value data in a sample data stream. The histogram, also known as raw data spectrum, was created using this highest value data. In the second section, the FPGA was used to interpolate three additional samples between raw samples, and the highest sample value was then determined. To determine the value of an interpolated sample, Lagrange's interpolation is implemented within an FPGA. The ADC values that are greater than pre-determined threshold values will be chosen by the FPGA. For the interpolation equation, a few points are additionally obtained just before to the pulse's beginning. Once the array has a value of five points, the FPGA algorithm will begin the interpolation procedure. The procedure will look for three interpolated values that are higher than a threshold between the first and second points of the pulse. In order to compute the equation again on five points, the new derived points will be inserted between the array's points, and the array will be moved by one new sample that arrives from the ADC. The FPGA is run at a clock frequency of 40 MHz, which is sufficient to finish one procedure before the arrival of the subsequent sample, which is spaced out by1 μs.

In Figure 4.14, the histogram plots are displayed. Figure 4.14’s left panels in each of its subfigures display the spectra for peak height created using the raw sample data, while the right panels display the spectra for pulse height created using interpolated data. It has been shown that the variance of detected peak height values in raw data spectra is higher than that in interpolated data. The variance in the raw data

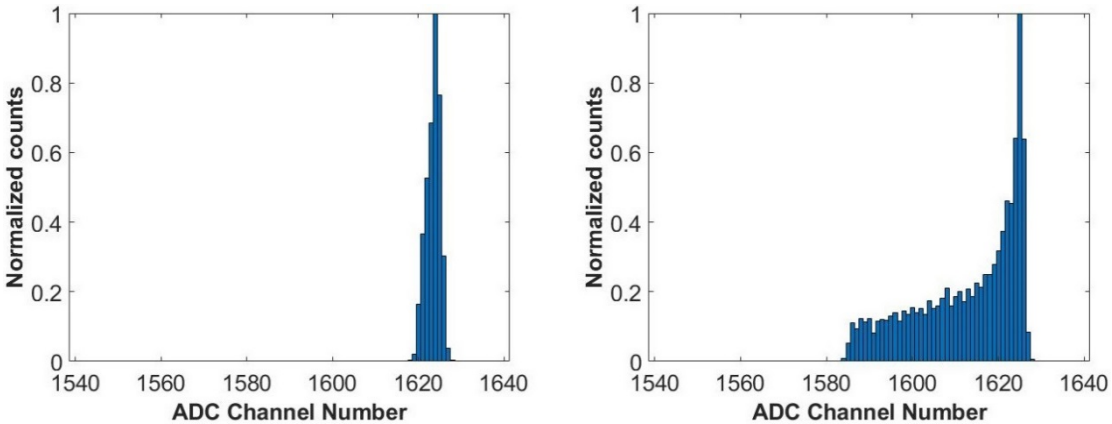
spectra is decreased when the shaping time is increased since there are more sample points in the pulse.



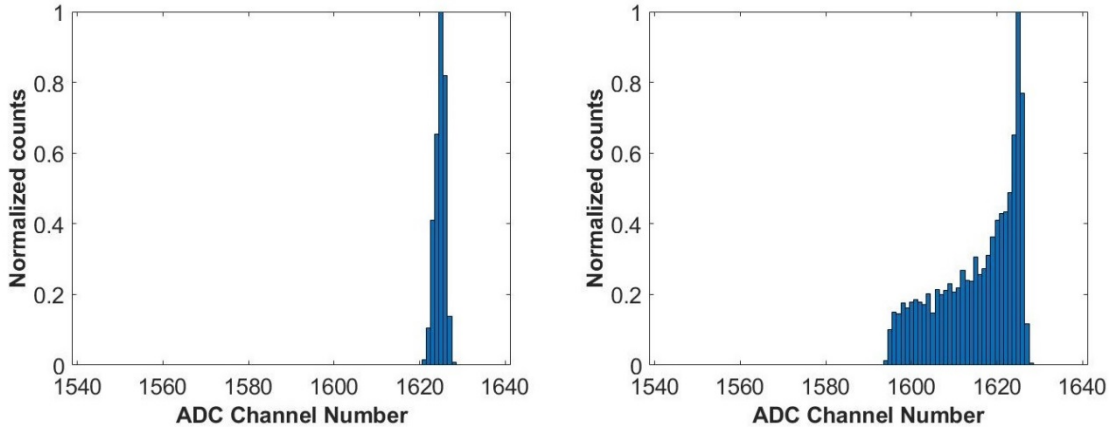
(a) Data with 5 μs semi-gaussian pulse input



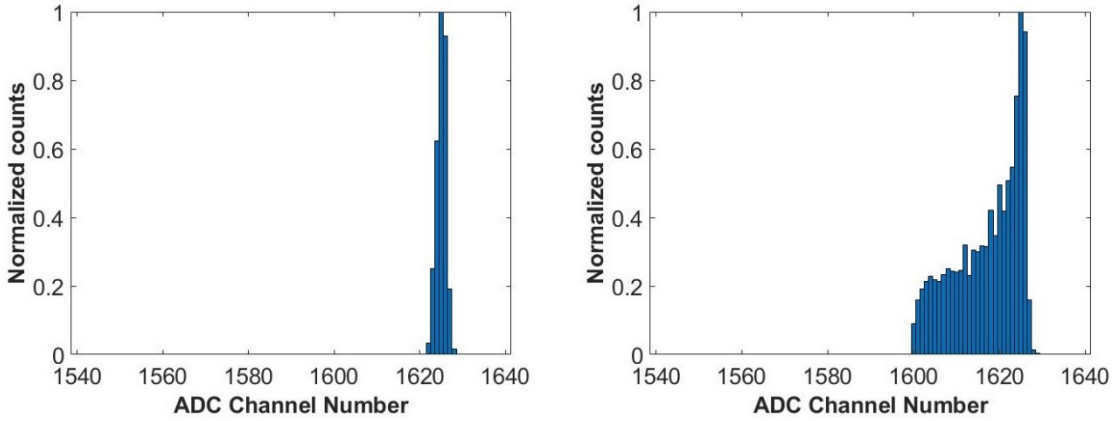
(b) Data with 6 μs semi-gaussian pulse input



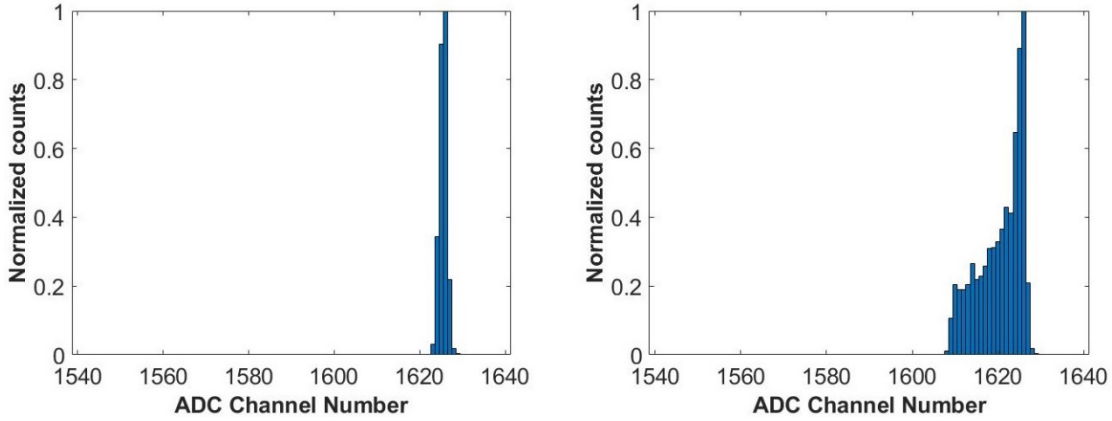
(c) Data with 7 μs semi-gaussian pulse input



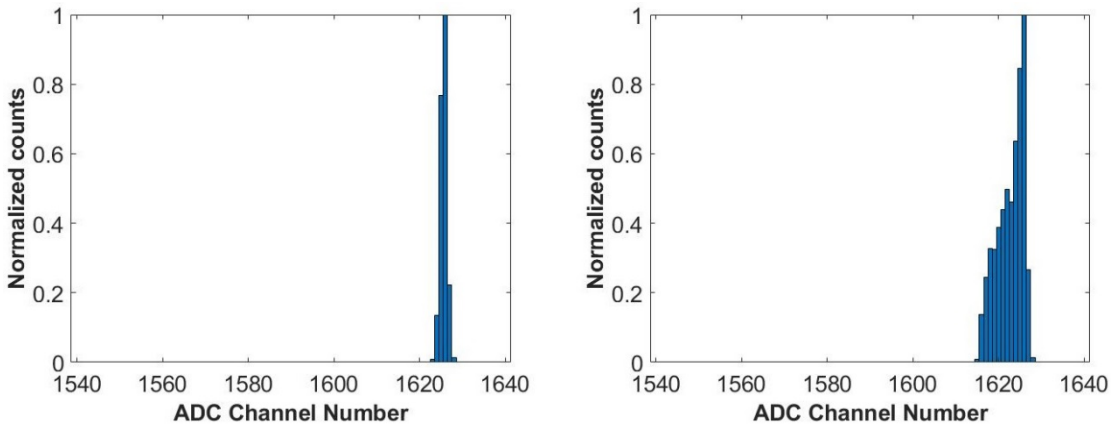
(d) Data with 8 μs semi-gaussian pulse input



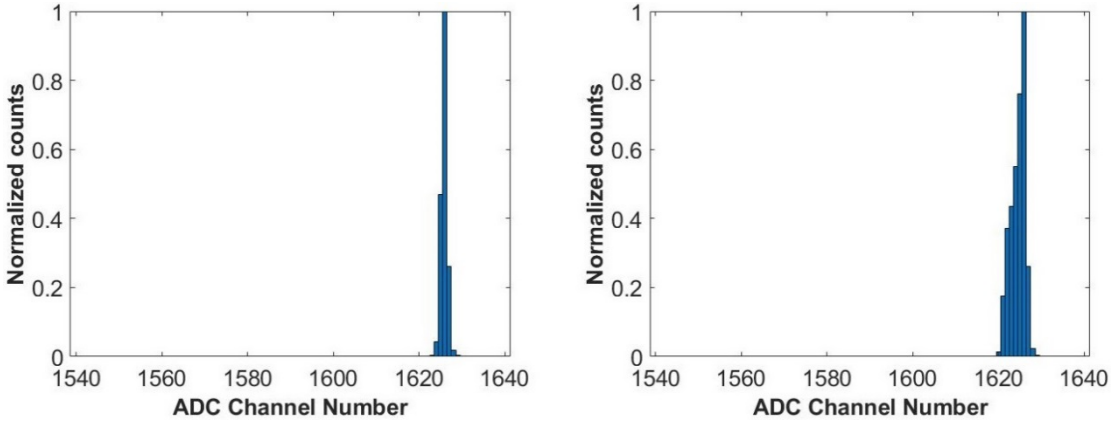
(e) Data with 9 μs semi-gaussian pulse input



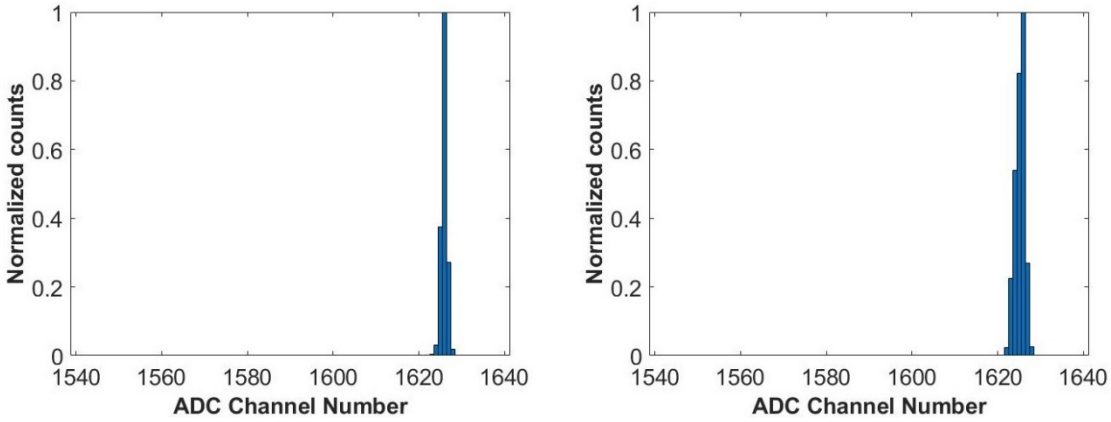
(f) Data with 11 μs semi-gaussian pulse input



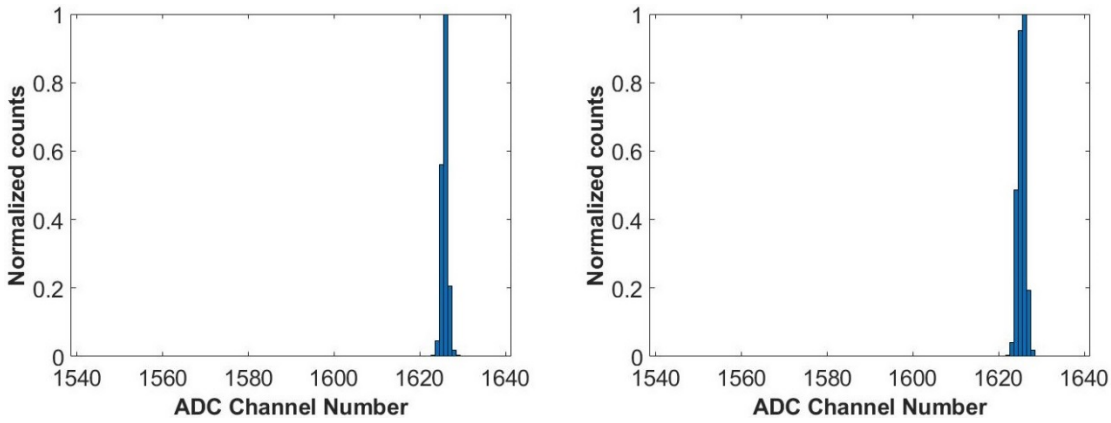
(g) Data with 14 μs semi-gaussian pulse input



(h) Data with 20 μs semi-gaussian pulse input



(i) Data with 25 μs semi-gaussian pulse input



(j) Data with 30 μs semi-gaussian pulse input

Figure 4.14: Peak height histograms constructed using interpolated data (left) and raw sample data (right).

To determine the performance with regard to shaping time, the spectral spread comparison is done for interpolated data, and raw data from the data displayed in Figure 4.14. The count on the Y-axis is normalized by taking ratio of the count values to the greatest spectral bin count value. According to plot displayed in the Figure 4.15, the variance in interpolated data at 8 μs of shaping time is 7 channels, and it stays that way for increasing shaping time pulses. The suggested approach needs a minimum pulse shaping duration of 9 μs to work at its best with a 1 MHz sampling rate and three points of interpolation. By raising the sample frequency, the variance and shaping time may be decreased. Figure 4.14 (a) and (b) show the minor double peak in interpolated spectral data that results from an interpolation error caused by the lack of sufficient raw samples. Raw sample data has a lower likelihood of containing the precise peak sample value, which explains why raw sample spectra have a large spectral tail. The generated peak height is quite near to the real peak height due to interpolation, which prevents the spectral tail from being seen in the interpolated data. A longer shaping time will result in more raw samples taken close to the pulse peak, which will decrease interpolation error, increase the chance of obtaining an exact peak sample, and decrease spectral spread. Better interpolation will be provided by an increase in shaping time, although pile-up occurrences will also rise. The ADC channel number 1626 has the highest counts across all spectrum charts, corresponding to a voltage level of 0.992 V. The intrinsic offset of the ADC, which is consistent across the whole range, is the cause of the 8 mV offset.

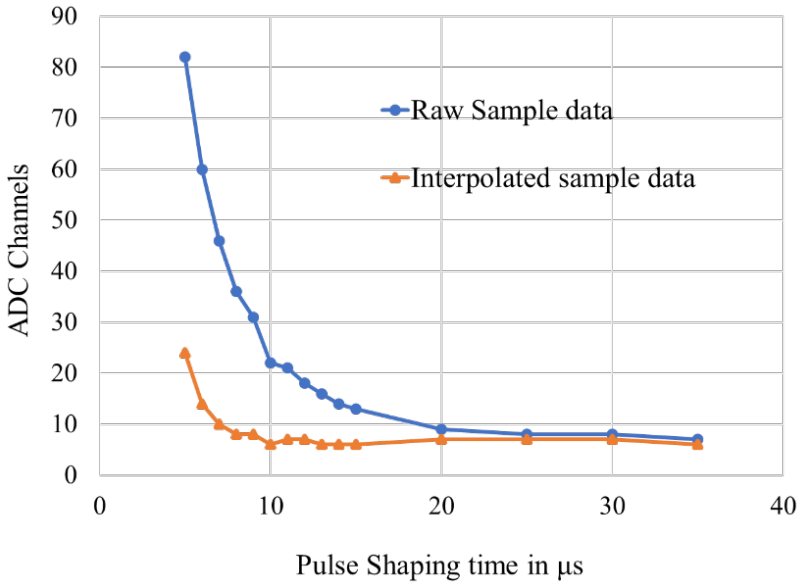


Figure 4.15: Plot of variance (spectral dispersion) in ADC channels vs signal shaping time

After the pulse shaping time of 35 µs, the variance for the raw data and the interpolated data are almost identical, according to the plot in Figure 4.15. After 9 µs of shaping time, the variance in the interpolated data remains constant. The proposed approach uses a shaping time of 9 µs based on this experiment. Since the shaping time is inversely correlated with the sampling rate, it will be correspondingly shorter if we utilize a higher sample ADC. However, in this instance, higher FPGA clock frequency is necessary to decrease the FPGA processing time for interpolation. Rise in ADC sampling rate and FPGA clock frequency will increase power consumption.

4.6 The proposed algorithm's performance with the silicon drift detector (SDD) configuration

A setup comprising an SDD detector, HV bias, CSPA, and shaping amplifier was created to evaluate the proposed method with real-time radiation data. The 4 µs pulse peaking time (9 µs pulse shaping time) is chosen to improve accuracy and dead time based on the tests described in the previous Section.

Figure 4.16 depicts the configuration of a detector, front-end electronics, sampling ADC, and FPGA. The ADC card receives the output of the shaping amplifier, and the FPGA A3PE1500 controls the analogue to digital converter. In real time, the FPGA executes interpolation after reading data from the ADC. The FPGA creates the histogram that is sent to a computer by determining the peak of the interpolated data.

FPGA is running on the 40 MHz frequency which is enough for operation as the experiment is carried out for 1 MHz sampling ADC. The one event interpolation process is finished within 1 μs time and the histogram generation process requires 1 μs time which is carried out while the pulse decay process starts after completion of peak detection process.

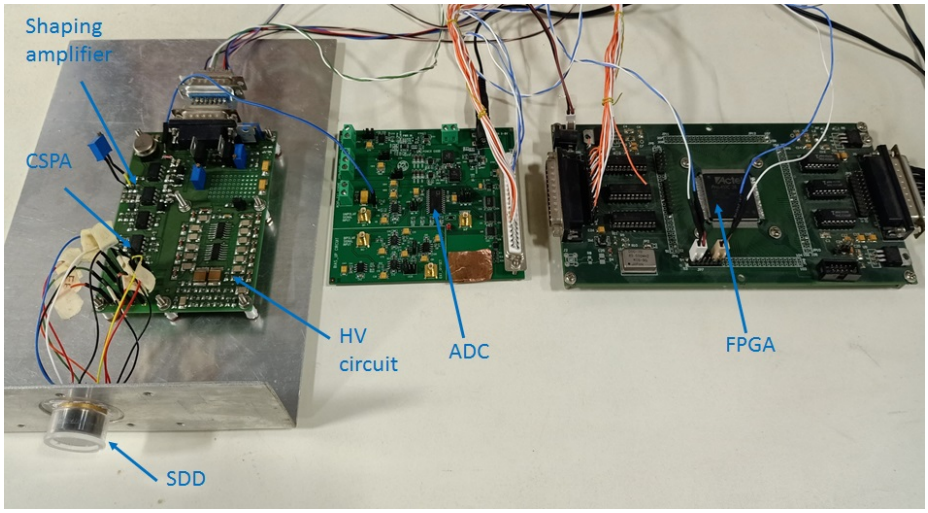


Figure 4.16: Front-end setup interface with ADC and FPGA cards for the Silicon Drift Detector (SDD).

Figure 4.17 displays the shaping amplifier output when a ^{55}Fe X-ray source is used to illuminate the detector. The two peaks are the 5.9 keV Mn Kα and 6.4 keV Mn Kβ lines, respectively.

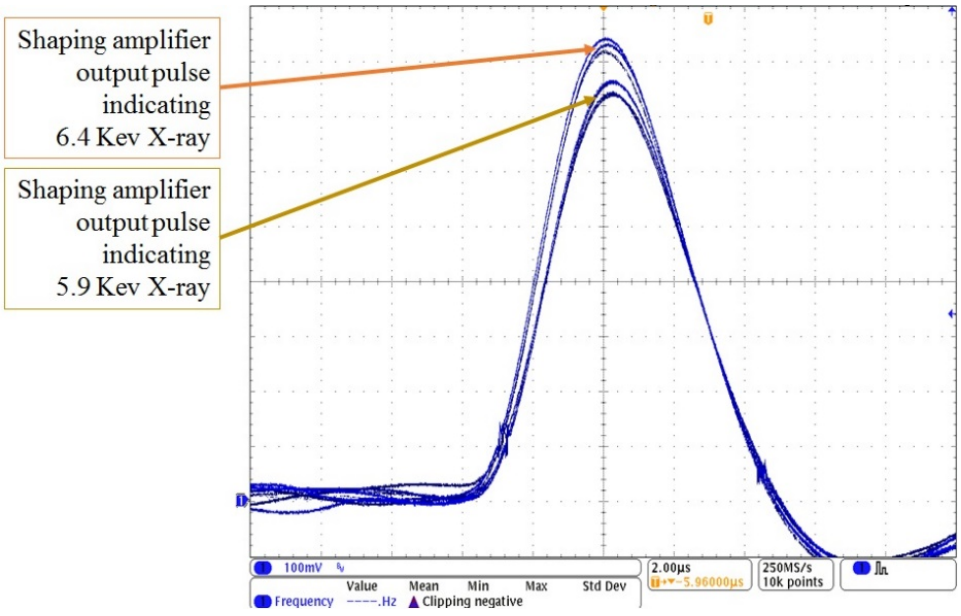


Figure 4.17: CRO image shows the output of the shaping amplifier. The Y-axis has a 100-mV grid size, whereas the X-axis has a 2 μs grid.

The 6.4 keV line, which has lesser flux, is shown by the higher amplitude signal, while the 5.9 keV line, which has greater flux, is shown by the lower amplitude. For certain X-ray lines, the flux is always proportional since the source is natural radioactivity.

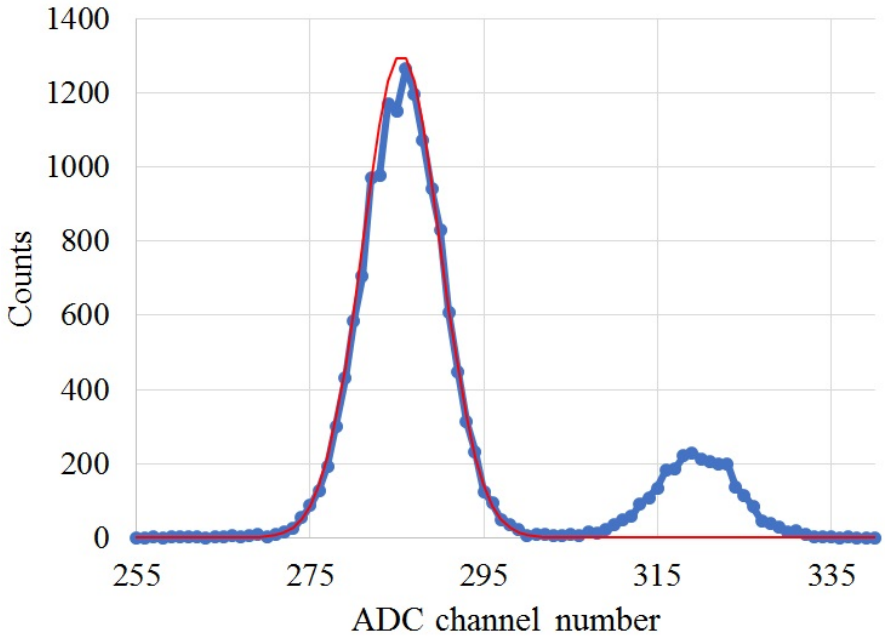


Figure 4.18: Spectral data were collected by illuminating a ^{55}Fe X-ray source with a real-time interpolation approach that was developed on an FPGA. A fitting with gaussian function using red line is over-plot to the main peak.

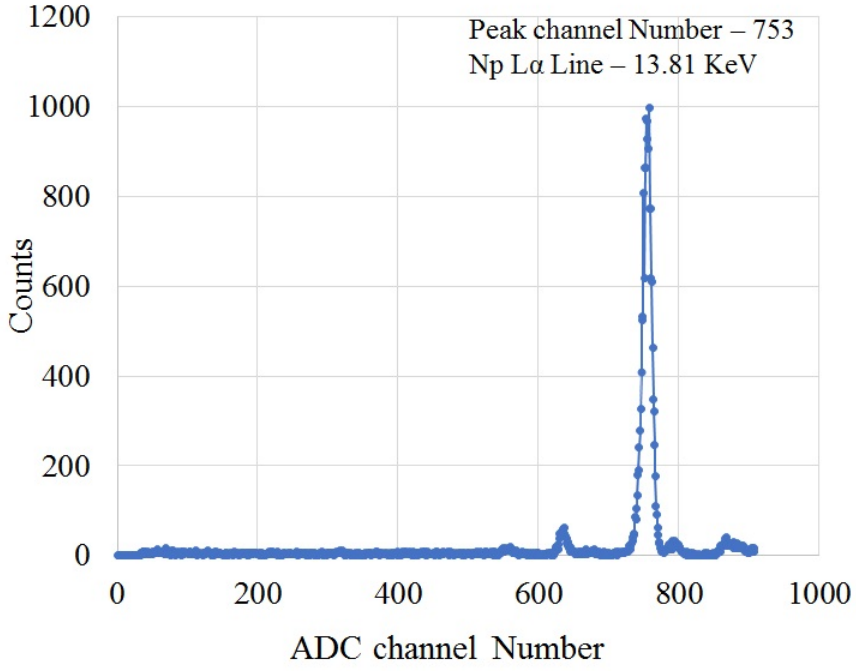


Figure 4.19: Spectral data collected by illuminating ^{241}Am X-ray source (Real-time interpolation method used).

The spectra shown in Figure 4.18 is obtained by illuminating ^{55}Fe source in front of detector and integrating the event data. The energy resolution 165 eV is achieved at 5.9 keV with interpolation technique implementation in FPGA, which is comparable to the methods explained in the earlier chapter. The same system was used to gather the data for ^{241}Am X-ray source. Figure 4.19 displays the ^{241}Am X-ray spectrum, in which the Np Lα is discernible.

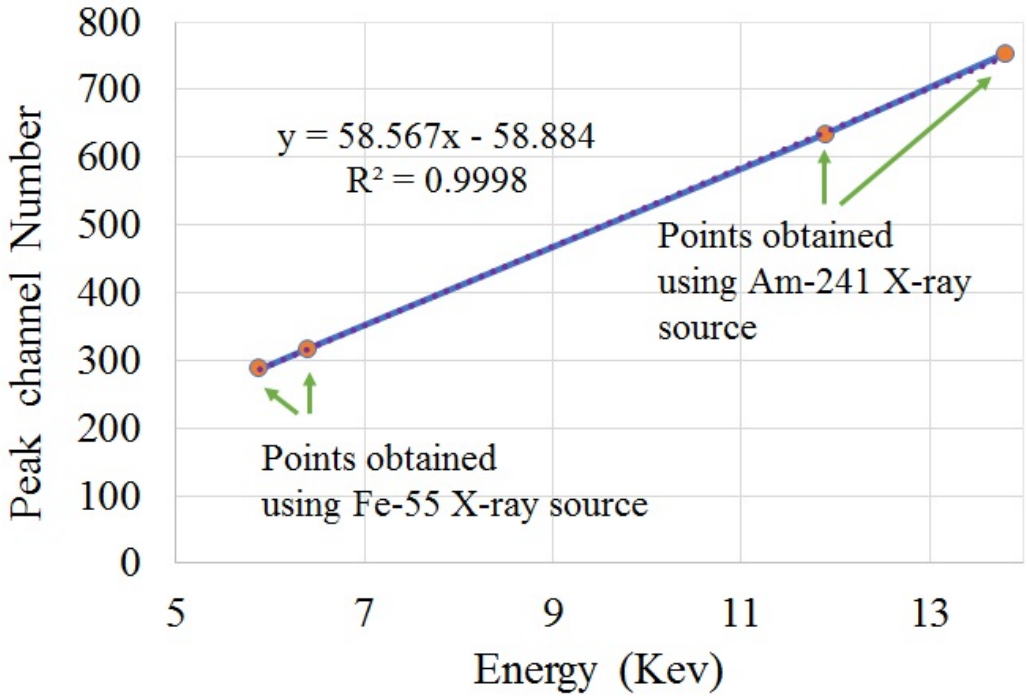


Figure 4.20: Plot of the incident energetic lines' peak channel as a function of energy. The residuals are displayed together with an over-plotted dashed trend line on the data.

In Figure 4.20, the peak channels of observed X-ray lines are shown with respect to incoming energy to determine the system's linearity. Offset and gain were then calculated from these peak channels using a straight-line fit.

Table 4.1 and Table 4.2 compare several pulse processing methods. The finest energy resolution, 152 eV, is achieved by the digital pulse processing technology, but the complexity of its implementation for numerous detector systems makes it unsuitable for use in space instruments. In order to use the digital pulse processing approach, a higher sample rate ADC is required. This calls for a higher FPGA clock frequency, which increases FPGA power consumption. The implementation of a trapezoidal filter inside an FPGA or DSP is used for pulse processing, which uses additional FPGA resources and may restrict the construction of many channels inside a single FPGA

device. Because this technique requires less processing time, pileup incidents are much minimized. For single detector systems, the conventional peak detector approach is effective, but it has the drawback of requiring more pileup time because of the longer processing time. The shaping amplifier, peak detector, event trigger generator, and ADC are among the several parts needed to accomplish this method.

Table 4.1: Comparison of various pulse processing techniques for energy resolution, Peaking time, Event process time, and Power

Pulse Processing Method	**Energy resolution eV @ 5.9 keV**	**Pulse Peaking time used (µs)**	**Event process time including peaking time (µs)**	**System Power (watt) for a single chain of the detector system**
The conventional peak detection technique	157	5	7	6
Digital Pulse Processing technique	152	1	2	10
Linear Discharge technique	300	4	40	5.5
Pulse width modulation (PWM) technique	300	8	16	4.5
The Proposed method (Interpolation of sample data)	**165**	**4**	**8**	**4.5**

When many detector readouts with low energy resolution are required, the other two techniques—linear discharge technique and pulse width modulation—can be applied. The linear discharge technique has a longer pileup period since it bases its operation on the discharge time of the pulse. It is challenging to find a high-frequency triangle wave with enhanced linearity and stability, which is required for the PWM approach. In the PWM approach, a longer shaping time is needed for greater energy resolution, but this increases pileup time. Both methods don't need an ADC because they rely on time-to-energy conversion. The PWM technique necessitates more FPGA resources because it must determine the width of all pulses. The proposed method

requires less power, mass and size for multi detector system compared to conventional peak detector method and digital pulse processing method. If the readout system for detectors like as SiPM, Silicon PIN, CdTe, and others is constructed using digital pulse processing and the proposed approach, both methods will provide comparable energy resolution since detector noise is quite high in comparison to readout system resolution. All the developed methods are not optimized for the processing time, Mass and power, so they are not compared by numbers in Table 4.2. But the comparison is carried out by having currently developed design numbers and general idea about particular methods requirement.

Table 4.2: Comparison of various pulse processing techniques for pile-up event, FPGA processing requirement, Mass, and PCB area requirement.

Pulse Processing Method	**Pile up event**	**FPGA processing requirement**	**Mass for multiple channels system**	**PCB Area required to implement multiple channels**
The conventional peak detection technique	Moderate	Low	High	High
Digital Pulse Processing technique	Low	High	High	High
Linear Discharge technique	Very high	Moderate	Low	Low
Pulse width modulation (PWM) technique	High	Moderate	Low	High
The Proposed method (Interpolation of sample data)	**Moderate**	**Moderate**	**Low**	**Low**

The proposed method has peaking time 4 μs which can give maximum throughput of 40 Kcps [47] due to pile up. The suggested approach with a sample rate of 1 MHz is best suited for most radiation detector equipment with flux rates less then 40Kcps, such as Alpha Particle X-Ray Spectrometers, Charge particle detectors, wide area X-ray telescope detectors, and so on. By restricting the incoming flux rate to the detector or

raising the sample rate of the ADC, the suggested approach may still be employed for radiation sensors that cope with greater flux rates.

4.7 Summary

The suggested approach (interpolation with low sample rate ADC), which was covered in Sections 4.5 and 4.6 of this chapter, provides improved resolution and linearity. It is demonstrated that LaGrange's interpolation technique with three-point interpolation is the most appropriate approach for the suggested method from the discussion and conclusions drawn in sections 4.2 and 4.3. In the suggested method, no peak detector or event trigger generating circuit is needed. The FPGA operates at a lower clock frequency, which lowers system power. An extremely power-efficient ADC with low sampling rate is employed. Any single detector or multiple detector system can use the suggested approach. The demonstrated system runs at a sampling rate of 1 MHz and has a shaped pulse peaking time of 4 μs. The sample duration can be increased correspondingly if the shaping time is short. The experimental results indicate that for better resolution, the sampling time should be at least four times lesser than the peaking time of the shaped pulse. Because of the faster processing time in this approach, pileup occurrences are substantially less frequent compared to the linear discharge and pulse width modulation methods and approximately equal to those in the traditional peak detection method. The demonstrated system requires just minor changes to be employed for a space instrument because it is constructed with components that have a space-qualified version.

CHAPTER – 5

5 SUMMARY AND FUTURE PLAN

5.1 Summary of the research work

The Lagrange interpolation-based detector signal readout technique for SDD-based X-ray spectrometers was developed using commercially equivalent space-qualified components. When the SDD is cooled to -40°C for the pulse peaking time of 4 μs, the developed spectrometer provides an energy resolution of ~165 eV at 5.9 keV. This readout method can also be used with other radiation detectors. This technique almost meets the energy resolution criteria for many radiation instruments.

A comparative study of seven interpolating methods namely Near, Linear, Cubic, LaGrange's, Newton Raphson, Whittaker Shannon and Neville's were conducted for peak height measurement of semi-gaussian pulse. The relative error (RE), mean square error (MSE), mean absolute deviation (MAD), and hardware resource consumption have all been used to compare performance. It was observed that Lagrange's method uses moderate hardware resources with better RE, MSE and MAD. With this study, Lagrange's interpolation method is selected for the proposed method.

The known readout techniques for radiation detectors are studied and developed in this research activity. The techniques are developed to compare with the proposed method. Four Pulse height measurement techniques namely conventional peak detector, Digital pulse processing (DPP), linear discharge method and Pulse width modulation were studied, developed and tested. The methods were compared with each other by having the same front-end electronics whose resolution/performance was measured standard digital pulse processing system. The standard system provides an energy resolution of 152 eV at 5.9 keV when the SDD is cooled to -40°C and for the pulse peaking time of 3 μs. With the same front-end electronics, other pulse height analysis techniques back-ends were interfaced. The conventional peak detector technique shows ~157 eV energy resolution with 5 μs peaking time, Linear discharge methods shows ~300 eV energy resolution with 4 μs peaking time and PWM method shows ~300 eV energy resolution with 8 μs peaking time.

When the new technique was compared to the previously mentioned techniques, it was discovered that the new technique provides comparable energy resolution with less pileup, less processing time, and less FPGA processing requirement. The new method was created primarily to target the readout of a system with many channel outputs and limited mass, power, and size. In comparison to other techniques for a multichannel detector or multiple detector systems, the developed technique requires less mass, power, and size. It may be difficult to use ASICs for detector readout in space missions because they must be designed for a specific detector and must be qualified for the radiation environment. The new technique is developed using the components for which similar parts are available in a radiation tolerant package. In this view, it will be easier to use this technique in space payloads.

5.2 Future plan

The development of the readout technique for radiation detectors has reached a level of some maturity in the last few decades. Readout techniques have vastly improved over discrete or Application Specific Integrated Circuit (ASIC) readouts. With these enhancements, it is demonstrated that the spectrometer can provide energy resolution close to the Fano limit.

The research activity can be expanded in a variety of directions, and we have some plans to conduct research in this area. We are working to improve the proposed method's resolution by improving the FPGA algorithm and incorporating base-line noise estimation and correction. We are also working on the detection and correction of pile-up events. This method will also be used for multi-linear SDDs with two-dimensional readouts and segmented anodes and cathodes on both sides of the SDD for electron and hole signal readouts to accurately measure the X-ray position interaction. In this case, the readout system is required to have 170 eV resolution with features like smaller and lighter in size with less power consumption. We are also working on incorporating this readout technique into a space payload, which will be a significant step forward in the development of future planetary/astronomy missions. The developed method is planned to use for upcoming DAKSHA mission from India where multiple SDD detectors are used increase the effective area.

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PUBLICATIONS

Paper-1

Title: A new approach for pulse amplitude measurement using Lagrange's interpolation for radiation or particle detectors

Journal name: Advances in Space Research (Elsevier)

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Paper-2

Title: Comparison of 1-D interpolation techniques to measure the Gaussian pulse amplitude accurately using low sampling data for radiation detector readout.

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