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A SIMPLE CCD CAMERA FOR IMAGING

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A SIMPLE CCD CAMERA FOR IMAGING

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Abstract:

A CCD Camera system was designed, fabricated and tested using an area imager chip of 100 X 100 elements from fairchild, USA type CD-201. The paper describes various subsystems developed for the CCD camera system such as sequencer to generate clocks for transporting the charge packets from the photosites, a videoprocessor to process electrical signal in response to the optical image and display system, etc.

The work on CCD Camera was initiated with a view to become acquainted with the use of CCD detector for imaging and later develop into a more sensitive and sophisticated camera system for imaging astronomical objects having low light signals. The superior performance of CCD detector in terms of sensitivity, linearity, signal to noise ratio over the other detectors, the essential features and the latest state of art of CCD camera for astronomy has been described in brief.

CCD CAMERA

CCD Camera system is an imaging system where image tube of a Conventional T V Camera is replaced by solid state image sensor based on the charge coupled device technology.

A CCD camera system consits of five basic functional blocks :

(1) An Area image CCD sensor :- It consists of photon sensitive CCD silicon detectors organized in matrix of rows and columns integrated on a single chip.

(2) A clock generator :- To generate a number of clock pulses needed to be applied on CCD gates to shift the charges from each pixel for a serial output.

(3) A Video Processor to process the sampled video signal to improve upon signal to noise ratio.

(4) A raster generator for the display of image on the Z modulated Oscilloscope and

(5) A lens system to focus the image on the CCD sensor.

Being a solid state device it has usual advantages of ruggedness, reliability, portability and lowpower dissipation. It is a versatile video instrument useful in noncontact optical instrumentation; optical data acquisition and television image detection. The essential characteristics of imaging by CCD sensor over image tube is (a) wider dynamic range (80 db) (b) wider spectrum response (0.4 μm to 1.1 μm) (c) better quantum efficiency (60%) (d) low light imaging capability and (e) no lag or burn problem etc.

Architecture of CCD 201

CCD 201 (Fig.1) is a 2 phase 10,000 elements (100 X 100) self scanning, Interline transfer type area image sensor with burried channel and ion implanted barrier. In addition chip has also built in 100 colums of 2 phase analogue shift

registers inter-digitated in the photosensor array called vertical shift register and a 102 elements of 2 phase output preamplifier and a compensation amplifier. The image photons incident on the image sensor elements generate a packet of electrons in each element. The resulting photo-electrons are accumulated in the photosites during high state of photogates. The duration of the light high state is the integration period (approx. 20 msec). At the end of integration period the photogate voltage (VP) is lowered and alternate vertical site interlacing charge packets are transferred to their associated vertical shift register. They are then transferred to the output horizontal register, a row at a time by the complementary vertical clocks V_1 and V_2. Fity vertical transfers are required to remove one field of information from the vertical registers. Subsequent to the removal of one field of information, second frame of cycle is instituted to gather information, from the photo-sites corresponding to the other field. The output shift register (also called Horizontal shift register) is 102 elements analogue shift register clocked 102 times faster than vertical shift register clock frequency. As each row of information is transferred from the vertical register to the horizontal register, it is serially moved to the output amplifier by the complementary horizontal clocks ϕH_1 and ϕH_2. The charge packets are applied to a precharged diode which develops a voltage linear in respone to the charge

delivered. This potential is applied to the gate of the output at S_1. Before each new charge packets, are sensed, the reset clock ϕ_R returns the charge detector voltage to a fixed base level. An additional output amplifier is driven with only reset signal ϕ_R to provide an output at the terminal CS which is similar in waveform as the reset transient present in the video output signal. This is used for the suppression of the reset clock transient present in the video output signal by the video processing circuit.

Drive Waveform Generators (Sequencer) :

Fig.2 shows the block diagram of the scheme used for the generation of various clock pulsed needed for CCD chip and the raster for display. Broadly it consists of the following functional blocks (1) Master Oscillator (2) Horizontal line counter (3) Vertical line counter (4) Buffer and MOS clock drivers (5) Sweep Generators.

Master Oscillator :

This generates 2.24 MHz as the fundamental clock frequency. All other system clocks are derived and signal output of the horizontal counter, a +5 volt and ground as inputs. The line selector in conjuction with horizontal and vertical counter generates vertical clock pulses ϕ_{V_1} ϕ_{V_2} and photogate clock ϕ_p. The select address for the line sector is derived from the vertical line counter.

Buffer and MOS clock drivers :

CCD apart from being highly capacitive MOS device needs drive voltage levels of +5 volt maximum to -8.5 volt minimum. Thus all the clock pulses first generate at TTL are then translated to MOS level (+5 volt to -8-5 volt) by the MOS clock drivers and buffer circuit.

Sweep generators :

This generates horizontal and vertical sweeps as raster for the display. The horizontal sweep is generated using terminal count Tc output as trigger pulse for sweep generator. The vertical sweep is generated using photogate clock pulse.

Video signal processing :

Fig.3A and 3B shows the various waveform generated by the above scheme. The video output of CCD at S_1 port contains a large amplitude of Reset clock transient. This is called Read out noise and has to be removed from the video signal before it is to be amplified for display and sychronized with the master oscillator clock frequency.

Horizontal line counter :

This is incorporated for the generation of 105 Horizontal clock pulses to transfer out serially one row of information stored in horizontal register before it is ready to transfer the next row of information. It consists

of a pair of 4 bit presettable counter (74161) preloaded for a counting module 224 with master oscillator output as clock pulses which are half the master oscillator frequency. The three waveforms generated by the horizontal line counters namely divided by 2 at Q_o, Terminal count at Tc and divided by 224 at Q_3 are utilized for the generation of other waveforms needed. The divide by two output at Q is used to generate complementary horizontal clocks ϕH_1 ϕH_2 and ϕR the reset clock. The inverted square wave output of the divided by 224 at Q_3 is used as clock for the vertical line counter and the terminal count output To is used for triggering the horizontal sweep generators as well as in line selector.

Vertical line counter :

It consists of pair of 74161 : The first seven stages of the total 8 are presetted for counting modulo 51. The last stage of the counter acts as toggle Flip-Flop and work as odd/even field identifier. A dual 4 line to one line selector 74153 is used as combinational logic using Tc and Q_3. The read-out noise is minimised by subtracting a fraction of compensating amplifier output, available at CS, from the video signal in a video operational amplifier 733, as shown in Figure 4. Compensating amplifier is driven by reset clock ϕR and appears at the port CS.

The video and compensating amplifier output signal are applied to the differential amplifier through buffer stages having provision for level adjustment of signal. The input level of CS signal is so adjusted as to cancel the read out noise due to reset signal from the video signal at the differential amplifier output. The voltage gain of 733 has been programmed to only 10 to avail the maximum video band width. The output of the differential amplifier is further amplified in amplitude for intensity modulation.

SIMPLE CCD CAMERA SYSTEM :

Fig.5 shows the block diagram of a simple Camera and display system. The image of an object to be displayed is focussed by a suitable lens system on the image sensitive area of CCD and all drive clock pulse are applied to the CCD chip. To display the image of the object on the Oscilloscope the processed video output after amplification is applied to the Z input and the horizontal and vertical sweeps are applied to the X and Y input of the oscilloscope.

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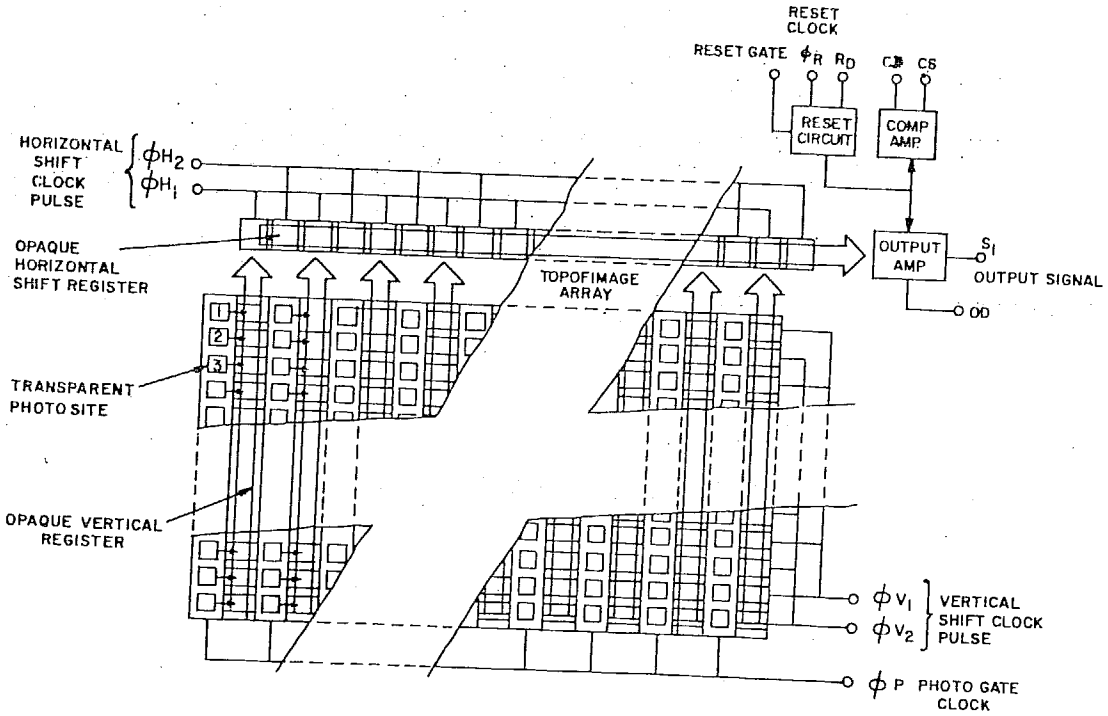

BLOCK DIAGRAM OF CCD - 201
INTER LINE TRANSFER AREA IMAGE SENSOR
FIG. 1

BLOCK DIAGRAM OF SEQUENCER
& DRIVER

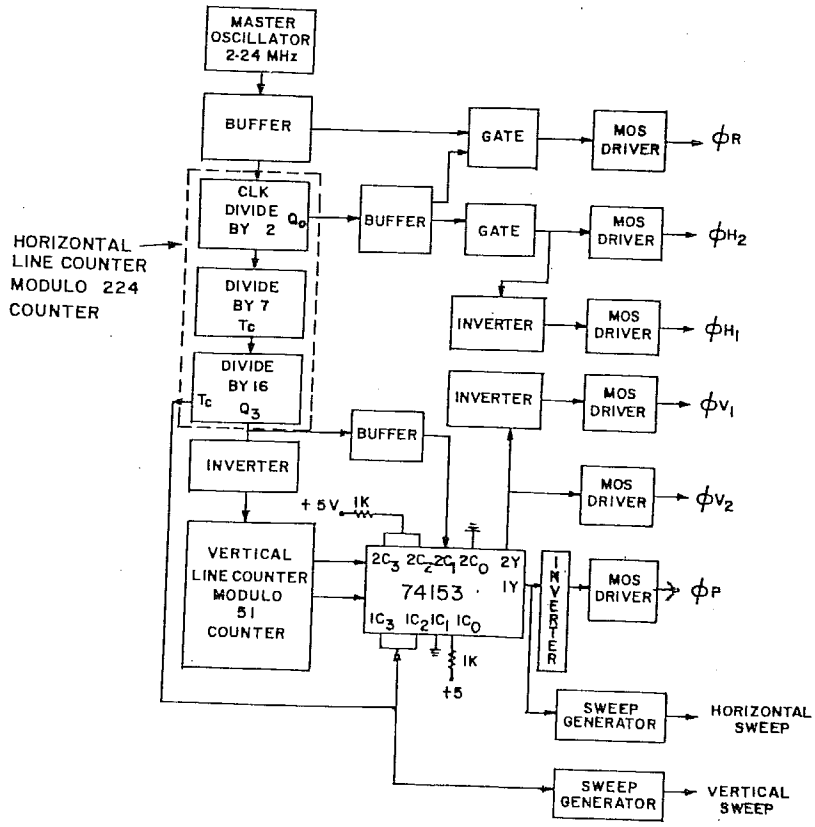

FIG. 2

VIDEO PROCESSING CIRCUIT

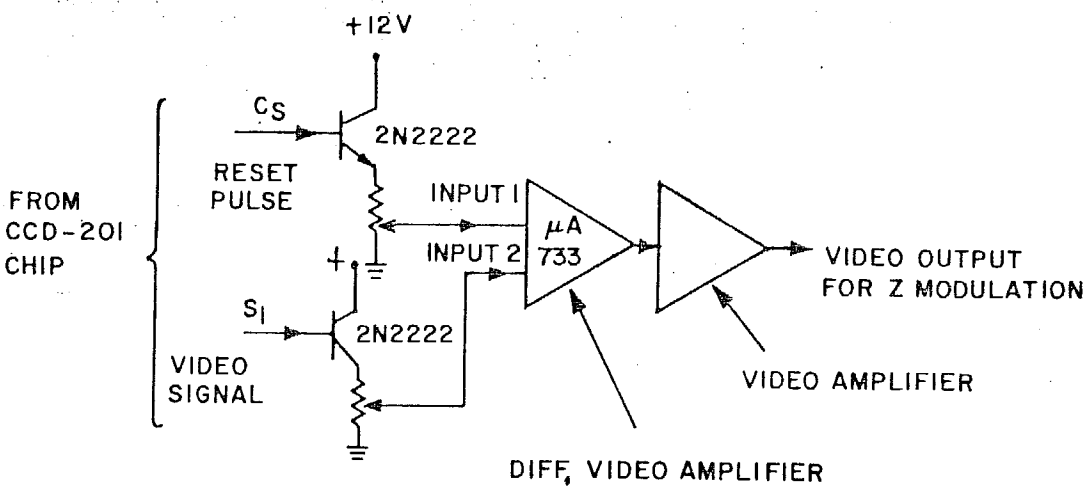

FIG. 4

BLOCK DIAGRAM OF SIMPLE CCD CAMERA
& DISPLAY SYSTEM

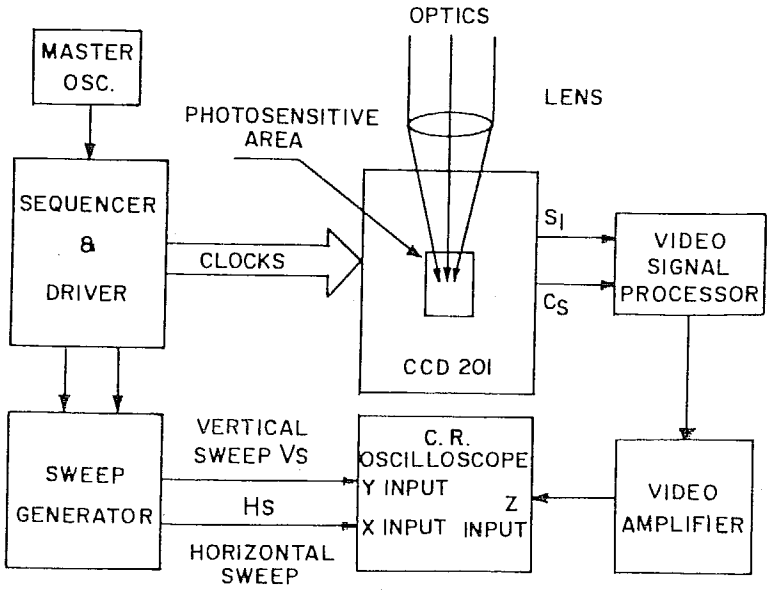

FIG. 5