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Technical Note

Design and Development of an Onboard E-Calibration Source for Current & Charge Detection for Space-borne Instruments

by

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Abstract
This report presents the design and development of an Electronic (E)-calibration source, capable of generating precise and known bipolar DC currents in the range of 100 picoamperes (pA) to 5 microamperes (μA). The source is designed for onboard calibration of highly sensitive current measuring instruments, particularly those used in space-based scientific payloads. The E-calibration source design also includes a switching mechanism that enables seamless toggling between the calibration current generated and the actual detector current using a pulse command signal. This enables efficient and accurate onboard space calibration without any interruption of ongoing system operations and manual intervention. The electronic calibration source can correct the inaccuracy of raw data to maintain accuracy, stability and reliability of the processed data, and will play a crucial role in ensuring the fidelity of data collected from critical space missions.

Keywords
Onboard Calibration, Current Source, Switching, PRL, Space instruments

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Contents

1. Introduction

In recent years, a wide array of scientific instruments has been deployed on space missions to study the near-Earth environment and interplanetary space. This environment primarily consists of plasma generated by solar radiation, resulting in the formation of ions and electrons (Kelly, 2009). To further our understanding of the near-Earth space and the different phenomena occurring in it, it is vital to characterize this plasma, which can be achieved using various in-situ instruments. These instruments are designed to measure key plasma parameters such as ion density, electron density, ion drift velocities, ion energy, and electron temperature, etc (e.g., Kelly, 2009; Heelis et al., 2017). These physical parameters are not measured directly but are instead derived from precise measurements of ion and electron currents collected by the instrument (Chen, 2003).

Typically, such measurements follow a well-defined signal processing sequence, as illustrated in **Figure 1**. In this sequence, charged particles (positive or negative charge) are collected by a collector/detector. The current generated is proportional to the flux/density of the collected particles, which varies significantly as a function of day/night, high/low solar activity, latitudes, altitudes, season, etc., leading to a broad dynamic range of currents. The resulting current is then converted into a voltage signal using a trans-impedance amplifier conversion stage, which often includes linear variable gain or logarithmic trans-impedance amplifiers to accommodate wide dynamic ranges of current (Hershkowitz et al., 1989). The analog signal is subsequently passed through signal conditioning amplifiers, then digitized using an Analog-to-Digital

Converter (ADC), and finally processed by a Microcontroller or Field Programmable Gate Array (FPGA) for storage, telemetry, and onboard decision-making.

The accuracy and stability of current measurement systems in space-borne instruments are significantly influenced by environmental factors like temperature fluctuations, aging of electronic components resulting in shifts in OpAmp bias currents, and drifts in gain-defining resistors and capacitors. All of these can degrade the fidelity of the measured current. This, in turn, affects the reliability of the derived plasma parameters (Hanson et al., 1973). Therefore, validating the integrity of the entire signal chain is essential to ensure consistent performance and measurement reliability during long-term operations.

While pre-launch validation using bench tests and vacuum chamber experiments can confirm baseline functionality, these methods are insufficient to account for dynamic variations that might occur in-flight conditions. In the harsh and variable thermal environments encountered in space, maintaining long-term stability and accuracy of measurements demands an onboard calibration mechanism capable of providing knowledge of the transfer function of the measurement circuit to carry out relevant corrections while processing raw data. Periodic calibration is carried out to minimize error in measurement data by updating the correction coefficient in raw data processing.

To address this need, an electronic calibration strategy is proposed in this work, wherein a known, programmable calibration current is periodically injected into the analog Front-End Electronics (FEE). This approach enables the detection of deviations caused by temperature variations, radiation exposure, or component aging, and facilitates post-processing data correction, thereby preserving the accuracy of the measurement system throughout the mission. The calibration source developed for this purpose provides a highly stable and accurate current output, programmable across a wide range of currents from 100 pA to 5 μA. By enabling in-flight validation and correction, this onboard calibration capability ensures long-term stability and accuracy of current measurements in post-processing data, ultimately enhancing the scientific validity of the measured plasma parameters in extended space missions.

2. Design and Development of E-Calibration Source

The block diagram of the designed E-calibration source along with the instrument normal chain is illustrated in **Figure 2**. The system has been developed to generate a load-independent, programmable current ranging from 100 pA to 5 μA, and it can be switched from the main electronics as per our requirements. This wide range of calibration current is achieved by controlling two reference voltages, V_1 and V_2, which are set via Digital-to-Analog Converters (DACs) and a source resistance R_s.

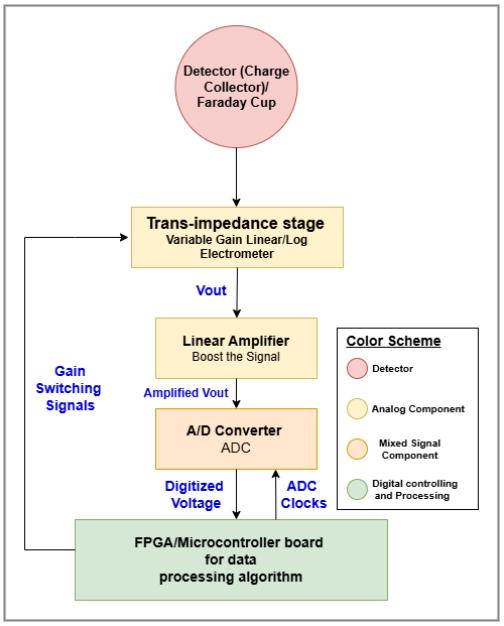

Figure 1. Signal processing block diagram of a general ion/electron measuring space-borne instrument

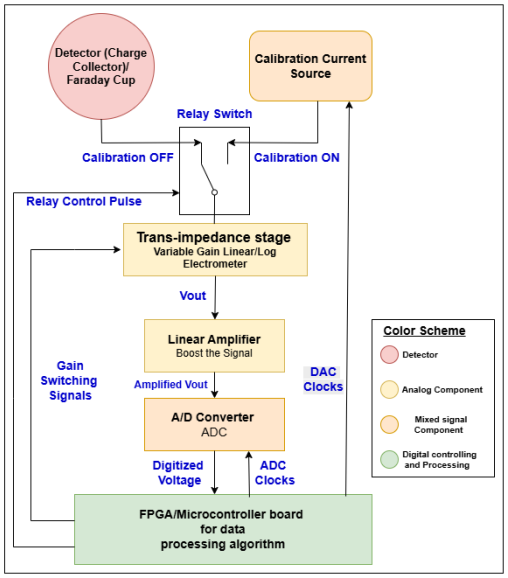

Figure 2. Signal processing block diagram of a general ion/electron measuring space-borne instrument, along with E-calibration source for the onboard calibration of the instrument

2.1 Subsystems of E-calibration source

There are majorly three subsystems of E-calibration source:

1. Load-Independent Current Source
2. Switching of Detector and Current Source
3. DAC and FPGA interface

2.1.1 Load-Independent Current Source

Accurate calibration of the measurement chain requires a design of current source with minimal leakage and high precision across the complete range of calibration. To meet these requirements, we designed a load-independent Howland current source, which achieves better than 95% accuracy over the complete range of generated current of 100 pA to 5 µA by using two programmable voltage references V_1 and V_2 and a resistance (R_s) (Texas Instruments, 2007). **Figure 3** depicts the schematic of the designed current source, which employs an LMP7704 OpAmp (Texas Instruments, 2024). The calibration currents are set by two DACs that generate voltages, V_1 and V_2. Resistors R_1 to R_4 are approximately equal (<=1% tolerence), ensuring that the output current (I_{out}) depends solely on the voltage differential across the source resistor R_s, as per the **Equation 1**.

$$I_{\text{out}} = \frac{V_2 - V_1}{R_s} \tag{1}$$

Although both the E-CAL circuit and the measurement electronics are co-located and therefore subject to the same thermal and environmental conditions, the E-CAL circuitry is deliberately designed to be minimal and thermally robust, serving as a stable calibration reference. The circuit employs precision resistors or RNC90 series of resistor from qualified resistor family which has tolerences in the range of 0.1%, low temperature coefficient in the range of 2 to 5 ppm/°C, a low-drift op-amp (LMP7704), and a stable DAC to ensure consistent performance under varying thermal conditions. Simulation and thermal chamber test results demonstrating the temperature stability of the E-CAL output are provided in sections 3 and 4. Additionally, to support long-term reliability and in-situ validation, the E-CAL current source includes a provision for digital monitoring using TI ADS1278, a 24-bit sigma-delta ADC, of which 16 bits will be utilized for the E-Cal data path. E-Cal offset (with zero DAC code) is measured during each calibration cycle. Since the detector input is disconnected during E-Cal, this offset can be digitized and stored in the FPGA and transmitted to ground for offset corrections. This approach may offers the potential to compensate for temperature-induced offset drift effectively, further enhancing the robustness of the calibration scheme.

2.1.2 Switching of Detector and Current Source

During routine instrument operation, the calibration source must remain isolated to prevent interference with actual measurements. When an in-flight calibration sequence is initiated, the FPGA issues an ON pulse to the relay driver, closing the relay and integrating the calibration current source into the signal path and isolating the detector to calibrate the electronics chain, as shown in **Figure 2**. Once calibration is complete, an OFF pulse from FPGA disengages the relay, restoring normal detector operation in an automated manner. **Figure 4** represents the schematic of developed switching electronics , featuring a GP250 120 E 00 12 (Nominal Voltage: 12V, Resistance 120 ohm) relay controlled by a transistor based driver circuit. The relay driver receives a digital ON/OFF pulse command typically from the FPGA or from the spacecraft to actuate the relay, thereby connecting or isolating the E-calibration source from the instrument's primary measurement chain (Leach International, 2024). Additionally, that disabling E-Cal through a zero-code DAC setting could potentially eliminate the need for a physical switch. However, in our current design, the switch/relay plays a critical role in completely isolating the calibration path, thereby minimizing any residual leakage or capacitive coupling to the detector input during actual measurements. This is essential for maintaining signal integrity, particularly in the detection of ultra-low currents in the picoampere range. Furthermore, the inherent zero-code error of the DAC may introduce additional offset currents. For example, a zero error of 0.5 mV across a 10 MΩ R_s can result in a leakage current of approximately 50 pA, which is non-negligible in such sensitive measurements.

In the current design, the two inputs of the GP250 relay are connected to the detector and the E calibration source, respectively, with the relay output routed to the FEE input. To minimize harness length and connector losses, the ECAL circuit, relay, and FEE are intended to be integrated onto a single PCB in future iterations. While this approach increases layout complexity, it offers enhanced signal integrity and overall system robustness, making it a worthwhile trade-off. However, during calibration mode, the detector remains floating in this configuration, which is a potential drawback. As part of ongoing testing, we are evaluating the calibration duty cycle to ensure that the floating condition does not degrade detector performance. Additionally, we are also exploring ways to avoid any switching in the detector-to-FEE path by implementing a calibration-only switching scheme. In this approach, the detector would be temporarily disabled either by turning off or reducing its bias supply whenever calibration is active. This would allow the E-calibration signal to be routed independently to the FEE without interfering with the detector signal. We find this approach promising and plan to explore its feasibility in hardware, especially in scenarios requiring high signal integrity. However, this scheme would only be applicable in systems where the detector can be safely disabled during calibration so that detector signal will not intermixed with the E-calibration signal.

2.1.3 DAC and FPGA Interface

Two 12-bit DACs are used to generate the reference voltages V_1 and V_2. By programming different combinations of V_1 and V_2, a range of calibration currents is produced according to the **Equation 1**. The DAC clocks and relay pulses have been controlled using the FPGA. The FPGA generates

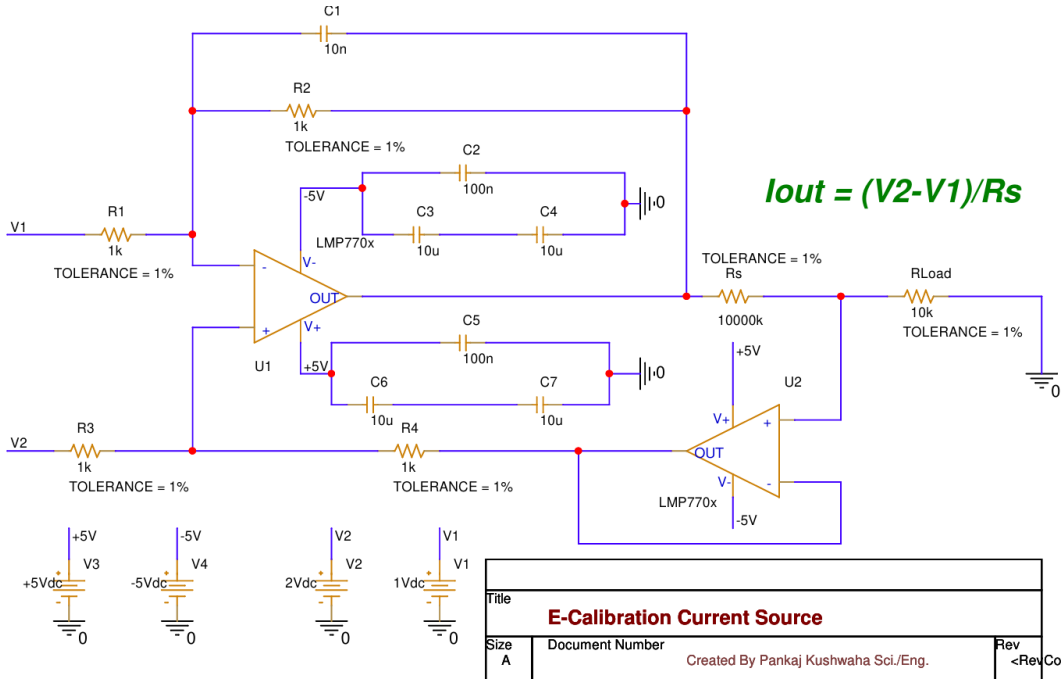

Figure 3. Schematic of designed load-independent current source

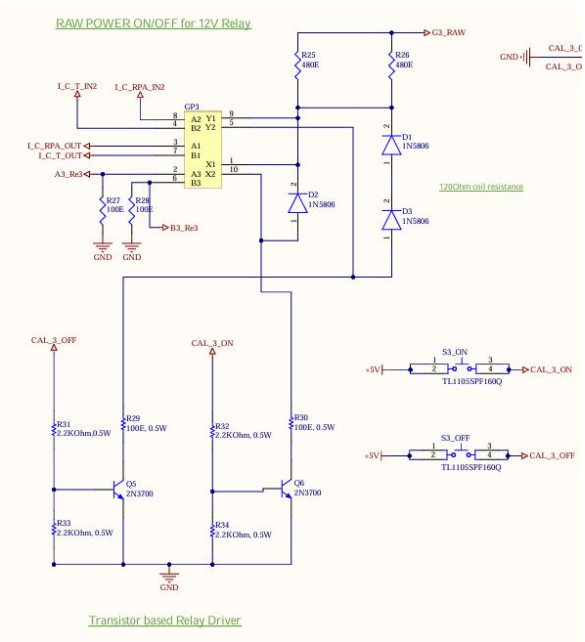

Figure 4. Schematic of designed switching circuit of E-calibration source contains the GP250/CP250 relay and its transistor based driver circuitry

the DAC serial interface and the relay control pulses, ensuring synchronized operation of voltage setting and switching (Texas Instruments, 2016). The current implementation of the E-calibration source has been tested using our developed processing card based on a commercial off-the-shelf (COTS) ProASIC3E FPGA. This FPGA meets the functional requirements for digital control and data handling during the initial development and validation phases of the E calibration source. For the space-qualified version, we intend to use the RTAX2000 FPGA, which is a radiation-tolerant device suitable for space applications. This FPGA will be incorporated into the final flight version processing card, where it will support all digital processing tasks required by both the primary instrument and the onboard calibration circuitry.

We also acknowledge that DAC non-idealities such as Differential Non-Linearity (DNL), Integral Non-Linearity (INL), gain error, and offset error can impact the precision of current generation. In the present prototype, V_1 and V_2 are provided by a 16-bit DAQ system, whose associated voltage errors are typically within hundreds of microvolts. When applied across a 10 MΩ R_s, this results in a current error on the order of tens of picoamperes, which is acceptable for the intended calibration range. Despite these limitations, the ECAL source consistently achieves better than 95% accuracy in the lower picoampere range, and up to 98% or better at higher currents and results were shown in section 3 and 4. Future iterations will employ the space-qualified DAC5675A-SP, a 14-bit precision DAC in the design.

The use of two DACs and two biasing voltages ($\pm 5\ V$) in the current design is required, as the circuit's ability to support bipolar current output is essential for accurately simulat-

ing both ion and electron current flows in space instrumentation. In addition to this, dual-supply operation improves slew rate margins and settling behavior, which can be important for calibration systems requiring fast switching between current levels. Even though the op-amp used is RRIO (rail-to-rail input/output), practical limitations such as output swing degradation near rails, load driving capability, and increased distortion near the supply limits may affect accuracy. The dual DAC approach also offers improved resolution and flexibility, allowing finer control over current levels than a single DAC could achieve. Moreover, it enhances offset matching when generating small differential voltages, for instance, using 1.0 V and 0.9 V instead of relying on a single DAC referenced to ground, thereby reducing relative error and improving noise immunity. However, if the application requires only a unipolar current, the design can be reconfigured to operate with a single DAC and single supply by one input and one biasing as a grounded.

A detailed parameter comparison table is added for selection and finalization of DAC and Opamp in **Table 1** and **Table 2**.

Based on the components datasheet, simulations, and hardware results, the specifications of the E calibration source are presented in **Table 3**.

2.2 Modes of Operation

As shown in **Figure 2**, instrument will operate in two distinct modes:

1. Calibration OFF Mode
2. Calibration ON Mode

2.2.1 Calibration OFF mode

It is a normal mode of operation of the instrument. As shown in **Figure 2**, The current sources are electrically disconnected from the main electronics chain, and both V_1 and V_2 are set to 0 V and detector is directly connected with main electronics chain for the electron and ion measurements. However, due to the low bias current of the operational amplifier, a small leakage current in the range of pA may still flow into the circuit, potentially introducing measurement errors. To eliminate this residual error, relay switches are used to completely isolate the calibration circuit from the main electronics chain of the instrument.

2.2.2 Calibration ON mode

In this mode of operation, as shown in **Figure 2**, the relay configuration switches the known current source into the main measurement chain, while simultaneously disconnecting the detector input. This setup allows the calibration of the FEE, which contains an I/V converter, amplifiers, and ADC, using the known injected current. After calibration, correction factors for gain, resistance drift, and temperature coefficients can be applied to enhance the accuracy and stability of the measurement system over time. This approach ensures that any variations in the electronic components due to temperature changes, aging, or other environmental effects can be compensated for, thereby improving the long-term precision of the instrument's current measurement capabilities.

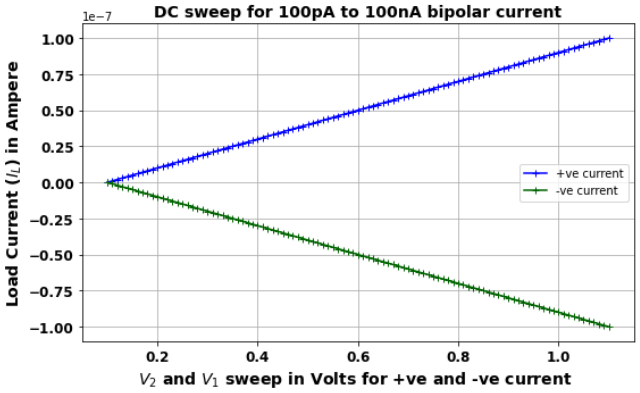

Figure 5. DC Sweep simulation for the generation of 100 pA to 100 nA of bipolar current. In which V_1 = 100 mV and R_s = 10 MΩ and V_2 sweeps from 100 mV to 1.1 V with a step of 1 mV for positive current (blue) and vice-versa for negative current (green) generation

Table 4 depicts the major components used in the development of the E-calibration source and their equivalent space-qualified components part numbers so that the same circuitry can be realized using the space-qualified components for the development of a space-borne instrument calibration system. In addition to this a comprehensive worst-case drift error ΔT (–20°C to +65°C) has been added in **Table 5** based on datasheet specifications for each component (DAC, OPAMP, and resistors) to see the effect of temperature change. This includes gain and offset errors, temperature coefficients, and reference voltage drifts.

3. Simulations and Hardware Results

The mentioned design of E-calibration source in **Figure 3** is simulated in PSpice software, and based on the results, a PCB is designed in Altium software.

3.1 Simulation Results

In the shown **Figure 5**, the DC sweep results of the designed current source are presented, demonstrating the generation of a bipolar current ranging from 100 pA to 100 nA. This is achieved by sweeping V_2 from 100 mV to 1.1 V in 1 mV steps while keeping V_1 fixed at 100 mV for positive current, and vice versa for negative current generation, with the resistor R_s set to 10 MΩ.

Similarly, **Figure 6** and **Figure 7** show the DC sweep results from the current source designed for generating a bipolar current from 100 nA to 0.5 μA and 0.5 μA to 5 μA, respectively. Hence, the simulation results shown in **Figure 5**, **Figure 6**, and **Figure 7** depict the generation of 100 pA to 5 μA of current from the designed current source.

Table 1. Comparison of DACs based on different key parameters

S. No.	Parameter	DAC121S101	DAC5670	DAC5675	DAC8165
1	Bit Depth	12	14	14	14
2	Zero Error / Offset Error	2.1 mV (Typ)	±0.09% FSR = 2.9 mV (3.3V)	0.01% FSR	±5 mV
3	DNL	+0.21, -0.10 LSB	±0.8 LSB = 40 µV (3.3V)	±0.6 LSB = 30 µV (3.3V)	±0.3 LSB
4	INL	8 LSB max, ±2.75 LSB typ	±1.5 LSB = 75 µV (3.3V)	±1.5 LSB = 75 µV (3.3V)	–
5	FS Error	-0.04% FS = -5 mV (5V FS)	58 mV (3.3V) + offset	165 mV (3.3V)	±0.2% FSR
6	Gain Error	0.11% FSR (typ)	±1.6% FSR (typ)	5% FSR	-0.5% FSR
7	V_{Supply}	5V	3.3V	3.3V	5V
8	Max Sample Rate	2 MSPS max	1.2 GSPS	400 MSPS	2 MSPS
9	Package	10-lead CFP	CBGA 192	HFG 52	TSSOP-16
10	Control Interface	SPI	LVDS + HyperTransport	LVDS	SPI
11	Power	1.19 mW (Nominal)	2 W	660 mW	3.3 mW
12	Temp. Drift	–20 µV/°C	75 ppm of FSR/°C	12 ppm of FSR/°C	5 ppm/°C
13	Space Qualified	Qualified	Qualified	Qualified	Not Qualified

Table 2. Comparison of Op-Amps Based on Key Parameters

S. No.	Parameter	Requirement	LMP7704-SP	OPA4277UA-SP	ADA4610S	AD648S	AD549
1	Input Offset Current @27°C	<5 pA	±500 fA	±500 pA	±25 pA	±10 pA (max)	±60 fA
2	Input Offset Voltage @27°C	<100 µV	±60 µV	20 µV	±400 µV	±2 mV (max)	±500 µV
3	No. of Channels	4	4	4	4	1	1
4	Space Qualified	Yes	Yes, 100 krad(Si)	Yes, 100 krad(Si)	Yes, 100 krad(Si)	Yes, 100 krad(Si)	No
5	Unity Gain Bandwidth	1 MHz	2.5 MHz	2.5 MHz	5 MHz	1 MHz (typical)	1 MHz (typical, MIL grade)
6	Operating Temperature Range	–55°C to +125°C	–55°C to +125°C	–55°C to +125°C	–55°C to +125°C	–55°C to +125°C	–55°C to +125°C

Table 3. Specification of the E-Calibration Current Source

S.N.	Specification	Value	Remarks
1	Current range	100 pA to 5 µA bipolar	100 pA to 0.5 µA with 10 MΩ resistor; 0.5 µA to 5 µA with 1 MΩ resistor
2	Power	150 mW	For generation of bipolar current using ±5 V bias
3	Footprint	50 mm × 50 mm	2-channel E-calibration current source considering footprint of space qualified components
4	Mass	≈15 gm	≈10 gm is contributed by relay mass and excluding enclosure, shielding, and SMA connectors
5	Resolution	10 pA	Considering 14 bit DAC resolution
6	Biasing voltage requirements	±5 V	Opamp and DAC Biasing voltage
7	Output Impedance	1 Hz–10 Hz: Z_{out} ≈ 10 MΩ 1 kHz–100 kHz: Z_{out} ≈ 1 MΩ	Output impedance varies with frequency
8	Accuracy	pA range: 95% nA to µA range: 99%	Based on measured calibration performance
9	Stability	Stable up to 100 kHz	Gain margin ≈ 20 dB; Phase margin ≈ +45°; Unity gain ≈ 3 MHz
10	Full-Scale Linearity	99%	Based on measured and ideal current linearity
11	Settling Time	1 ms	Limited by DAC speed and circuit bandwidth
12	Operating Temp	–20 °C to 65 °C	Based on thermal testing
13	RMS noise over DC signal	10 pA RMS	

Table 4. Major Components and their equivalent space-qualified components used in the design of E-calibration source

S. No.	Component Type	COTS Component	Space-Qualified Component	Critical Parameter
1	Precision Op-Amp	LMP7704UA	LMP7704-SP	Low Bias Current: 0.2 to 0.5 pA @ 25°C 400 pA @ 125°C
2	Switch / Relay	CP250	GP250 120 E 00 12 or GP250 40 E 00 06	Space-qualified; Nominal operating voltage: 12 V or 6 V
3	DAC (Digital to Analog Converter)	DAC121S102 (12-bit) and DAQ (16-bit)	DAC5675A-SP (14-bit)	<1 mV Voltage Resolution
4	FPGA (Field Programmable and Gate Array)	PROASIC3E Microchip FPGA	RTAX2000 Microchip	Space-qualified

Table 5. Component Parameter Drift Estimation over Temperature Range of –20°C to +65°C

Component	Parameter	Value	Temp. Coefficient	Drift over ΔT (–20°C to +65°C)
DAC	Gain Error	±10%	±100 ppm/°C	±0.85% over 85°C
DAC	V_{ref} Drift	±60 mV	±50 ppm/°C	±4.25 mV
OPAMP	V_{OS}	±0.3 mV	±1.5 µV/°C	±127.5 µV
OPAMP	I_B	100 pA	±0.5 pA/°C	±42.5 pA
Resistor	Value	10 kΩ	10 ppm/°C	±0.085%

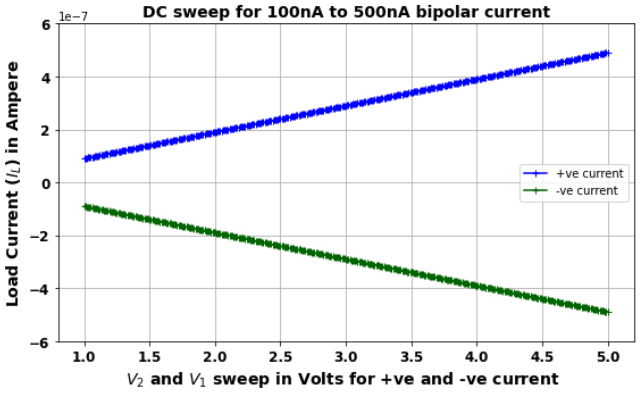

Figure 6. DC Sweep simulation for the generation of 100nA to 0.5 μA of bipolar current. In which V_1= 100 mV and R_s = 10 MΩ constant and V_2 sweeps from 1 V to 5 V with the step of 10 mV for positive current (blue) and vice-versa for negative current (green)

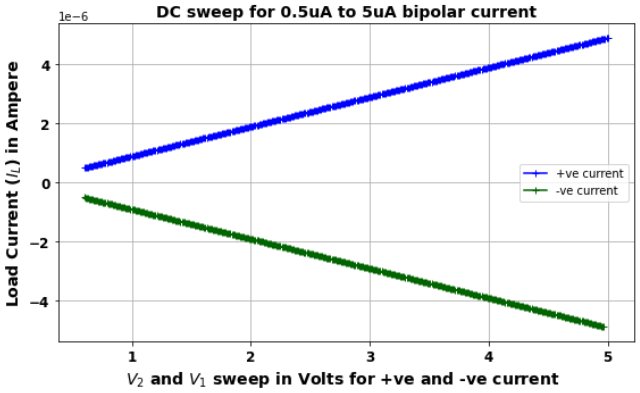

Figure 7. DC Sweep simulation for the generation of 0.5 μA to 5 μA of bipolar current. In which V_1= 100 mV , V_2 sweeps from 0.6 V to 5 V with the step of 10 mV for positive current (blue) and vice-versa for negative current (green) keeping R_s = 1 MΩ constant

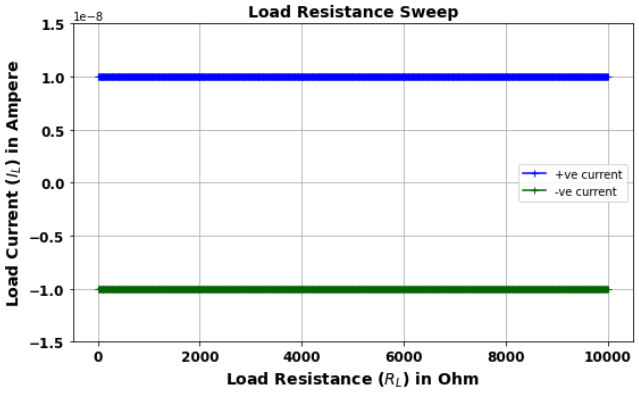

Figure 8. Load Resistance (R_{load}) Sweep simulation for the generation of 10 nA bipolar constant current. In which R_{load} sweeps from 10 Ω to 10 kΩ with the step of 10 Ω, V_1 = 2.4 V, V_2 = 2.5 V for 10nA and V_1 = 2.5 V, V_2 = 2.4 V for -10nA, keeping R_s = 10 MΩ constant

Figure 8 shows the simulation results for the load resistance (R_{load}) sweeps from 10 Ω to 10 kΩ in the steps of 10 Ω, for positive 10nA keeping V_1 = 2.4 V, V_2 = 2.5 V, and vice-versa for negative 10nA, keeping R_s= 10 MΩ constant. As we can see in the results, the current remains constant at ±10 nA for the complete variation of load resistance from 10 Ω to 10 kΩ, which confirms that the current output is independent of load variations. The above simulation results show that our designed load-independent current source functions properly for the generation of constant current under conditions of varying load. Hence, due to the load independence capability of the designed E-calibration source, this E-calibration approach can be used with the various designs of FEE in the development of space-borne instruments. To see the variation in the E calibration current source due to temperature change, a temperature sweep simulation is carried out. **Figure 9** shows the temperature sweep simulation of -20°C to 120°C with a step of 1°C for the generation of different constant currents from pA to μA range. In which we have considered resistance tolerences of 1%, temperature coefficients TC_1 and TC_2 is 5 ppm/°C and 1 ppm/°C respectively for each resistors. As we can see that small currents in the picoampere range are more sensitive to temperature variations. To investigate this further, the E-calibration source was also evaluated in a controlled thermal chamber, and the corresponding results are presented in Section 4.

3.2 Hardware Results

Based on the simulation results, the circuit is optimized and a 6-layer PCB layout is designed as shown in **Figure 10**. This PCB contains six different current calibration channels, which can generate six different currents from 100 pA to 5 μA based on the required calibration currents using voltage combinations of V_1 and V_2 for each channel. To ensure a minimum leakage and maintain a proper signal integrity, a 6-layer PCB

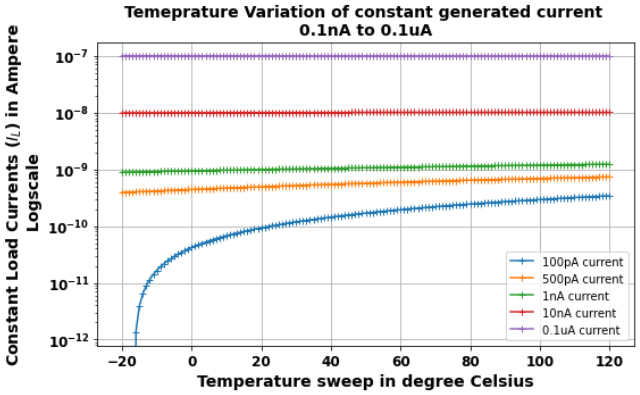

Figure 9. Temperature sweep simulation from -20°C to 120°C in a step of 1°C. Resistance tolerences of 1% and TC_1, TC_2 is 5 ppm/°C and 1 ppm/°C respectively for each resistor to generate the constant currents of 100 pA, 500 pA, 1 nA, 10 nA and 100 nA

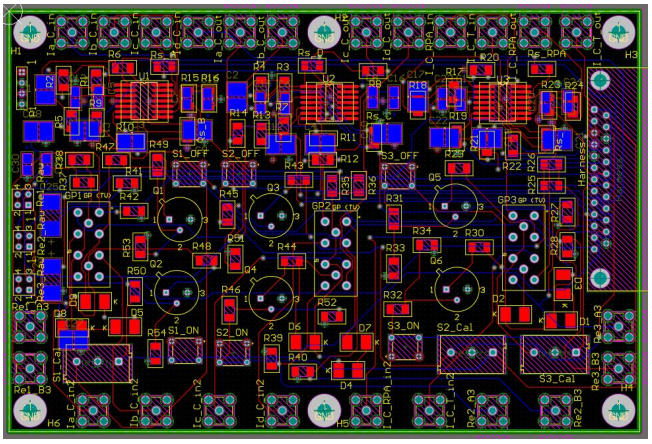

Figure 10. PCB Layout of six-channel E-calibration current source PCB which contains 6 layers (2 signal layer, 2 ground plane , and 2 power plane)

is designed and fabricated in which L_1, L_6 are signal layers, L_2, L_5 are ground plane layers, and L_3, L_4 are ±5V power plane layers. **Figure 11** shows the 150 mm × 100 mm fabricated PCB of six channel E-calibration source.

The designed PCB, shown in **Figure 11**, was tested and results were obtained for the generation of bipolar current ranges from 100 pA to 5 μA. The generated current was measured using a commercial high-precision 6.5-digit electrometer (B2987A), and the data was logged using the designed LabVIEW-based checkout system illustrated in **Figure 18**. The hardware testing was conducted for both polarities of currents, i.e., positive and negative, to enable the measurement of ions and electrons, respectively. In the results presented in **Figure 12** to **Figure 16**, the blue curves correspond to positive current measurements, while the green curves represent negative current measurements.

Figure 12 presents the plot of absolute ideal current versus measured current for generated bipolar current values ranging from 100 nA to 5 μA. In this experiment, V_1 is held constant at 0.1 V, R_s is fixed at 1 MΩ, and V_2 is varied from 1 V to 5 V in steps of 10 mV for positive current shown in blue color and V_2 = 0.1 V and V_1 is varied similarly for negative current shown in green color using Data Acquisition card (DAQ). The experiment was repeated 32 times with the same values of V_1, V_2, and R_s, to evaluate the consistency and repeatability of the generated current across the specified range.

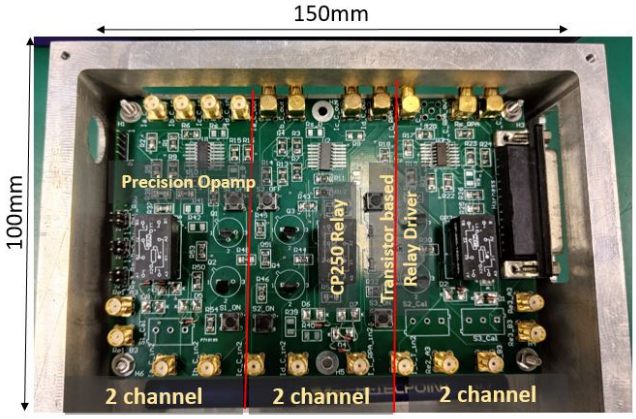

Figure 11. 150 mm × 100 mm 6-layer PCB of six-channel E-calibration source

Figure 13 depicts the corresponding percentage error graph for the measurements presented in **Figure 12**, where it can be observed that the majority of the current measurement errors are less than ±0.3% for the generation of bipolar currents in the range of 100 nA to 5μA.

A similar experiment was conducted to generate bipolar current ranges from 100 pA to 0.5 μA. **Figure 14** presents the plot of absolute ideal current versus measured current for this range. In this setup, V_1 is constant 0.1 V, V_2 is varied from 0.2 V to 5 V in steps of 1 mV for positive current generation, V_2 = 0.1 V and V_1 is varied similarly for negative current using a DAQ and R_s is fixed at 10 MΩ. The experiment was repeated 50 times to evaluate the consistency and repeatability of the generated current across the specified range, and the aggregated data is shown in **Figure 14**. The plot demonstrates a linear relationship between the ideal and measured currents during continuous data acquisition. To evaluate the measurement accuracy, a graph of theoretical current versus percentage current error is plotted as shown in **Figure 15**. It may be noted in this figure that for the bipolar currents generated in the range of 100 pA to 1 nA, the measured current error increases upto 2% to 5%. This increase in the measured current is primarily due to leakage currents in electronic components such as operational amplifiers. Nevertheless, for currents between 2 nA and 10 nA, the percentage error remains within ±1%, as shown in **Figure 15**. Similarly, **Figure 16** shows the error graph for bipolar current generated between 10 nA and 0.5 μA, wherein the measurement errors remain

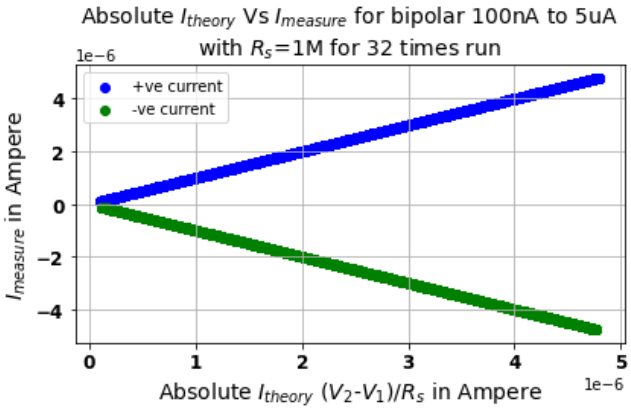

Figure 12. I_{theory} vs $I_{measure}$ for a current range of 100 nA to 5 μA and -100 nA to -5 μA using a constant resistor R_s = 1 $M\Omega$. For positive current (blue), V_1 = 0.1 V and V_2 is swept from 1 V to 5 V in 10 mV steps. For negative current (green), V_2 = 0.1 V and V_1 is sweeped similarly. The x-axis represents the absolute value of the theoretical current, calculated as $|I_{\text{theory}}| = |(V_2 - V_1)/R_s|$

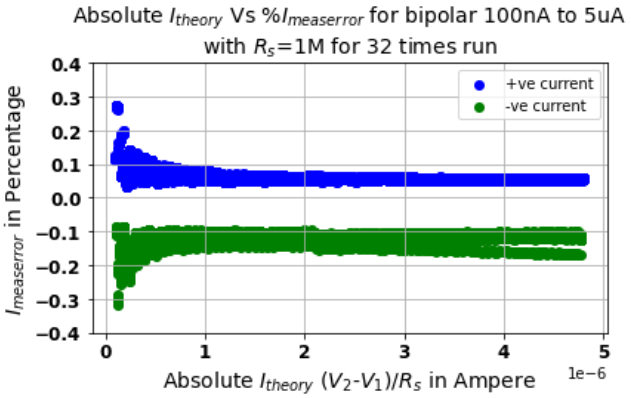

Figure 13. I_{theory} vs %$I_{measerror}$ for the bipolar current ranges from 100 nA to 5 μA for 32 times, Blue curves shows the measured current error corresponds to positive current whereas the green curves shows the negative current error

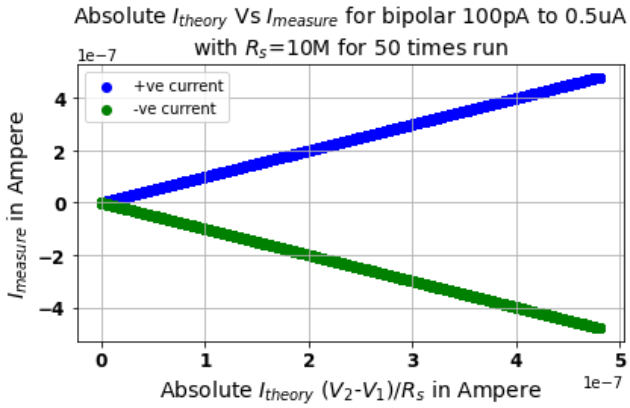

Figure 14. I_{theory} vs $I_{measure}$ for a current range of 100 pA to 0.5 μA and -100 pA to -0.5 μA using a constant resistor R_s = 10 $M\Omega$. For positive current (blue), V_1 = 0.1 V and V_2 is swept from 0.2 V to 5 V in 1 mV steps. For negative current (green), V_2 = 0.1 V and V_1 is varied similarly. The x-axis represents the absolute value of the theoretical current, calculated as $|I_{\text{theory}}| = |(V_2 - V_1)/R_s|$

within ±0.5%.

Figure 17 shows the test setup for the characterization of the designed current source, wherein the DAC control signal is being generated by the ProASIC3E (COTS) FPGA. For the characterization of the current source V_1 and V_2 values of the current source is generated by DAC. The digital correspondence of the values has been stored in the FPGA. A total 16 such V_1 and V_2 values are stored in the FPGA and are selected based on the control signal given by LabVIEW based characterization checkout software developed (Kushwaha et al., 2021). A screengrab of the software is shown in **Figure 18**. Based on the selected voltage values, the DAQ generates the digital signal to the FPGA, based on which the DAC values are changed to select the new current.

The preliminary test results for the interface between the designed ECAL and the first stage of the front-end electronics (FEE), which consists of a linear trans-impedance amplifier (TIA), were obtained. Currently, a 12-bit DAC is used to generate the control voltages V_1 and V_2. In this experiment, V_2 was held constant at 4.94 V, while V_1 was varied across discrete voltage levels. This configuration produced a discrete set of current values, which were initially measured using a commercial picoammeter. Subsequently, the picoammeter was replaced with the TIA to evaluate the impact of load connection on the designed E calibration source. The same combinations of V_1, V_2 and R_s were used during this test. **Figure 19** shows the comparison between the TIA-measured current (blue) output (derived from voltage measurement) and the picoammeter output (green). The results exhibit good agreement between the two, with a maximum offset of ±40 pA and a standard deviation (1-sigma variation) of approximately 3 pA. Further studies involving different gain stages are planned

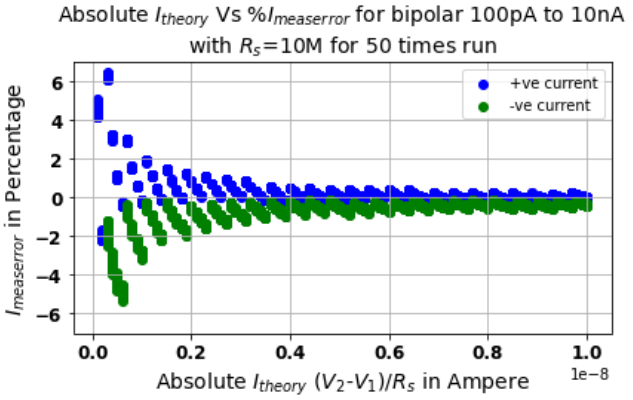

Figure 15. I_{theory} vs %$I_{measerror}$ for the bipolar current ranges from 100 pA to 10 nA in which blue and green shows the positive and negative measured current errors respectively

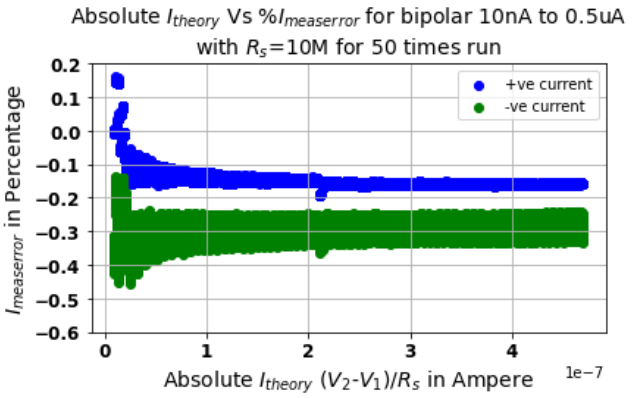

Figure 16. I_{theory} vs %$I_{measerror}$ for the bipolar current ranges from 10 nA to 0.5 μA in which blue and green shows the positive and negative measured current errors respectively

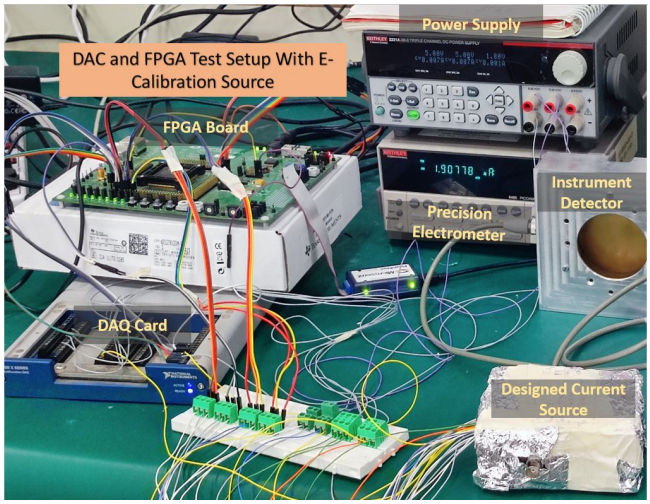

Figure 17. Hardware test setup for the generation of V_1 and V_2 variable voltages using DAC and FPGA

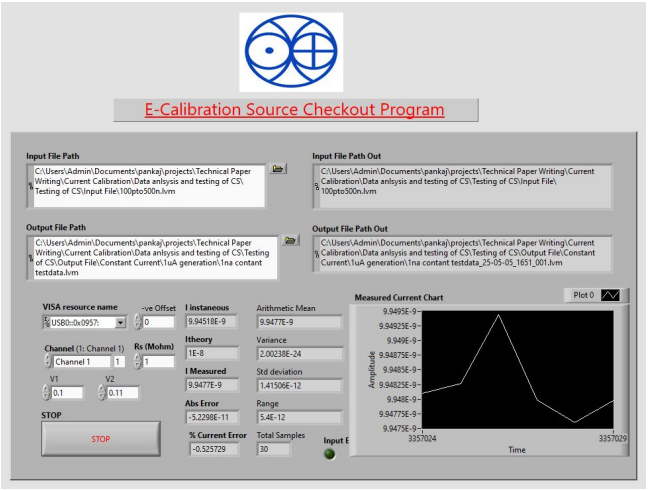

Figure 18. LabVIEW based checkout software for testing and characterization of E-Calibration Source

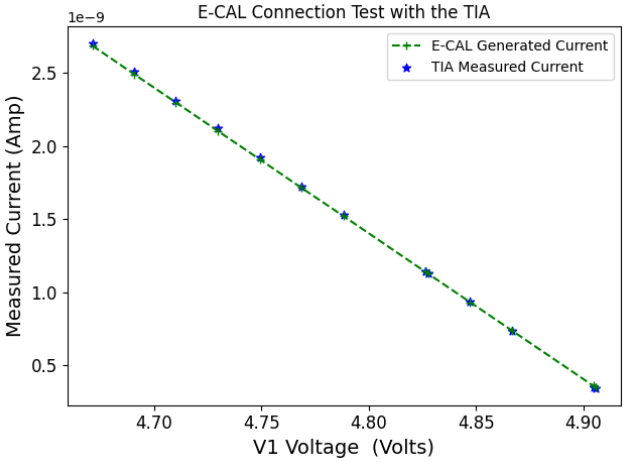

Figure 19. Comparison between ECAL generated current and measured TIA measured current for different V_1, and V_2 is kept constant at 4.94 V

for future work.

4. Thermal test of E-Calibration Source

The E-calibration source consists of precision operational amplifiers and resistors, whose performance with respect to temperature must be characterized. To evaluate this, the E-calibration source was tested inside a controlled thermal chamber, and measurements were recorded for different constant current settings. In this experiment, the thermal chamber was operated over a temperature range of –5 °C to 65 °C, considering that the present E-calibration circuit is built using commercial off-the-shelf (COTS) components rated for –25 °C to 85 °C. In this setup chamber followed a pre-programmed thermal cycling profile for a total duration of 7.5 hours. Initially, the temperature was decreased from 25 °C to –5 °C within the

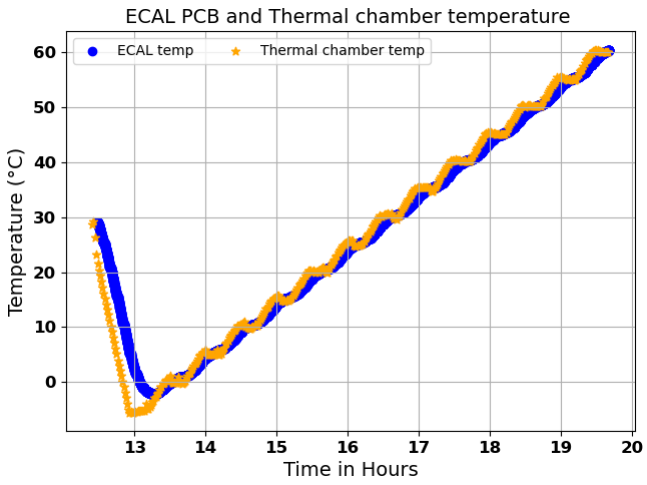

Figure 20. Temperature profile from –5 °C to 65 °C of the thermal chamber and the E-calibration PCB over a 7.5-hour thermal cycling test. The E calibration PCB temperature is in blue, and the chamber temperature is in orange

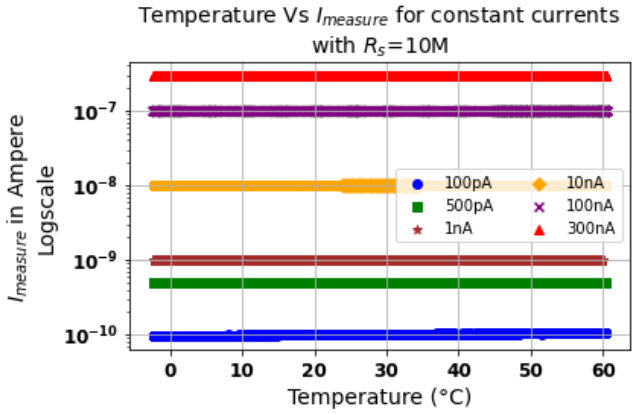

Figure 21. Thermal test of E-calibration source from –5 °C to 65 °C for different generated constant currents. X-axis represents the temperature of the E-calibration PCB, and Y-axis represents the current measurement in log scale

first 30 minutes. Thereafter, it was incremented in 5 °C steps every 15 minutes, with a dwell time of 15 minutes at each temperature point, until it reached 65 °C. **Figure 20** shows the temperature profile of the thermal chamber (orange) and the corresponding temperature of the E-calibration PCB (blue) as a function of time. The chamber temperature was recorded using the built-in RTD sensor, while the PCB temperature was measured using a PT100 sensor placed on the PCB and connected to a Keysight B2987A commercial electrometer. As observed, both temperature traces follow a similar trend, indicating consistent thermal tracking between the chamber and the E-calibration PCB.

Figure 21 shows the temperature performance, from 5 °C to 65 °C, of the different generated constant currents from the E-calibration source using the same thermal profile shown in **Figure 20**. As we may see in the graph, all discrete currents are quite stable for the whole range of temperature variations.

Figure 22 illustrates the current error across different constant current levels as a function of temperature, ranging from –5 °C to 65 °C. As observed, the current error remains within 1% for currents above 500 pA, indicating good temperature stability for this range of currents. However, for currents below 500 pA, the error increases with temperature variation, reaching up to 5%. This increased error is attributed to variations in the input bias current of the operational amplifier (400pA @ 125 °C), which become significant at picoampere levels, as discussed in **Table 5** of component drift error. Based on the current findings, it is inferred that maintaining a stable temperature between 20 °C and 30 °C is essential for reliable current generation below 500 pA. In future, further studies, including thermo-vacuum testing, are planned to comprehensively assess the temperature dependence of the precision E-calibration source.

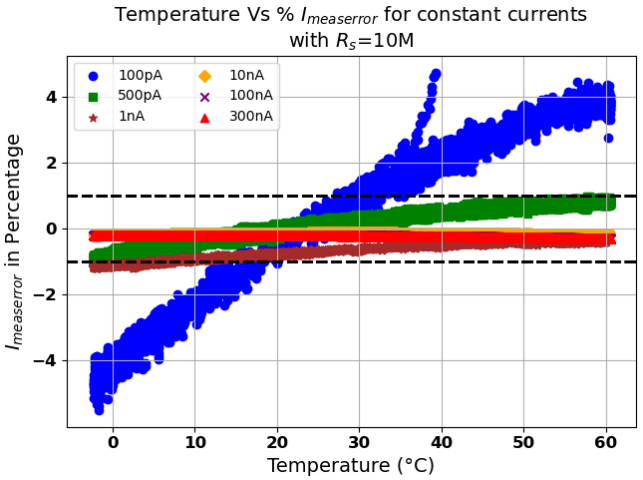

Figure 22. Current error across different constant current values as a function of temperature during the thermal test

5. Future Plans

As discussed, a design of calibration of currents in onboard systems is proposed. Supporting simulations, hardware and thermal tests are also demonstrated and are shown to be performing well. The proposed E-calibration source is suitable for integration with space-borne instruments to enable onboard calibration. In the future, the designed E-calibration source will be integrated with the FEE of our in-house developed ion measurements space-borne instrument, under consideration for flight in the upcoming ISRO's missions. In that design, there will be five independent channels of E-calibration source to generate five different currents simultaneously. As per our requirement, currents in the range of 100 pA to 0.5 μA will be generated using the R_s at 10 MΩ constant, and V_1, V_2 will be programmable using the onboard DACs for the required current generation for onboard calibration.

Table 6 shows the few values of test currents calculated corresponding to the wide range of ion densities expected in a typical low earth orbit. **Figure 23** illustrates the initial test setup of the E calibration source in conjunction with the instrument detector. In this setup, a continuous current of 300 pA is injected at one channel of the E-calibration source from a commercial current source through the detector, while relay circuitry switches between the designed current source and the detector current, the output current is measured using the precision electrometer and LabVIEW based checkout system to verify the complete functionality of the E-calibration source. The results demonstrate that the system is currently achieving an accuracy of 95% or better in measuring currents in the picoampere range, indicating that any degradation due to the current configuration is within acceptable limits. Furthermore, in the final implementation, the E calibration source will be integrated directly onto the FEE PCB, eliminating the need for additional connectors and harnessing in the detector signal path.

The final integrated PCB design, where the E calibration source and FEE will reside on the same board, we will implement guard rings around sensitive analog traces to minimize surface leakage currents and PCB-based routing, eliminating the need for external coaxial/sma harnesses, which further reduces leakage and improves reliability. These design modifications will ensure accurate and stable current generation, particularly for picoampere measurements, and will be incorporated in the flight version of the instrument.

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Table 6. Theoretically calculated currents using I = $\eta n_e A V_d$ formula, where transparency (η), Ion density n_e, Area of detector (A), Relative ion drift velocity V_d

Ion Density (n_e)	Current (I)
5×10^2 cm^{-3}	350 pA
1×10^3 cm^{-3}	700 pA
1×10^4 cm^{-3}	7 nA
1×10^5 cm^{-3}	70 nA
5×10^5 cm^{-3}	0.35 μA

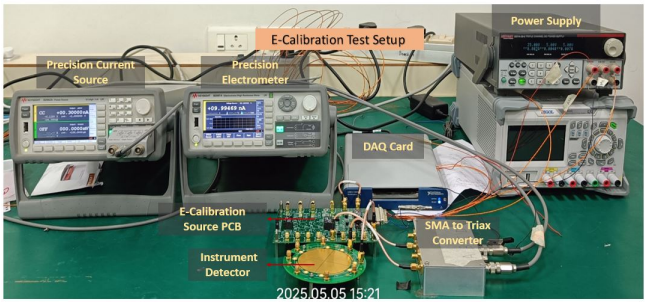

Figure 23. Test Setup for the six channel E-calibration source along with the instrument detector, commercial electrometer, and commercial current source

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PRL research encompasses the earth the sun immersed in the fields and radiations reaching from and to infinity, all that man's curiosity and intellect can reveal

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